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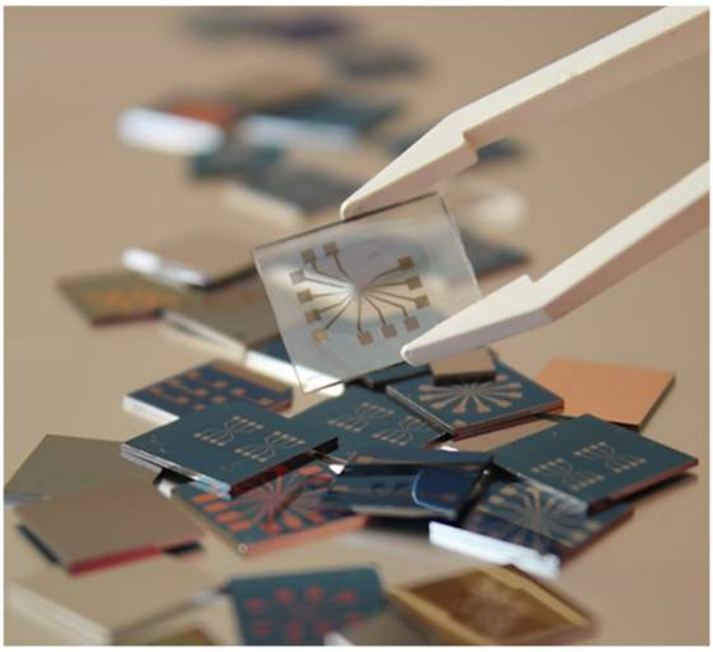
Nanostructuring of Devices for Nanoscience Applications



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CIC
nanoGUNE
nanoscience cooperative research center

Abstract

Having the ability of physically accessing the realm of molecules and atoms, of nanoparticles and nanotubes, leads to constant advances in our fundamental scientific knowledge. Moreover, it sets the ground for developing new technologies in many different fields, such as biomedicine, energy, materials science or food industry. The words "nanoscience" and "nanotechnology" englobe every aspect of all this interdisciplinary research.

Lithographic techniques allow patterning nanostructures and eventually, building devices that constitute our means for exploring the world at the nanometre scale. Fabricating devices for nanoscience applications typically requires patterning nanostructures on surfaces with different characteristics (concerning their chemical, electrical or mechanical properties). Apart from that, the proposed experiments often aim at probing objects with sizes that go beyond the resolution capabilities of the state-of-the-art lithographic techniques.

This thesis is dedicated to the study of electron beam lithography (EBL), its practical limits and complementary strategies for fabricating devices and nanostructures for nanoscience research. The working pace and activities carried out during the development of this thesis have partly been conditioned by the needs of the newly established laboratories of CIC nanoGUNE, principally, regarding the optimisation of a few basic lithographic processes. Setting up new equipment and preparing protocols for the fabrication and characterisation of nanodevices also required special attention.

To begin with, we optimised the lithographic process on a range of substrates with very different conductivity and thicknesses, such as insulating glass and CaF_2, highly doped silicon chips or electron-transparent Si_3N_4 membranes. Each type of substrate had a different response upon exposure to the electron beam and the process had to be accordingly adapted to each case. Apart from that, we explored the resolution capability of our in-house EBL resources (working at moderate beam energies <20 kV), with which we could achieve minimum feature sizes of around 20 nm. Among the obtained results we could highlight plasmonic nanostructures on insulating substrates and electrodes with high aspect ratio nanogaps aimed for molecular electronics. On the other hand, we had the opportunity of experimenting with a high resolution electron beam writer (working at 100 kV) for patterning nanostructures on graphene flakes. This work was carried out in the facilities of the Technical University of Denmark (Kgs. Lyngby, Denmark) during an external stay of 3 months. In this case, the lithographic process was carried out at a whole wafer scale, starting from the preparation of substrates by graphene exfoliation. Nanostructures with a minimum feature size of around 10 nm were patterned onto the graphene flakes employing a high resolution negative resist.

We also studied electromigration as a complementary technique for obtaining devices with elements that were beyond the limits achievable by EBL. The method consisted on patterning metallic wires with nanometric cross-section and breaking them by electrical fatigue under controlled conditions. Electromigration tests were carried out in different metals and alloys, obtaining different types of structures depending on the employed procedure. The devices obtained by this method showed distinct features in their charge transport characteristics. We could thus identify tunnel junctions, metallic nanoconstrictions and single electron transistors.

We then focused our attention on studying palladium-based single electron transistors in more detail, since electromigration proved to be a convenient method for the fabrication of these devices. The obtained devices showed single electron charging effects and occasionally, other features in their charge transport, such as the Kondo resonance. Apart from that, we could observe some peculiar features, which were interpreted as being part of the characteristic resonances of one dimensional nanostructures that had formed in the devices as a result of electromigration.

Finally, we utilised the combination of EBL and electromigration for obtaining devices for spintronic research. More specifically, we intended to achieve a platform for studying pure spin transport in low dimensional systems. Thus, we performed electromigration in lateral spin valves (LSVs) with lithographically pre-defined nanoconstrictions. We proceeded to gradually narrowing the constrictions by electromigration and measuring the spin transport in the devices at different stages. Although time constraints have prevented concluding the project, we have proposed further experiments for achieving our initial objectives. On one hand, we had the prospect of studying the transport of pure spin currents when reaching sizes at which conductance quantisation starts to appear. On the other hand, we wanted to determine if it was possible to observe the tunnelling of pure spin currents through break junctions.

In conclusion, throughout this thesis we achieved the fabrication of devices by EBL on different types of substrates. The obtained minimum feature sizes were approximately at the resolution limit of our EBL equipment. On the other hand, we obtained several types of devices beyond the capabilities of EBL by complementing the fabrication with electromigration. The obtained nanostructures were aimed for research applications in the fields of electronics, spintronics and plasmonics.

Laburpena

Nanozientzia, definizioz, eskala atomikoa eta makroskopikoaren tartean kokatzen diren objektuak (hots, gutxienez dimentsio batean 1 eta 100 nm bitarteko neurria dutenak) eta hauekin lotutako fenomenoak aztertzeaz arduratzen da. Nanozientzian egindako ikerkuntzak biomedikuntza, energia edo materialen zientzia bezalako arlo ezberdin askotan etengabeko aurrerapauso eta berrikuntza garrantzitsuak ematea ahalbidetzen du, bai oinarrizko ezagutzak eskuratuz eta baita teknologia berrien garapena sustatuz ere.

Mundua nano-eskalaren ikuspegi berri honetatik aztertzeak, zeharo txikiak diren objektuak ikusteko (hau da, mikroskopia teknikaren baten bidez irudiak ateratzeko) eta beraiekin elkarrekiteko beharra dakar (adibidez, elektrikoki edo mekanikoki kontaktatuz). Gu geu mundu makroskopikoari lotuta izanik, mundu nanometrikoan objektuak ikusi eta erabili ahal izatea ez da lan bat ere erraza. Zenbait mikroskopia teknikaren garapenak, ekorketazko tunel-mikroskopia, kasu, (ingelesez scanning tunneling microscopy edo STM deritzona), maila atomikorainoko bereizmenez irudiak ateratzeko eta zenbait kasutan, atomoak eurak ere era kontrolatuan mugitzeko aukera eskeintzen du. Orokorrean, ordea, aztergai ditugun objektu nanometriko horiek nanogailuen bidez aztertzeko joera dago. Izan ere, nanogailuek esperimentu ezberdinak egiteko aukera zabalagoak eskeintzen baitituzte eta era berean, izan daitezkeen aplikazioei begira, sistema konplexuagoetan integratzeko aukera eman baidezakete. Nanogailuak, beraz, objektu edo sistema nanometrikoak mundu makroskopikoarekin lotzeko eta atal bi hauen arteko harremana bermatzeko erabili daitezken tresnak direla esan genezake. Nanogailuak egiteari, bai eskala txikian (hau da, ikerkuntza mailan), bai industria mailan, nanofabrikazio deritzo, zeina litografia izeneko prozesu multzo baten bidez burutzen den, batipat. Gai honi helduz, tesi honetan jorratu diren ildorik nagusienak datozkigu harira, hots, litografia bidezko nanogailuen fabrikazioa eta honen muga praktikoak gainditzeko sortutako estrategia osagarriak.

Litografia diseinatutako irudi bat substratu edo euskarri fisiko batetara transferitzeko prozesua da. Prozesu hau teknika ezberdinak erabiliz egin daiteke. Adibide ezagunena fotolitografia da, non diseinaturiko irudia, maskara baten bidez proiektatuz, argiarekiko sentikorra den polimero edo erretxina baten mintz mehe batetara transferitzen den. Erretxina errebelatu ondoren, berau ere maskara edo molde bezala erabiltzen da, estali gabe utzitako guneetan materialea gehituz edo erauziz irudia sustratura transferitzen delarik.

Teknika litografiko ezberdin ugari dauden arren, tesi honetan elektroi-izpien bidezko litografia deritzona erabili dugu nagusiki. Fotolitografiaren antzera funtzionatzen du, baina kasu honetan, ekorketazko mikroskopio elektroniko bat eta elektroiekiko sentikorra den erretxina bat erabiltzen dira irudia substratura transferitzeko. Printzipioz, argiaren ordez

elektroi izpia erabiltzeak, teknikari bereizmen gaitasiun handiagoa ematen dio; hau da, irudi txikiagoak transferitzeko ahalmena du. Gainera, kasu honetan, fotolitografían ez bezala, ez da maskara fisikorik erabiltzen irudia proiektatzeko. Horren ordez, diseinua euskarri elektronikoan soilik gordetzen da eta zehaztasun handiz zuzenduriko elektroi-izpi fokatu baten bidez zuzenean "idazten" da erretxinaren gainazalean.

Teknika litografikoen garapena hein handi batean industria elektronikoaren beharrizanei loturik egon dela esan dezakegu. 1947an lehendabiziko transistorea sortu zenetik gaurdaino, mikroprozesadoreen oinarrizko osagai diren gailu elektroniko hauen elementuek zentimetrotako eskalatik hamarnaka nanometro izaterainoko bilakaera sinesgaitza jasan dute. Eskala aldaketa ikuskarri honen erritmoa "Moore-n legea" deritzonaren arabera gertatu da, egungo bizitzan ezinbesteko bihurtu diren aparailu elektronikoen etengabeko hobekuntza bermatuz. Bilakaera hau litografia prozesuen hobekuntzari eta nanofabrikaziorako teknika berrien garapenari esker gauzatu ahal izan da, besteak beste. Honetaz gain, nanogailuen miniaturizazioari estu lotuta egon den etengabeko berrikuntza ere azpimarratu beharrean gaude. Izan ere, transitoreen adibidera itzuliz, nanogailu hauen muturreko miniaturizazioa ez bailitzateke posible izango erabilitako materialetan eta diseinuan egindako berrikuntzengatik izan ez balitz. Bestalde, gaur egun merkatuan "plastikozko elektronika" edo "elektronika malgua" deritzonaren hainbat adibide (pantaila malguak, gailu elektroniko gardenak, etab.) aurkitu ditzakegu. Honelako erabilpenek nanogailuak era guztietako oinarrietan fabrikatzea eskatzen du (hau da, propietate kimiko, elektriko eta mekaniko zeharo ezberdinak dituztenak), hala nola, beira, oxidoak, plastikoak, etab.

Nanogailuen txikitzearen adibide deigarrienetako bat molekula bakarreko transistoreen kasua dugu. Erabilera komertzialetik urrun izan arren, nanogailu hauek ikerketa mailan oso interesgarriak dira, kargaren garraioaren propietateak materialen mailarik oinarrizkoenean aztertzeko aukera eskeintzen baitute. Molekula isolatuetan oinarrituz nanogailu elektronikoak sortzeko egindako ikerkuntzak lan oparoak eman ditu, bai materialen propietateak molekula mailan sakonki aztertzeko asmoz, bai etorkizuneko sistema nanoelektronikoen eraikuntzari begira. Aviram eta Ratnerrek 1974an proposaturiko gailu molekularren kontzeptua egia bihurtu izana, azken bi hamarkadetan emandako nanogailuen fabrikaziorako teknika aurreratuen garapenari sor zaio.

Aipatzekoa da industria elektronikoaren mugarik gabekoa zirudien nanogailuen txikitze joera honek bere amaiera aurki ezagutu dezakela. Izan ere, zenbait elementuren neurria eskala atomikora hurbiltzen den heinean, egungo transistoreen teknologia (CMOS) ez da erabilgarria izango, fluktuazio kuantikoen agerpena eta bero gisa barreiaturiko energiaren gehitzea direla eta. Honela, elektronikarako ordezko teknologien agerpena bultzatu da azken hamarkadetan. Honen adibideetako bat spintronika dugu, zeinak elektroiaren karga eta spin-a, biak, informazioa prozesatzeko erabiltzea proposatzen duen.

Berez, spintronikaren hastapenak 1988 inguruan kokatzen dira, magnetoerresistentzia erraldoiaren aurkikuntzarekin batera (ingelesezko giant magnetoresistance edo GMR). Izan ere, spintronikaren aplikazio komertzial arrakastatsuena, hau da, disko gogorren irakurgailuetan dagoen teknologia, GMR efektuan oinarritzen da. Aipaturiko aplikazioek polarizatutako karga korronteen garraioan oinarritzen dira, hau da, spin korrontea eta karga korrontea biak batera garraiatzen dira. Spintronikak eskeintzen duen abantaila nagusienetako bat, ordea, kargarik gabeko spin korronte puruak sortzea eta garraiatzea da. Spin korronte puruetan oinarrituriko nanogailu eta zirkuituak erabiltzeak informazioa prozesatzeko abiadura handiagoa eta kontsumituriko energia murriztea ekarriko lituzke. Beraz, etorkizunean spintronikan oinarrituriko konputazioa aurreikusteko arrazoirik ez da falta.

Orokorrean, aipatzekoa da industria elektronikoaren etorkizunerako nanogailuen miniaturizazio eta berrikuntzatik eratorritako ideia guzti hauek, zientziaren beste alorretara etengabe zabalduz doazela. Izan ere, teknika litografikoen hobekuntzak, materiale berrien agerpena eta nanoegiturak fabrikatzeko estrategia berriak nanozientziren beste edozein alorretan aplikagarriak izan daitezke.

Tesi honetan elektroi-izpien bidezko litografia eta elektromigrazioa landu dira nanozientzian aplikagarriak diren nanogailuak lortzeko asmoz. Hemen aurkeztutako lan esperimentalaren erritmoa eta jarduerak, hein batean, CIC nanoGUNEko laborategi ireki-berrien hastapenetan agertutako beharrizanek baldintzatu dituzte. Besteak beste, oinarrizko zenbait litografia prozesuren optimizaziorako premiak, zein nanogailuen fabrikaziorako eta karakterizaziorako instrumentu eta prozeduren prestakuntzak gure arreta berezia eskatu dute.

Laburki, lan honetan aurkitu daitezkeen atalak ondokoak dira:

Lehenik eta behin, nanozientziaren ikuspegitik nogailuek duten garrantzia azpimarratuz, euren fabrikaziorako teknika ezberdinen adibideak eman ditugu, bai litografia bidezkoak eta bai bestelakoak ere. Ondoren, elektroi-izpien bidezko litografian erabilitako teknika esperimentalak sakonki azaldu ditugu, nanogailuen fabrikazio prozesu osoan erabilitako instrumentuak deskribatuz (1. Eta 2. Kapituluak).

Ondoren, elektroi izpi bidezko litografiaz egindako saiakuntzen deskribapen zehatza eman dugu, izandako arazoak eta hauek ekin ahal izateko egindakoa zehaztuz (3. Kapitulua). Gure helburua, gerora proposaturiko esperimentuak eta ikerketak burutzeko nanogailuak edozein substratutan eta erresoluzio altuaz fabrikatu ahal izatea izan da. Horretarako, teknika litografiko honen erabilera sustratu ezberdinetara moldatu dugu, hala nola, isolatzaile elektrikoak diren sustratuak (beira, kaltzio fluoruroa, etab.). Kasu berezi honetan, litografia prozesua burutu ahal izateko, elektroi izpiaz irradiatzerakoan ematen den kargaren metatzea era honek eragindako aldarapen elektrostatikoa ekiditea lortu dugu. Optimizaturiko prozedura jarraituz, plasmonikarako esperimentuetan aplikazioa duten nanoegiturak fabrikatzea lortu dugu kaltzio fluoruro sustratuen gainean, adibidez. Honetaz gain, memoria

aplikazioetarako balio dezaketen nanogailuak eraiki ditugu beira eta hafnio oxidozko substratuen gainean. Orokorrean, kalitate haundiko egiturak lortu ditugu proposaturiko aplikazioetarako.

Substratu isolatzaileen aurkako kasua ere aztertu dugu, hau da, elektroi-izpien bidezko litografia 15 nm-ko lodiera duten eta elektroieko gardenak diren silizio nitrurozko mintzetan egitea lortu dugu. Kasu honetan ere emaitzak onak izan dira, bai lortutako egituren kalitatearekiko eta baita bereizmenarekiko ere (lortutako egiturarik txikiena 20 bat nanometroz banaturiko elektrodo bikoteak izan dira). Honetaz gain, gafenoan oinarrituriko nanogailuen fabrikazioa ere egin dugu, energia altuaz (100 kV-ko azelerazio boltaiaz) lan egiten duen elektroi izpi bat erabiliz, Danimarkako Unibertsitate Teknikoan egindako egonaldi batean. Boltaia altuagoa erabiltzeak nanoegiturak bereizmen handiagoz definitzea ahalbidetzen du. Gure kasuan, 10 nm-ko tamaina minimoa duten egiturak egitea lortu da grafenoaren gainazalean. Kasu honetan, aipatzekoa da litografiaz gain grafeno sustratuen prestaketan (esfoliazio fisikoaren bidez) egindako lana gehitu behar izan dugula. Atal hau amaitzeko, CIC nanoGUNE-ko instalazioetan dagoen litografiarako ekipamenduaren ahalmena probatu nahi izan dugu. Hau da, energia ertaineko (gehienez 20 kV-ko azelerazio boltaia daukan) elektroi izpi bat erabiliz lortu dezakegun bereizmena zein den zehaztu dugu substratu ezberdinen gainean. Orokorrean, lortu diren tamainarik txikienak 20 nm inguruko nanokonstrikzio metalikoak eta 20 nm-ko distantzia minimora kokaturiko elektrodo bikoteak izan dira. Aipatzekoa da lortutako tamaina minimo hauek gure ekipamenduaren bereizmen teorikoaren mugan bertan kokatzen direla; beraz, emaitza hauek prozesu litografikoa behar bezala egiten dugula frogatzen dute.

Litografia bidezko nanogailuen miniaturizaziorako nanoGUNE-n dugun ahalmena frogatu ostean, litografiazkoak ez diren teknikak frogatzeari ekin diogu (4. Kapitulua). Gure helburua elektroi-izpien litografia bidez (bereizmen muga dela eta) lortu ezinezkoak diren egiturak fabrikatzea izan da. Izan ere, nanoeskalan gertatzen diren fenomenoak ikertzeko diseinaturiko esperimentuek sarritan 10 nm baino gutxiagoko neurria duten objektuak, hala nola, nanopartikulak edo molekulak, kontaktatzeko beharrizana sortzen dute. Gaur egun ez dago beharrizan hauek zuzenean asebetetzeko adinako ahalmena duen teknika litografikorik.

Konkretuki, elektromigrazioa deritzon teknika erabili dugu, zeina korronte elektrikoaren bidez sekzio nanometrikodun egiturak (nanohariak, kasu) eraldatzean oinarritzen den. Aplikaturiko korronte elektrikoaren dentsitatea nahiko altua bada (~10^{12} A/m^2 ingurukoa) hari metalikoaren barnean materia mugimendu edo ioien "migrazioa" ematen da. Migrazio honek azkenean hariaren apurketa eragiten du, nanometro gutxitako tamaina duen haustura bat lortu daitekeelarik. Fenomeno hau molekula bakarreko transistoreak egiteko erabili izan da, nanometro bat baino gutxiagoko banaketa tartea duten nanoelektrodoak fabrikatuz eta hauekin molekula isolatuak elektrikoki kontaktatuz. Elektromigrazioa fabrikazio teknika moduan erabili ahal izateko era kontrolatuan egiteko ahalmena izan behar dugu, izan ere, lortutako emaitzak zorizkoak dira, hein handi batean. Elektromigrazio prozesua partzialki

kontrolatzeko modu bakarra hari metalikoa apurtzen ari den bitartean bere barnetik igarotzen den korronte elektrikoaren aldaketak etengabe neurtzea eta aplikatutako boltaia honen arabera erregulatzea da. Hau era automatikoan egin ahal izateko programa informatiko bat prestatu dugu eta aldagai ezberdinek prozesuan duten eragina aztertu dugu, ehundaka hari metaliko apurtuz. Teknika hau litografiarekin bateratu dugu, izan ere, 100 nm inguruko zabalera duten nanohari metalikoen prestaketararako. Metal ezberdinez egindako hariak prestatu ditugu, hala nola, paladioa, urrea, platinoa, kobrea, eta nikela. Aleazio magnetiko batzuk ere erabili dira, adibidez permaloia (nikel-burdin aleazioa) eta paladio-nikela. Nanohari hauen elektromigraziorako estrategia ezberdinak erabili dira. Alde batetik, elektromigrazioa era jarraituan egin da, boltaia hazkor bat hariaren bi muturren artean aplikatuz, etenik bage, haria apurtu arte. Bestetik, era mailakatuan ere egin dugu, hau da, elektromigrazio ziklo bat baino gehiago eginez. Honela, haria pixkanaka apurtu da, ziklo bakoitzean boltaia hazkor bat aplikatuz, elektromigrazioaren hasierara iritsi arte eta gero boltaia berriz jeitsiz, hariaren materiala hoztu eta erlaxatzen uzteko. Lortutako emaitzak oso ezberdinak izan dira erabilitako estrategiaren eta metalaren arabera. Lortutako egituren artean, 1-3 nm bitarteko tamaina duten hausturak aipatu daitezke. Era honetako nanogailuetan korronte elektrikoa tunel efektuz igarotzen da haustura nanometrikoan zehar. Aipatutako egitura hauek transistore molekularrak eraikitzeko aproposak dira, molekula bakar bat zein beste objektu nanometriko bat haustura horretan txertatuz. Hariak guztiz apurtu aurretik atomo gutxi batzutako zabalera duten nanokonstrikzioak ere lortu daitezke. Egitura hauek ez dira mekanikoki oso egonkorrak, baina apurketak jasaten dituzten bitartean igarotzen den korrontearen kuantizazioa ikusteko aukera ematen dute. Hau da, kargaren garraio balistikoa izatera igarotzen denean gertatzen diren ezaugarriak antzeman daitezke. Lortutako nanogailuen beste adibide bat elektroi bakarreko transistoreak dira, zeintzuek korrontea era kontrolatuan, elektroiz elektroi, neurtzeko aukera ematen duten.

5. Kapituluan, elektromigrazio bidezko elektroi bakarreko transistoreen fabrikazioa sakonago aztertu dugu. Gehienetan, honelako ezaugarriak dituzten egiturak elektrodo bikote baten bidez konektaturiko puntu kuantiko batean oinarriturik egoten dira. Puntu kuantiko hau, elektromigrazioz sorturiko nanopartikula metaliko bat izan liteke, hariaren hausturaren erdian kokaturik. Puntu kuantikoaren (PK) tamaina txikia dela eta (gure nanogailuetan 10 eta 30 nm bitartekoa dela estimatu dugu) aldarapen elektrostatikoak sortzen dira PK eta nanoelektrodoetako elektroien artean (Coulomb-en blokeoa deritzona sortzen da). Ondorioz, elektroiak banaka igarotzen dira puntu kuantikotik. Era honetako sitemek, egoera esperimental egokietan, metal ezberdinez egindako nanoegituretan elektroien arteko korrelazioak aztertzeko aukera ematen dute. Paladio eta paladio-nikel aleazioa ere erabili ditugu nanogailuon fabrikazioan. Honela, efektu magnetikoak aztertzeko aukera gehitu dugu.

Azkenik, 6. Kapituluan, optimizatiriko litografia eta elektromigrazioa bateratuz spintronikan aplikazioa duten naogailuak fabrikatu ditugu. Konkretuki, elektromigrazioz

sorturiko nanokonstrikzioetan spin korronte puruak igaroarazi ditugu eta konstrikzioa estutu ahala spin korrontea nola aldatzen den aztertu dugu. Proiektu honetan etorkizunerako lan ugari proposatu dugu, bai konstrikzioei dagokienez, baita beste egitura mota batzuetan ere spin korronte puruen garraioa aztertzeko (adibidez, puntu kuantikoak edo apurketa nanometrikoak dituzten nanogailuak).

Oro har, tesi honetan nanozientziarako nanogailuen fabrikaziorako teknikak landu dira. Bertan azaltzen diren jarduera esperimentalak CIC nanoGUNEko laborategietan eta Danimarkako Unibertsitate Teknikoko (DTU) nanoteknologia eta mikroteknologia departamentuan egindako egonaldi batean burutu dira. Bi eratako jarduerak egin ditugu; alde batetik, elektroi-izpien bidezko litografia prozesuen azterketa sakona eta optimizazio lana egin dugu. Horrela, litografiarako gure baliabideen mugak aztertu ditugu, era berean substratu ezberdinen gainean nanogailuen fabrikaziorako prozesuak optimizatuz. Gainera, elektroi-izpien bidezko litografia eta elektromigrazioa bateratuz, teknika litografiko honen bereizmen ahalmena baino haratago dauden nanoegiturak lortu ahal izan ditugu. Azkenik, hasieran optimizaturiko fabrikazio prozesuez baliaturik, nanozientziaren arlo ezberdinetan, hala nola, plasmonikan, nanoelektronikan eta spintronikan aplikazioa duten nanogailuak sortu ditugu.

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Chapter 1

We understand the fabrication of nanodevices as the means to enable nanoscience research, i.e. exploring the world from the perspective of the nanometre scale. In the same way, lithographic techniques embody the tools for building the necessary platforms for realising such studies.

This introductory chapter starts with a brief overview of the evolution and future prospects of device fabrication, within the frame of the development and the needs of the electronic industry. We briefly discuss the trends of miniaturisation and innovation of devices for nanoscience research, as well as the latest advances in lithographic techniques (section 1.1).

Apart from that, we give some examples of complementary strategies employed for circumventing the limitations of the current lithographic techniques and enabling the advanced fabrication of nanodevices (section 1.2).

1 Introduction to nanoscience

The technological revolution that followed the establishment of the foundations of quantum mechanics has not been equalled, so far. The thorough understanding of its laws led to the invention of the transistor, which most agree in pointing out as one of the technological wonders of the modern world. It has had an impressive evolution in roughly half a century, from the scale of centimetres to the latest 14 nm node technologies [1], which will soon be present inside computers, smartphones and all the seemingly essential gadgets of today's life [2, 3]. This has conditioned to a large extent the way we learn, work and entertain ourselves, or in other words, the way we live.

There has been a constant urge for acquiring the necessary basic knowledge to keep up with such pace in the technological development of the semiconductor industry. This has been the driving force and inspiration of new science and eventually, of new technologies, in fields as different as biomedicine, energy, materials science or food industry. These new science and technologies adopt a completely new perspective, previously out of our reach, which consists on exploring the world in the nanometre scale. The word "nanoscience" englobes every aspect of all this fundamental and interdisciplinary research, which is constantly leading to important advances in many different fields.

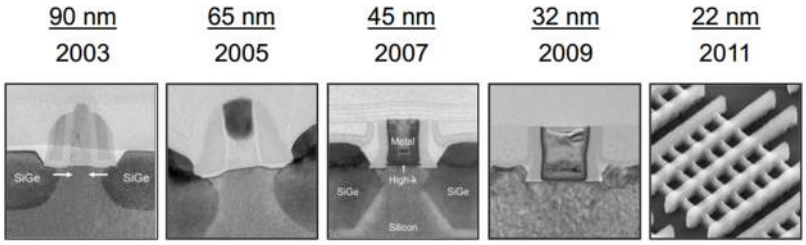
1.1 Devices for exploring the nanoworld

Exploring the world at the nanometre scale involves observing (imaging) and interacting with (for instance, by electrically or mechanically contacting) elements as small as molecules (roughly ~ 1nm in size). Obtaining the means for performing such tasks in the *nanoworld*, being ourselves in the macroscopic world, is not trivial. We thus come up to the subjects that constitute the main body of this thesis: lithography, its practical limits and complementary strategies for fabricating devices for nanoscience research.

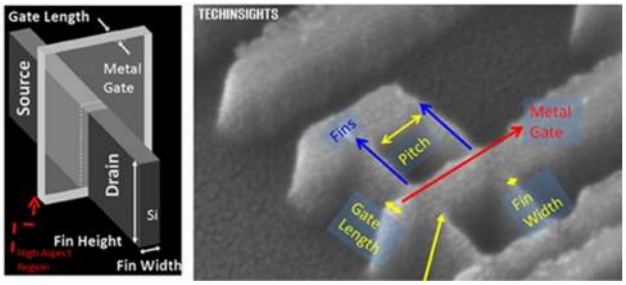
The techniques and strategies for fabricating nanodevices have developed in the slipstream of the electronics industry. Thus, taking the evolution of transistors as a reference, we note that they have kept steadily decreasing in size for nearly six decades, since their invention in 1947. The celebrated "Moore's law" has dictated the shrinkage trend, namely, about a 0.5 scaling every 18 months, resulting in processors with enhanced computing power and speed within the same period [4]. This trend of miniaturisation has also orchestrated the evolution of the resolution capability and throughput of lithographic techniques, which constitute the means for the fabrication of devices and nanostructures for nanoscience research.

Downscaling devices does no longer mean doing a simple decrease in size. Instead, it requires continued innovations in materials and structures, as exemplified in Figure 1.1. Apart from the ubiquitous electronic devices, this demand for innovation has been extended to most areas of nanoscience and nanotechnology.

a)



b)



-14 nm (2014)
-Fin width: ~ 8 nm
-Fin height: 35 nm
-Fin pitch: 60nm
-3D gate length: 30 nm
-3D gate width: 80 nm

Figure 1.1. Scaling of transistors over the last decade. a) Images of the cross section of CMOS transistors from the last few generations, belonging to a smaller node size (from 90 to 22 nm) roughly every two years. b) Schematics and image of the architecture of Intel's latest 14 nm FinFET transistors, with a 3D gated channel that juts out of plane. The 14 nm technology has already been published and it is due on shelves at the beginning of 2015 (Taken from www.intel.com) [5].

In the next generations of transistors (namely, 10 nm and 7 nm nodes, due in 2015 and 2017) [6], the size of some of their elements (the thickness of the gate dielectric, for instance) will reach atomic dimensions. At this point, the appearance of unacceptable leakage currents, quantum interference and heat dissipation issues are expected to put an end to the miniaturisation of the current transistor technology (CMOS) [7].

All in all, the future computing technologies demand alternatives at different timescales. On one hand, the lithographic techniques must keep on evolving in order to guarantee further miniaturisation of the current technology in the near future. On the other hand, there is a need of a major conceptual change that would lead to a totally new computing technology at a longer term. Or, alternatively, the current technology could be complemented (instead of being entirely supplanted) by enhancing its performance, for instance, by the incorporation of heterostructures. Most importantly, all these advances in lithography, the emerging materials and the alternative strategies for the fabrication of devices and nanostructures, will continuously be transferred to other areas of nanoscience.

1.1.1 Reaching out for molecular dimensions

The miniaturisation of devices, either by increasing the resolution of lithographic techniques or by employing complementary strategies to circumvent their limits, still constitutes a very active field of research. In this context, we could highlight the achievement of several types of single electron transistors (SET)[8], including single molecule transistors (SMT) [14] and even single atom transistors [9], which address the ultimate level of device miniaturisation.

Molecular devices were already envisioned by Aviram and Ratner in 1974 [10]. Since then, individual molecules have been regarded as potential building blocks for future nanoelectronic systems. Prototype circuits [11] and functional devices based on a single molecule and working as transistors [12, 13, 14], diodes [15, 16], switches [17, 18], and memory devices [19, 20] have already been reported (see Figure 1.2). Apart from these potential applications, SMTs constitute adequate platforms for studying the charge transport properties of materials at their most fundamental level.

Regarding fabrication, we must say that in general, lithographic techniques do not possess the necessary resolution for obtaining such devices. The only valid methods involve

the use of very complex equipment with ultra-high precision manipulators. For instance, the probe of a scanning tunnelling microscope (STM) was employed for the construction of a single atom transistor by moving atoms one by one [9]. In the case of SMTs, it is necessary to combine high resolution techniques, for instance, electron beam lithography, with complementary strategies, such as electromigration. Some of these strategies are explained in section 1.2.2.

1.1.2 New devices for emerging technologies

Coming back to the needs of the electronics industry, alternative systems and materials to either enhance the performance or replace conventional bulk silicon-based technology are being actively searched [6]. The most prominent examples are spintronics and quantum computing.

Spintronics or "spin electronics" proposethe use of both the charge and the spin of electrons for building devices and circuits. The main potential of spintronics is the possibility of eventually building charge-less circuits, uniquely based on spin currents. The advantages of using pure spin currents are a dramatic decrease in power consumption and an enhanced data-processing speed [21,22]. Part of the effort has been directed toward the creation of a pure-spin analogue to the conventional transistor [23,24], inspired in the original idea of Data and Das [25]. From the fabrication point of view, the development of spintronic devices entails performing exhaustive studies on how to obtain adequate interface resistances. Besides, the optimisation of material deposition (grain size, purity, epitaxy, etc.) can also be critical in order to obtain adequately performing devices.

Magnetic random access memories and hard-disc read-heads constitute two very successful technological applications of spintronics, which are based on spin-polarised charge currents. However, the main potential of spintronics resides in the possibility of eventually building charge-less devices and circuits, uniquely based on spin currents. The advantages of using pure spin currents would be a dramatic decrease in power consumption and an enhanced data processing speed [26,27].

Quantum computing represents another interesting alternative to conventional electronics [28]. However, the fundamental building block of quantum computing, namely, the "qubit" (analogue to bit), must face great challenges in terms of fabrication, isolation, manipulation and read-out [29]. Some of the most remarkable advances in this field comprehend the electrical read-out of an isolated nuclear spin in a single molecule transistor configuration [30, 31]. Once more, building and characterising such devices often requires tools with atomic level precision, such as the STM. This makes the mentioned achievements wholly inadequate for mass production. However, they certainly set the

ground both for performing further advances in quantum computing and for doing fundamental studies of charge transport at the atomic scale.

1.1.3 Merging miniaturisation and innovation

We note that the miniaturisation and the creation of innovative technologies are intimately related. For instance, transistors with a single atom or a single molecular magnet as active elements are proposed as physical supports for qubits, the basic units of quantum computing [9, 30].

On the other hand, carbon-based materials are being introduced for acting as either the magnetic or non-magnetic constituents of spintronic devices. Among them we can highlight graphene [32, 33], carbon nanotubes [34] and single molecules, which are two-dimensional, one-dimensional and zero-dimensional nanostructures, respectively. Utilising this elements, molecular spin valves have been built, in which carbon nanotubes serve as a non-magnetic conductive channel for spin transport, while two single molecule magnets act as spin injectors and detectors [35, 36]. These new types of devices are classified into a new branch of spintronics, the so-called molecular spintronics, which is at the same time considered as part of organic spintronics.

Interesting studies have also resulted from merging single electron physics (mainly concerning the charge transport in transistors based on metallic quantum dots, isolated molecules or short fragments of carbon nanotubes) and spintronics [37].

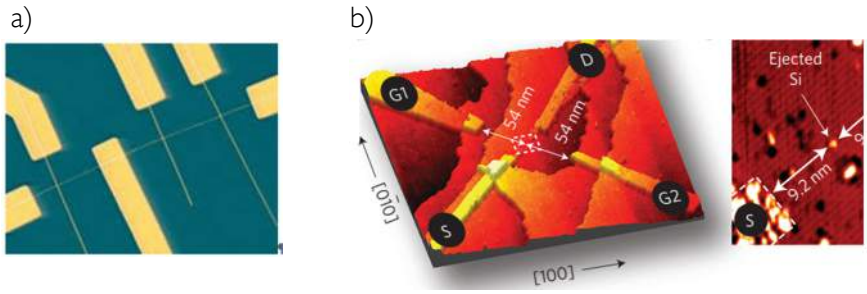


Figure 1.2. Some devices at the ultimate level of miniaturization. a) Prototype circuit constituted by semiconducting nanowires (although conventional EBL is still necessary for electrically addressing the circuit). Taken from [11]. b) Single atom transistor formed by quantum dot and contacts built by placing individual phosphorous dopant atoms in silicon. Taken from [9].

1.2 Nanofabrication for nanoscience

The nanofabrication of devices can be addressed using either the "top down" or the "bottom up" approach, although lately, combining both approaches is also a common practice. The bottom up approach involves using chemical or physical forces operating at the nanoscale to assemble basic units into larger structures [38], in a similar manner as in biological systems. Thus, it comprehends chemical synthesis, growth and self-assembly of materials into nanostructures at different levels of order and complexity. Organic macromolecules, nanotubes and nanoparticles are some typical examples. Nanofabrication by top down approach usually comprises a combination of processes that involve shaping or patterning, depositing materials (metals, oxides, polymers, etc.) and etching (either chemically or physically). The top down approach is based on building small structures from bigger starting materials. It could be compared to carving or sculpting a block of material into the desired shape and size. If the tools utilised are small enough, such as the sharp point of a focused electron beam (down to ~ 2 nm), the size of the chiselled features can be of the same order of magnitude.

Nowadays, the top down approach (mainly photolithography), is the only method used for the mass fabrication of devices. As regards to the fabrication of devices for nanoscience research, more innovative (although, perhaps less mature) lithographic techniques are often employed. Moreover, the fabrication is often complemented with bottom up strategies.

1.2.1 Lithographic techniques for nanoscale patterning

Fabricating devices for research applications can be very challenging. STM and AFM probes have occasionally been used for fabricating devices with elements ranging between 1 nm and atomic size [9,39]. Both examples belong to the category of scanning probe lithography (SPL). It consists on creating structures by directly adding or removing material (even individual atoms) with nanoscopic scanning probes. Apart from a few remarkable examples obtained with different modalities of SPL, direct-writing lithographic techniques are mostly used for the fabrication of novel devices. They utilise a scanning probe consisting of either a focused electron beam or ion beam for patterning (either by etching or by directly depositing materials, depending on the technique). They offer a relatively high resolution (~ 10 nm) and the necessary flexibility for constantly adapting the design of the devices to the experimental requirements, since they are mask-less techniques. Electron beam lithography (EBL) [40], focused ion beam etching (FIB) [41] and focused electron/ion beam induced deposition (FeBID/FIBID) belong to this category [42]. Feature sizes near 10 nm (and occasionally, even smaller) can be achieved with EBL, for instance, depending on the working conditions [43,44]. We could also highlight the helium ion microscope

lithography (HIM), which is among the latest advances in direct-writing techniques (Figure 1.3 a). It uses a focused helium ion beam for etching resists or other materials, reaching minimum feature sizes of around 5 nm [45,46]. It is also worth mentioning the innovative direct-writing techniques that arose from employing STM probes for EBL, (obtaining a resolution of around 5 nm), or the use of TEM for directly sculpting nanostructures [47] (Figure 1.3 b).

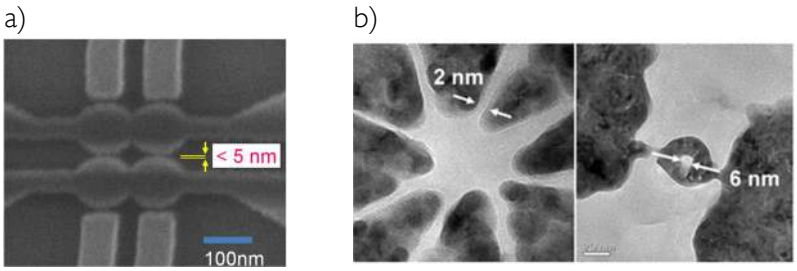


Figure 1.3. Nanostructures obtained by advanced direct-writing techniques. a) Device with a quadruple quantum dot system with a minimum feature size of 5 nm, patterned on a graphene bilayer by means of He-ion-beam milling. Taken from [45]. b) Nanostructures etched on metallic thin films by TEM. Taken from [47].

- Combining lithography with the bottom up approach

We note that the combination of lithography (usually EBL or AFM-based techniques) and the bottom up approach, is acquiring an increasing importance. For instance, the use of directed self-assembly of block copolymers on pre-patterned substrates enhances the throughput of the mentioned techniques [48, 49] (see Figure 1.4*)*. On the other hand, self-assembly is also used for promoting the chemical grafting of individual molecules or nanoparticles onto metallic electrodes, as part of the strategy for building single electron transistors [8]. Electrodes separated by 1 or 2 nm have also been obtained by end-to-end chemical self-assembly of gold nanorods [50]. Another interesting example is the feedback-controlled electrochemical deposition of metal into lithographically defined electrodes. This last technique allows reversibly tuning the inter-electrode gap size down to sub-nanometre distances [51].

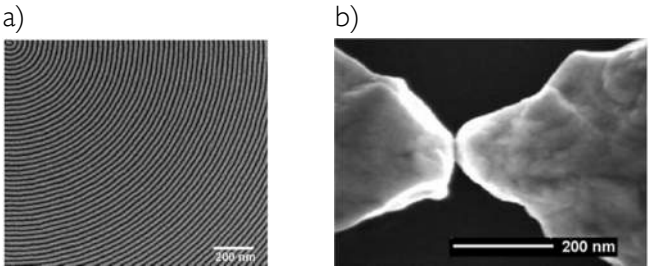


Figure 1.4. Combination of top down and bottom up approaches. a) Example of a resist line array obtained by a directed assembly of a block copolymer onto substrates pre-patterned by EBL. Taken form [49]. b) Nanogap of around 1 nm obtained by electrochemical deposition onto electrodes pre-patterned by EBL. Taken from [51].

- Note on the resolution of lithographic techniques

When the resolution of a given lithographic technique is specified, it typically refers to the smallest feature size that can be directly patterned on a thin resist film, in optimum working conditions. However, we must be aware that the actual resolution depends on the whole lithography process. Therefore, it could be much diminished after transferring the pattern to the substrate by etching or lift off. (More details about the different steps of the lithographic process are given in Chapter 2).

Experiments in nanoscience research often aim at electrically probing objects as small as metal nanoclusters, isolated molecules or single atoms. We thus conclude that none of the conventional lithographic techniques has enough resolution for obtaining devices comparable to such dimensions.

1.2.2 Strategies for contacting nano-objects

Sometimes, the feature sizes conceived for novel devices go beyond the limits of the state-of-the-art lithographic techniques. Several strategies have helped to fill in the gap between the resolution capability of the lithographic resources and the actual requirements for the proposed experiments. As an example of such strategies, we will mention a few, which in combination with EBL allow obtaining inter-electrode distances ranging from tens of nanometres to 1 nm. These methods have been principally used for electrically contacting objects with nanometric dimensions.

- Mechanically controllable break junctions (MCBJ)

This approach consist on mechanically breaking a partially suspended metallic nanowire fabricated (by EBL) on a flexible substrate. The nanowire breaks into two electrodes at a

predefined breaking point. It offers the possibility of fine tuning the electrode spacing with a picometer resolution by bending the substrate in a three-point geometry. A solution of molecules or nanoparticles is previously deposited and self-assembled in the metallic nanowire. The rate of success in trapping and contacting a single nano-object between the electrodes is of around 30%. The main disadvantage of this experimental setup is the low gate coupling [52].

- Electromigrated break junctions (EBJ)

Electromigration consists on causing the breakdown of a metallic nanowire by electrical fatigue, resulting in the formation of closely separated electrodes. It has mostly been used for building SMTs [14] (a detailed description of the process is given in chapter 4). Similarly, the electrical breakdown of carbon nanotubes can also yield nanoelectrodes, which in principle are more compatible with organic molecules [53]. In either case, the formed electrodes can hold a nanoscale object, which can be added before or after creating the nanogap. The inherent randomness of the electromigration process results in low yields (typically <10 %) [14] and devices with very different characteristics, constituting its main disadvantage. However, it allows performing an efficient electrostatic gating, as well as doing electrical and optical experiments simultaneously[54]

- Electrostatic trapping

Combining chemically assembled species with lithographically patterned electrodes constitutes an efficient approach for electrically contacting isolated molecules. For instance, dimer structures consisting of two metallic nanoparticles bound to a linker molecule can be electrostatically trapped between pre-patterned electrodes [55].Nanoparticles are polarized by an applied electric field and are attracted to the gap between the electrodes where the field is maximum [56]. This alternative is more deterministic than trapping a bare molecule in a EBJ or MCBJ, although the nanoparticles can also cause problems. For instance, they can screen the gate potential and their charge transport features can be superposed to those of the molecule, especially at low temperatures.

1.2.3 Patterning nanostructures on functional surfaces

Fabricating devices for nanoscience research demands techniques with flexibility and versatility, apart from high resolution. Research applications typically require patterning nanostructures on surfaces with different characteristics (chemically, electrically or mechanically speaking), which condition the strategies and techniques that can be used.

The fabrication of actual devices implies adapting the details of the lithographic process to each practical case. For instance, in the case of EBL, there are several side effects that can

happen when exposing a material to an electron beam. Heating and electrostatic charging effects are the most common among them. These effects are even more pronounced when patterning on an insulating material, either organic or inorganic. Patterning on flexible materials can also serve as an example of the challenges that the use of novel substrates in many fields of research can suppose.

Different strategies have been proposed for enabling patterning on any type of substrate. One of the most common examples is the use of conductive coatings for performing EBL on electrical insulators [57].

1.3 Concerning this thesis

This thesis focuses in the fabrication of devices and nanostructures for nanoscience research by electron beam lithography and complementary techniques.

The work presented in this manuscript was situated in the context of setting up a new nanofabrication laboratory. This meant carrying out the optimisation of basic lithographic processes, performing tests for patterning on different types of surfaces and exploring the possibilities of complementing our lithographic resources with alternative nanofabrication techniques.

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Chapter 2

In this chapter we explain the experimental techniques and methods we employed in the development of this thesis. It is mostly devoted to the description of the electron beam lithography (EBL) process, which was the principal technique utilised for nanofabrication. It was necessary optimising a few basic lithographic processes at the beginning of our experimental work, since our nanofabrication laboratories in CIC nanoGUNE were newly established and this lithographic technique was new for most of us.

The multiple steps of the EBL process are explained in different sections (2.1.1 to 2.1.5), describing the equipment utilised in each step. We pay especial attention to the detailed description of the electron beam writer and the exposure process (sections 2.1.2 and 2.1.3). The rest of the equipment used in the nanofabrication of devices is briefly explained.

The equipment and methods used in the characterisation of the fabricated devices are briefly described in section 2.3.

2. Experimental techniques and methods

2.1. Nanofabrication by electron beam lithography

Lithography is a process that allows transferring a pattern to a substrate. In the case of direct write electron beam lithography (EBL), this is done by a focused electron beam and a coating of electron-sensitive polymer, commonly known as resist. The resists are chemically modified by the energy they receive from the electrons. Hence, the pattern is literally written on the resist coating as the electron beam scans its surface. The patterned resist is then employed as a stencil mask for transferring the desired features to the substrate by additive (material deposition) or subtractive (etching) processes.

The EBL process consists of several steps (see Figure 2.1); coating of a substrate with an electron-sensitive material (resist), irradiation or "exposure" of the resist with an electron beam, developing of the written pattern and pattern transfer between the resist mask and the substrate.

In this section we explain a standard procedure for EBL step by step. However, we had to introduce variations in some cases, depending on the substrate or the application. More specific details will be given in the corresponding sections of the following chapters.

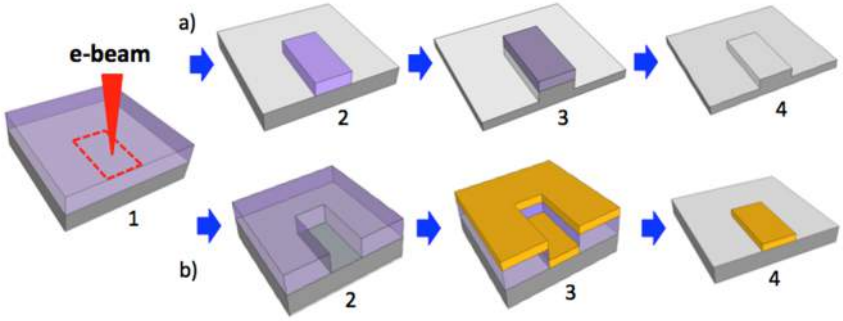


Figure 2.1. Sketches depicting the typical sequence of an EBL process. Sequence a) represents a subtractive patterning process with the following steps: 1) exposure of the substrate coated with resist, 2) pattern transfer to the resist after developing, 3) etching and 4) stripping of the resist. Sequence b) corresponds to an additive patterning and goes as follows: 1) exposure, 2) developing, 3) material deposition and 4) lift off.

2.1.1. General procedure for substrate preparation

Substrate dicing and cleaning

The archetypal support for electronic devices is a thin slice of single-crystal silicon, commonly known as wafer, which is commercialised with different sizes, doping levels and coatings.

The lithography facilities at nanoGUNE are prepared for processing whole wafers of up to a 4 inch diameter. However, we commonly work with substrate fragments of smaller size, known as chips, which are obtained by cutting the wafers with a dicing saw. We generally employ 10 mm x 10 mm square chips because they fit properly the holders for electrical measurements.

We have employed different substrates for the work presented in this thesis, as shown in Table 2.1.

Table 2.1. List of substrates employed for EBL in this thesis.

Substrate	Description
Pyrex (borosilicate glass) (4'' wafer)	-1 mm thickness; cut into 10 x 10 mm chips.
Calcium fluoride (CaF_2)	- 0.5 mm thickness; Purchased as 10 x 10 mm chips.
Silicon (4'' wafer)	-0.5 mm thickness; cut into 10 x 10 mm chips. -p-doped; with thermally grown silicon oxide (SiOx) dielectric coating of 150 nm thickness.
Graphene flakes on silicon (4'' wafer)	-0.5 mm thickness and 4'' diameter (used as whole wafer). -p-doped; thermal oxide (SiOx) dielectric coating of 90 nm or 300 nm thickness.
Silicon nitride (Si_3N_4) (suspended membranes on 3 mm diameter chips)	-Suspended Si_3N_4 membranes of 15 nm, 30 nm and 50 nm thickness, supported on 0.5 mm thick Si chip (3 mm in diameter) with 200 nm thick Si_3N_4 coating.

Cutting the wafers leads to the appearance of silicon debris, which must be removed before coating the chips with resist. Our general procedure for substrate cleaning consisted on 5 minutes of ultrasonic agitation while immersed in acetone, followed by another 5 minutes of ultrasounds in isopropyl alcohol (IPA). Afterwards, the chips were dried with a nitrogen gun and baked for around 1 minute in a hot plate at 190ºC for dehydration.

Resist processing

The e-beam resists can be either organic or inorganic and they are classified into two main groups, depending on the effect of electron beam exposure: positive resists and negative resists. In the case of positive resists the polymer chain is fragmented in the irradiated areas and the shorter polymer fragments are removed upon developing. The contrary happens with negative resists, where the cross-linking of molecules in the exposed areas creates an insoluble network that remains after developing.

The most important properties of a resist are its sensitivity and contrast, which mainly determine its resolution capability [1].

- The sensitivity of a positive (negative) resist is higher when the scission (cross-linking) of its constituting molecules occurs at a lower exposure dose. The term "dose" in EBL refers to the amount of electrons per unit area that the resist receives.
- The contrast defines how the resist is affected by the spatial distribution of the energy during exposure. When the contrast is higher, the resist limiting with the exposed areas is less affected by the scattered electrons, resulting in a steep and sharp edge profile.

There are resist processing strategies that can vary the profile of the transferred pattern. For example, a double layer of resist is commonly used to create an undercut profile, as it can be seen in the next schematic picture (Figure 2.2). We made use of this strategy by placing a sensitive resist as bottom layer and a less sensitive resist as top layer. Thus, after exposure and developing, the bottom resist is further eroded. An undercut profile favours a shadow masking effect when depositing metal on top of the resist, facilitating the lift off (removal of the resist by solvents). It generally gives better defined edges in the transferred pattern, especially when combined with a directional metal deposition technique, such as electron beam evaporation.

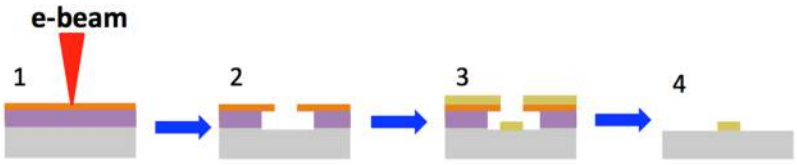


Figure 2.2. Double layer resist processing. 1) Exposure of the double layer of resist (the resist with highest sensitivity is placed at the bottom). 2) Formation of an undercut profile after developing. 3) The shadow masking effect during metal deposition is enhanced by the overhanging resist layer. 4) Lift off is favoured by the discontinuity created in the deposited metal layer.

In this thesis we have mainly worked with one of the most widely used positive resists, namely, poly(methyl methacrylate) or PMMA. On the other hand, we have also employed an inorganic negative resist, namely, hydrogen silsesquioxane (HSQ). Table 2.1 shows the characteristics of the products we used.

PMMA has an excellent resolution capability (around 10 nm) [2] due to its combination of low sensitivity and high contrast. PMMA is an organic polymer that is commercialised in solution for EBL applications, presenting diverse dilutions and molecular weights (MW). The former determines the thickness of the coated resist layer, while the latter affects the sensitivity. A lower MW yields a higher sensitivity, because the polymer chains are shorter and less scission (and consequently, a lower exposure dose) is needed to render them soluble.

HSQ is a high resolution (~ 6 nm) negative resist. It results in a robust three dimensional network with a similar composition of silica upon cross-linking. Its main drawback is the dependence of its performance on film thickness, humidity and aging processes.

Table 2.2. Relation of the employed resists and the purpose for which they were selected. Note that MW (at the top of the second column) stands for molecular weight.

Resist	MW and Dilution	Purpose
25 PMMA A15	-25 kDa -15% in anisol	-Bottom layer for obtaining an enhanced undercut profile at high (100 kV) acceleration voltage.
996 PMMA (MIBK)	-996 kDa -2% in methyl isobuthyl ketone	-Top layer for obtaining an enhanced undercut profile at high (100 kV) acceleration voltage. Using MIBK as casting solvent avoids intermixing with the bottom layer when working at a whole wafer scale.
495 PMMA A2	-495 kDa -2% in anisol	-Bottom layer for an undercut profile at moderate (10-20 kV) acceleration voltages.
950 PMMA A2	-950 kDa -2% in anisol	-Top layer for an undercut profile at moderate (10-20 kV) acceleration voltages. -Single layer for high resolution patterning at moderate (10-20 kV) acceleration voltages.
XR-1541 002 (HSQ resist)	-2% in methyl isobuthyl ketone	-Single layer for high resolution patterning at high (100 kV) acceleration voltage.

The typical procedure for resist deposition is spin coating. It consists on drop casting an amount of solution in the centre of the substrates and spreading it by using a centrifugal force. In our case, the substrate was held by vacuum and rotated in a spin coater. The rotation speed (in the order of 1000 rpm) was selected depending on the viscosity of the solution and the desired film thickness. Afterwards, the casting solvent was evaporated by a baking step in a hot-plate. The general procedure for substrate preparation is summarised in Table 2.3.

Table 2.3. General procedure for substrate preparation. This table summarises the general procedure employed in our laboratory (mainly for obtaining Si chips coated with PMMA). Note that in the case of multi-layer resist systems steps 3 and 4 must be repeated for each layer applied on the same substrate. Different procedures and additional steps were needed in some cases. Specific details are given in the corresponding sections.

Step	Process	Description
1	Dicing	-Cutting a whole wafer into 10 mm x 10 mm chips.
2	Cleaning	-5 minutes of ultrasounds in acetone. -5 minutes of ultrasounds in IPA. -Drying with N_2 gun and baking at 190ºC for 1 minute.
3	Spin coating	-1 minute at 4000 rpm.
4	Baking	-1 minute at 195ºC in a hotplate.

2.1.2. Description of an EBL system

This lithographic technique evolved from the scanning electron microscope (SEM). Physically, the EBL system elements are those of the SEM: an electron source, an electron-optical system and the sample-holder stage. For EBL an electronic interface is attached to the SEM, to provide control over the deflection and interruption of the beam [3]. On the other hand, the stage is controlled by a laser-interferometric positioning system. It can perform high precision movements that allow scanning the whole substrate.

Operation principle

Electrons are emitted from the source (in our case, a thermal field-emission filament). A set of focusing electromagnetic lenses force the beam to converge during its trajectory along the column and a final objective lens focuses the crossover of the beam onto the substrate surface. The resultant beam is scanned over the substrate surface by magnetic deflectors. Another deflector is used to blank the beam and interrupt the exposure when necessary. Besides, there are additional elements for correcting astigmatism, composed of a set of poles that create a local tuneable magnetic field and shift the beam into its optimum cylindrical symmetry. There are also detectors for backscattered and low energy secondary electrons, which allow SEM imaging of the sample surface [9,10]. Ultra high vacuum is necessary inside the SEM column (below 10^{-9} Torr) while the sample chamber is maintained at around 10^{-5} Torr.

A sketch of the electron-optical control system is shown in Figure 2.3. The resultant beam is very fine in diameter (around 2 to 4 nm, depending on the working conditions) and round shaped. It has a bell-shaped distribution of the current density (so-called Gaussian beam).

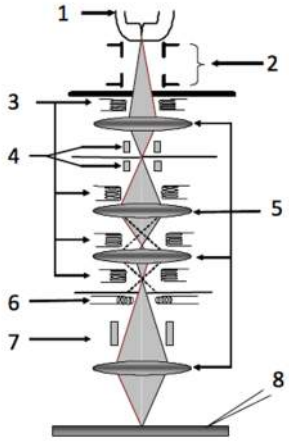


Figure 2.3. Schematic drawing of the inside of an electron beam column. It comprehends the following elements: 1) electron source, 2) accelerator, 3) beam axis alignment coils, 4) blanking electrode, 5) electromagnetic lenses,

6) astigmatism corrector, 7) electrostatic deflector, 8) sample surface. It gives a cross-sectional view of the electron-optical system inside the column, including a representation of the electron beam as it passes through the different electron-optical components.

Three different instruments were used; on one hand, a *Raith 150-Two* and a *e-line plus* from Raith GmbH (both of similar characteristics) located in CIC Nanogune and on the other hand, a *JBX-9500FSZ* from JEOL Ltd. (called JEOL 9500 from now on) at the facilities of the Technical University of Denmark. A few technical specifications of these instruments are listed below:

Table 2.4. Main characteristics of the EBL equipment utilised

Item	Raith 150-Two / e-Line Plus	JEOL 9500
Acceleration V	100 V to 30 kV in 10 V steps.	100 kV
Beam current range	5 pA to 20 nA	50 pA to 100 nA
Beam diameter	2 to 4 nm	4 nm
Aperture size	7.5, 10, 20, 30, 60, and 120 μm	60, 100, 200 and 330 μm
Scanning speed	0.125 Hz to 20 MHz	100 MHz

Aberrations

An electromagnetic beam system with minimum aberration is necessary to have a small effective beam size. The imperfections in fabrication and assembling of the column are responsible for astigmatism. As a consequence, there is a distortion of the captured image (as well as of the image to be patterned) caused by a deviation of the beam section shape from circular (ideal) to elliptic. A system of four poles surrounding the optical axis corrects this aberration by adjusting the balance of the electrical signal of the poles. The astigmatism must be corrected each time the working conditions (acceleration voltage, aperture size or working distance) are changed. The general procedure for adjusting the column conditions consists on imaging a spot or a particle in the substrate surface and adjusting the focus, astigmatism and aperture alignment iteratively.

2.1.3. Exposure; direct writing of the pattern on the resist

Exposure parameters

The writing is carried out in a vectorial mode, which means that a beam with gaussian profile is scanned in a straight line, filling the areas to be exposed. The spot diameter and

space between spots (step size) must be relatively small compared to the minimum feature size to be written.

The exposure dose (that is, the amount of charge per unit area that the resist receives) is adjusted by determining the time that the beam remains in each area (dwell time). This is calculated by the formulas shown in Table 2.5, depending on the beam current and step size selected for the exposure. The lower limit for the dwell time is set by the maximum scanning speed achievable by the instrument.

Table 2.5. Expressions for dose calculation. The exposure time or writing time is determined by formulas that relate the delivered dose, minimum step size and dwell time in each spot. The base dose and step size (S) are fixed and the beam current (I_{BEAM}) is measured, leaving the dwell time (T_{DWELL}) as the only unknown variable.

Feature type	Expression
Area	Dose = (T_{DWELL} x I_{BEAM})/Step^2 (μC/cm^2)
Line	Dose = (T_{DWELL} x I_{BEAM})/Step (μC/cm)
Dot	Dose = T_{DWELL} x I_{BEAM} (μC)

The following table shows the typical values of the exposure parameters we used for writing different feature sizes on PMMA.

Table 2.6. Example of exposure parameters at different working conditions. Typical values of the settings used for writing relatively small features on PMMA (below tens of microns), compared to those for writing bigger features (above hundreds of microns). The settings also vary depending on the beam current at which the equipment is able to work. In this case, the exposure parameters correspond to the Raith 150-Two or e-Line Plus lithography equipment. The value given for the beam current is approximate, since it can fluctuate depending on the state of the filament.

Item	Small features	Big features
Beam current range	20 pA	3 nA
Write field size	100 μm	1000 μm
Area dose (base dose)	100 μC/cm^2	100 μC/cm^2
Step size	3.2 nm	200 nm
Dwell time	512 ns	13.7 us
Beam speed	6.25 mm/s	14.8 mm/s

Scanning the surface

Once the desired exposure parameters are defined, the computer controls how the beam is scanned along the substrate, including beam speed, order and geometry of the

exposed areas. It also controls the coordinated movement of the sample holder stage to cover the whole working area of the design, which contains the complete pattern to be transferred. Each working area is divided into smaller write fields, in which the stage is kept still and the beam is deflected to write the pattern. Building certain feature of a pattern by using more than one write field is called stitching. If the deflection of the beam is not correctly calibrated, stitching errors or mismatching of different parts of the pattern can appear.

Deflection calibration

The operation for the adjustment of the electromagnetic/electrostatic deflections system to the sample coordinates is called *write field alignment*. It can be done by a manual or an automatic procedure, for which it is necessary to focus the beam in a selected mark in the surface. A previously patterned mark or a contamination dot originated with the e-beam itself can be used for this task. The stage moves the selected mark or feature to three different positions and the beam is deflected enough to scan a small area, including the mark. The operator is then presented with the scanned image and must indicate the mark with the cursor, as accurately as possible (in the case of manual alignment). The size of this scanned area must be previously selected by the operator, depending on the accuracy needed during exposure and the size of the write field. This calibration is iterated while decreasing the size of the scanned area and increasing the beam deflection, gradually doing a finer correction. After each iteration the software calculates new correction factors for the angles and the x and y coordinates. This procedure is repeated until no decrease in correction factors is observed.

Alignment of several lithographic layers

When a pattern is written in more than one lithography step, we need to perform certain alignments in order to match or *overlay* the different parts of the design. This is done manually, with an operation called *three-point adjustment*. It consists on matching references or alignment marks in 3 different sites of the physical pattern with the ones corresponding in the designed pattern. This mark detection allows aligning the deflection system and the stage to the pre-existing pattern. This procedure is also valid for patterning electrical contacts in objects deposited on the substrate, such as carbon nanotubes or graphene flakes.

Apart from the three-point adjustment, there are additional fine alignments that can be performed within individual write fields semi-automatically or automatically, following a similar procedure as for the write field alignment. They are used for aligning sub-micron sized elements (see Figure 2.4).

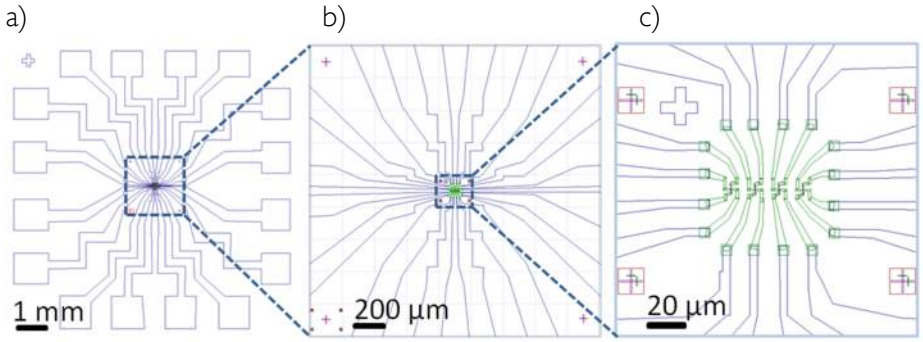


Figure 2.4. Example of a pattern with several lithography layers.. a) A view of the macroscopic contacts of the device; b) global alignment marks (crosses at the four corners of the design) used for 3 point adjustment; c) Detail of the microscopic part that connects the nanodevices to the contact pads. The write field alignment marks can be seen as four small crosses around the central pattern.

Electron scattering and proximity effect

The energy transfer via collisions with the electrons that eventually leads to the exposure of the resist is known as scattering.

As they penetrate the resist, many electrons experience small-angle *forward scattering*, which tends to broaden the initial beam diameter. When electrons reach the substrate, they occasionally undergo large-angle *backscattering* events, and return to the resist at places far from the spot where the primary beam entered. As the primary electrons slow down, much of their energy is dissipated in the form of lower energy secondary electrons. These slower electrons with energies from 2 to 50 eV are the principal responsible for the exposure.

The net effect is that the exposure to the electron beam does not only affect the directly irradiated area, but also the surrounding areas. This is known as *proximity effect*, and its main consequence is the loss of resolution.

The main factors that affect the proximity effect are the following:

- Incident electron beam energy. Primary electrons with a higher energy have smaller scattering angles, causing less broadening of the beam. On the other hand, they penetrate deeper into the substrate, so that there is additional backscattering [3]. However, at high energies the back scattering area gets deeper and wider. This results in a larger spatial distribution of the backscattered electrons and a lower effective dose absorbed by the area surrounding the patterned features (Figure 2.5). As a consequence, exposing at high beam energies causes less feature broadening, due to a lower proximity effect.

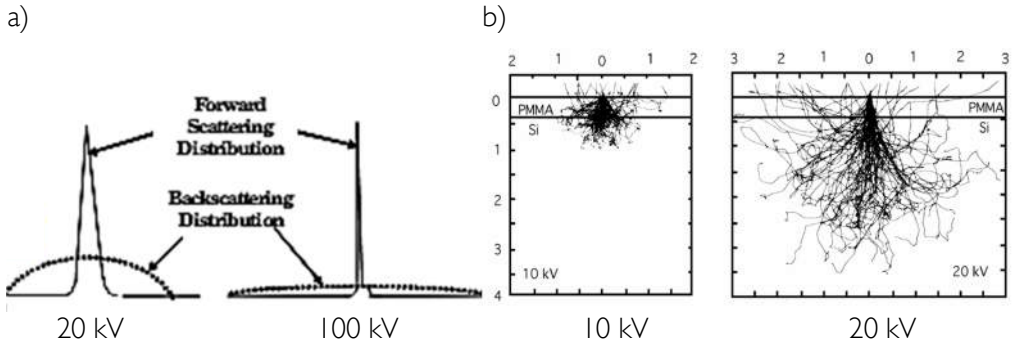


Figure 2.5. Representation of the spatial distribution of the electron scattering. a) Sketches qualitatively showing the distribution of forward scattered and backscattered electrons when exposing the resist with moderate beam energies (20 keV) and high beam energies (100 kV). Higher beam energies result in a large spatial distribution of the backscattered electrons, giving as a result a lower proximity effect near the exposed areas. b) Montecarlo simulation of electron scattering in PMMA on a silicon substrate at 10 kV and 20kV beam energies. Forward scattering is more present in the former, while backscattering plays a more important role in the latter. Taken form [4].

- Nature of the substrate. More electrons will scatter back in high density substrate materials. Elements with high atomic number (Z) lead to more backscattering.
- Resist thickness. Forward scattering results in a broadening of the beam as it goes deeper into the resist. Thus, thin layers of resist are preferred for higher resolution. Similarly, thin membrane substrates lower the amount of backscattering.

The most usual method for proximity effect correction is adjusting the dose (see Figure 2.6). It can be done manually, altering the exposure dose in different parts of the pattern or computationally for complicated pattern designs.

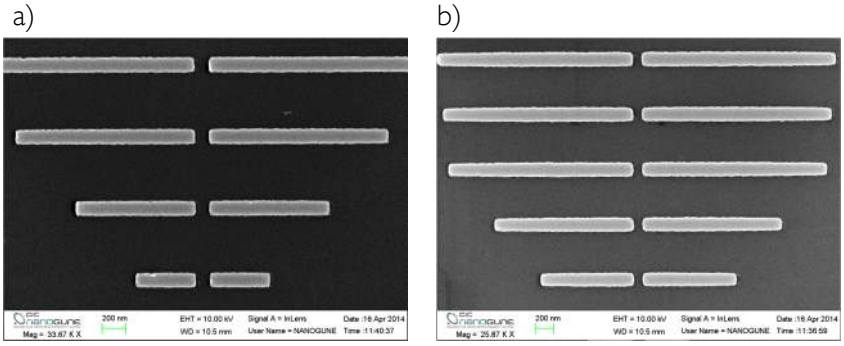


Figure 2.6. SEM image of structures patterned at 10 kV. Structures patterned a) with doses of 250 μC/cm^2 and b) 400 μC/cm^2. The structures become bigger (the gaps in between get smaller) and the edges acquire a round shape at higher doses, as the proximity effect increases.

Another common strategy is mask biasing, which consists on modifying the size (and sometimes, the shape) of the design in order to obtain the desired dimensions. There are computational methods for proximity effect correction that allow calculating the specific dose needed in each spot of the design by means of an algorithm. This last option implies doing previous exposure tests for finding out the proximity effect parameters. These methods require performing an exhaustive study of the absorbed dose for calculating the empirical coefficients to be used in the algorithm. Afterwards, the designed features are fractured in small fragments and a different dose if assigned to each fragment, in order to compensate the proximity effect caused by adjacent features. In the case of simple and regular patterns, manually modifying the dose and size of the design results in a more convenient and less time consuming strategy.

Table 2.7. Summary: general procedure for electron beam exposure

Step	Description
-Loading -Alignment to the stage coordinates	-Loading, definition of working distance and write field size. -Definition of a global coordinate system; adjustment of the origin and angle.
-Adjustment and calibration of the beam	-Focusing, correction of the astigmatism and the aperture alignment at the selected aperture size and acceleration voltage. -Correction of the deflection system. Write field alignment.
-Overlaying -Fine alignment	-Definition of a local coordinate system; 3 point adjustment (for matching to previous lithography layers). -Fine alignments in a single write field (for accurately matching small features to previous lithography layers).
-Setting exposure parameters and exposure properties	-Measurement of the beam current (in a faraday cup). -Setting the exposure parameters. Defining the base dose and step size for area, line and dot features. Calculation of the corresponding dwell time and beam speed. -Setting up a positionlist (list of items to be written) and edition of the exposure properties for each item (layer, exposure dose, working area and writing position).
-Exposure	-Calculation of the total exposure time (simulation). -Exposure.

2.1.4. Developing

The developer is a selective solvent that is able to dissolve only the exposed areas in positive resists or, on the contrary, the areas that have not been exposed in the case of negative resists.

A mixture of methyl isobuthyl ketone diluted with isopropanol MIBK/IPA 1:3 is employed for developing PMMA. Instead, an aqueous solution of tetramethyl ammonium hydroxide (TMAH) is used for developing HSQ.

The developer temperature affects the solubility of the polymers [5]. This means that the developing time must be optimized each time the temperature is changed. We performed the lithography in the cleanroom (which provides a constant temperature of 21°C). The patterned structures are typically developed by immersion in the corresponding solvent. Afterwards, the samples must be immediately rinsed for quenching the developing process and dried, for instance with a N_2 gun.

2.1.5. Pattern transfer; subtractive or additive processes

Once the pattern is developed in the resist layer, there are two principal methods to transfer it to the substrate: etching or metal deposition and lift off [2].

An additive pattern transfer technique comprises at least two steps. First, a thin film of material (a metal, in our case) is deposited on top of the developed resist. Afterwards, the lift off is carried out by immersion in a solvent (with or without ultrasounds), which removes the resist mask and the metal layer on top of it. Thus, the substrate areas that were not previously covered by the resist mask are metalised after the process.

Etching treatments yield a subtractive pattern transfer by eroding the areas that are not protected by the resist layer. Etching can be carried out by chemical or physical methods (wet etching with acids or bases, reactive ion etching, plasma etching, ion milling, etc.). The remaining resist can be stripped off by means of solvents or oxygen plasma treatment (in the case of organic resists).

- Electron-beam evaporation and thermal evaporation

These techniques consist on evaporating a material (in our case, a metal) either by a high voltage electron beam or by thermally heating it inside a vacuum chamber. In the first case, a high-energy electron beam is directed towards metal pellets inside a crucible. The metal eventually gets heated by the e-beam and starts evaporating. In the case of thermal evaporation, a boat containing metal pellets is heated by Joule effect until the material is melted and starts evaporating.

In both evaporation techniques the metal vapour is directed towards the sample and a quartz crystal monitor, which measures the real time rate and the deposited thickness. A shutter is manually closed on the sample when the desired thickness is reached.

The sample holder can be kept still or rotating. The evaporated metal is ejected in a fixed angle and this directionality allows using shadow masking strategies. In this thesis the evaporation was always done perpendicular to the substrate, although some instruments presented difficulties for controlling the exact direction.

There are several instruments for material evaporation at CIC Nanogune. There is a high vacuum evaporator, (*Oerlikon Univex*, operating at $P_{BASE} \sim 10^{-7}$mbar), which has both an electron beam and a thermal evaporation source. On the other hand, there is an ultra-high vacuum (UHV) evaporator for molecular beam epitaxy (*Createc,* operating at $P_{BASE} \sim 10^{-9}$mbar), with an electron beam and several thermal evaporation sources. As an example, Table 2.8 shows the typical operation conditions utilised in an UHV evaporator.

Table 2.8. Operating conditions for metal evaporation in an UHV evaporator. Typical conditions used for electron beam evaporation (EB) and thermal evaporation (TE) of copper, titanium and gold.

Metal	Technique	P_{BASE} (mbar)	$P_{DEPOSITION}$ (mbar)	Rate (Å/s)
Cu	TE	1×10^{-8}	3.4×10^{-8}	2
Ti	EB	3×10^{-9}	1×10^{-8}	0.1
Au	EB	3×10^{-9}	1×10^{-7}	0.2

- Magnetron Sputtering

Magnetron sputtering is another technique used for material deposition. Its principle relies on the production of plasma, usually from argon gas, and the magnetically directed collision of these charged species against a target. The colliding particles pluck atoms and molecules from the surface of the target, which eventually get deposited on the sample and form a film.

This deposition technique is in principle not as directional as electron beam evaporation or thermal evaporation, explained earlier. As a consequence, certain amount of the sputtered metal deposits on areas that were not directly exposed to the source, such as the walls of the resist mask. This can make the lift off more difficult and it can also result in the formation of fringes around the edges of the patterned features, depending on the nature and thickness of the sputtered material (See Figure 2.7).

In this thesis we used a high vacuum *AJA* sputtering system (operating at $P_{BASE} \sim 10^{-8}$ mbar) and a sputtering system inside the*4 Wave* Ar ion Miller (operating at $P_{BASE} \sim 10^{-6}$mbar). Besides, a *Leica* tabletop sputter ($P_{BASE} \sim 10^{-5}$mbar) was used for purposes that did

not require an optimum quality of the deposited metallic film. As an example, the operation conditions for DC sputtering of palladium are shown in Table 2.9.

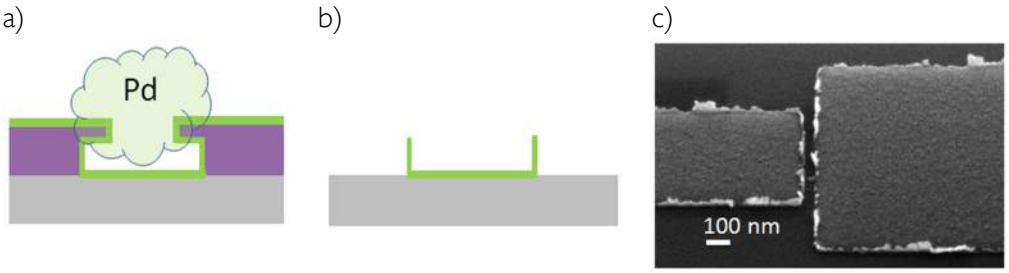


Figure 2.7. Formation of metallic fringes by sputtering. a) Sketch representing the deposition of palladium by sputtering. b) Metal deposited on the resist walls leads to fringes remaining after lift off. c) Example of closely spaced electrodes with a shortcut occasioned by the remaining metallic fringes.

Table 2.9. Operating conditions for metal deposition by magnetron sputtering. Operating conditions typically used for palladium deposition in different sputtering equipment,

Metal	P_{BASE} (mbar)	P_{Ar} (mbar)	Power (W)	Rate (Å/s)
Pd	6×10^{-8}	6×10^{-3}	100	1.8
Pd	3×10^{-6}	3×10^{-3}	250	2.5

- Argon ion milling

This physical etching process consists on bombarding the substrate with a beam of accelerated Ar ions, which literally *mill* or etch the material. The etching process is very anisotropic (it etches exclusively in the incident direction) and thus, the sample is usually rotated (in our case, at 15 rpm) during the process. The etching is not material selective; all the materials are etched, although at different rates, depending on their hardness.

A 4 Wave Ar ion miller used for this process. It was mainly employed for cleaning the interfaces between different lithography layers (employing a short etching time at a perpendicular angle). It was also used for removing the metallic fringes remaining after lift off in some patterned structures (with longer etching times at a grazing incidence angle of 10 degrees from the surface). The sample was rotated at 15 rpm during the process for a more homogeneous result (while keeping constant the incidence angle). The typical operation conditions are shown in Table 2.10.

Table 2.10. Conditions for argon ion milling

P_{BASE} (mbar)	Ar flow (sccm)	Power (W)	Acceleration voltage (V)	Power supply (V)	(mA)	Time (min.)
$\sim 10^{-6}$	15	250	50	300	50	variable

- Plasma cleaning

Oxygen plasma cleaning treatments were performed for promoting the adhesion of the resist on the substrate (for instance, on Si_3N_4 membranes). Occasionally, we also used it for cleaning the fabricated metallic devices.

It relies on the production of oxygen plasma, which reacts with organic species and also with most metals (therefore, it is necessary to check the compatibility with the fabrication process). It is commonly used for stripping off the resist residues remaining from lithography.

Table 2.11. Conditions for oxygen plasma cleaning

P_{BASE} (mbar)	Oxygen flow (sccm)	Power (W)	Time (min.)
1	10	100	variable

2.2. Photolithography

Photolithography transfers a pattern to a photosensitive resist by irradiation of light. Opposite to EBL, which is a maskless technique, photolithography needs a physical mask that contains the pattern and through which the resist is irradiated.

We occasionally used this technique for patterning macroscopic contacts (with sizes ranging from hundreds of microns to millimetres) that would be more time consuming to pattern by EBL. We employed a positive resist and a mask aligner from the company EVG.

The steps of the photolithography process are essentially the same as those explained for EBL in the previous sections (*i.e.* sample preparation, exposure, developing and pattern transfer). We will not comment further details about this technique, since in our case it did not involve the patterning of nanostructures.

2.3. Sample characterisation

In the following sections the methods and instruments used for electrical characterisation are explained in detail. The techniques used for the morphological characterisation of the samples are briefly mentioned.

2.3.1. Electrical characterisation

We basically needed the following elements for the characterisation of the charge transport properties:

- Elements for electrically contacting the samples.
- Equipment for providing the desired experimental conditions.
- An electrical measurement system.
- A system for controlling and coordinating the measurements and the experimental conditions.

The charge transport properties of the fabricated devices were measured at different conditions of temperature, pressure and magnetic field. The characterisation was carried out at a temperature range from 300 K to 1.8 K. The samples were loaded into a *Lakeshore* variable temperature probe station or inside a *Physical Property Measurement System* (PPMS) from Quantum Design Inc. The latter has a liquid helium cryostat that allows achieving a temperature of 1.8 K in the measurement chamber. The PPMS is equipped with a sample rotator and a superconducting magnet, with which we can apply up to ± 9 T at different angles.

We employed either a manual or an automatic switchboard to change the configuration of the contacts and we performed DC measurements at two or four terminal configuration, depending on the experiment. It must be noted that the two probe configuration measures the total contribution of the contacts and cables in series with the nanodevices. Instead, the four probe configuration allows measuring just the signal of the device under test. This last option is recommended when the device resistance is relatively low (roughly, $R < 1\ k\Omega$).

We used either the conductive tips of a probe station or copper wires (manually bonded by cold indium pressing) to connect the fabricated samples to the terminals of the measurement equipment (see Figure 2.8), depending on the required experimental conditions. In general, for four terminal measurements we used either the combination of a Keithley nanovoltmeter (model 2182) and a Keithley AC/DC current source (model 6221), or a Keithley dual-channel source-meter instrument (model 2636A). Instead, we used the

same Keithley 2636A (employing a single channel) or a Keithley sub-femtoamp remote source-meter SMU instrument (model 6430) for two probe measurements.

a) b) c)

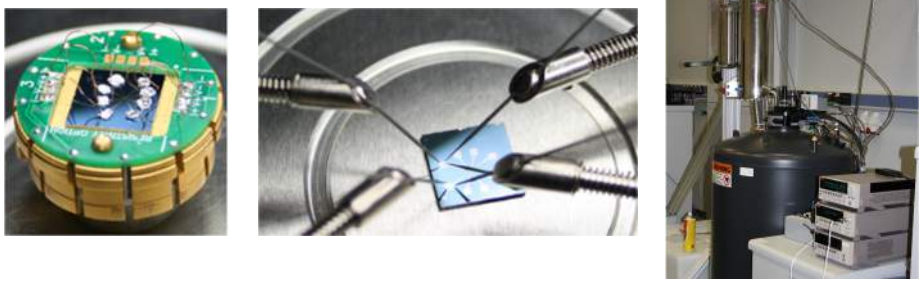
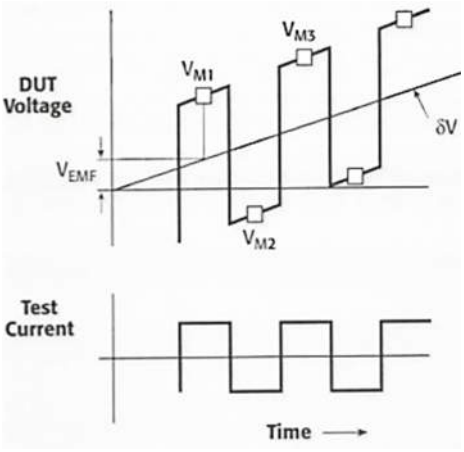


Figure 2.8. Devices contacted for electrical characterisation, a) Device contacted to a sample holder of the PPMS. The macroscopic pads of the device were manually bonded with copper wires by cold indium pressing. b) Device contacted by the tips of a probe station. c) Liquid He cryostat of the PMMS, equipped with a He reliquifier.

Several LabVIEW programs were designed for controlling the electrical measurement systems and the configuration of the cables in the automatic switchboard, as well as the temperature, magnetic field and sample position (rotation angle). We generally applied a voltage and measured the DC current as a function of temperature, the applied magnetic field and on occasions, as a function of the angle. For measurements in lateral spin valves (Chapter 6), we used the so-called *DC reversal* method or *delta mode*, which allowed subtracting the thermal noise from the measurements. It basically consisted on applying a DC current with an alternating polarity and performing several measurements of voltage over a period of time. The voltage drop across the device could then be calculated and decoupled from the offsets caused by thermoelectric effects (see Figure 2.9).

a)



b)

- Measured voltajes:

$$V_{M1} = V_{DUT} + V_{EMF}$$
$$V_{M2} = -V_{DUT} + V_{EMF} + \delta V$$
$$V_{M3} = V_{DUT} + V_{EMF} + 2\delta V$$

- Calculation of V_{DUT}:

$$V_A = (V_{M1} - V_{M2})/2 = V_{DUT} - \delta V/2$$
$$V_B = (V_{M3} - V_{M2})/2 = V_{DUT} + \delta V/2$$
$$(V_A + V_B)/2 = (V_{M1} - 2V_{M2} + V_{M3})/4 = V_{DUT}$$

Figure 2.9. DC reversal (*delta mode*) measurement technique. We assume that the thermal noise has two contributions: a constant offset (V_{EMF} in the figure) and a thermoelectric voltage that changes linearly with time (δV in the figure). The delta mode consists on alternating the polarity of the applied current and performing 3 measurements of the voltage over time (V_{M1}, V_{M2} and V_{M3} in the figure). Using these measurements we can extract the voltage drop across the device under test (V_{DUT}), as shown in the equations in b).Taken from [6].

2.3.2. Scanning electron microscopy (SEM) and optical microscopy

Electron microscope imaging was done at the electron beam lithography facility itself (*Raith 150-Two* and *e-Line Plus* from Raith GmbH). Apart from these instruments a *Quanta FEG 250* Environmental SEM from FEI was used. The elements and working principle of the SEM is that of the EBL, explained before (Figure 2.3).

A *Nikon150LV* optical microscope was used to examine the samples during developing and lift off.

2.3.3. X-ray reflectivity

This characterisation technique was used for determining the thickness of the deposited thin films. A *X' Pert PRO* x-Ray diffractometer from PANalytical was used in this work.

We performed X-ray reflectivity measurements mainly for the calibration of the metal deposition and etching rates. The technique basically consists on irradiating the sample with an X-ray beam at different incident angles and measuring the intensity of the reflected beam with a detector. As a result, we obtain a characteristic intensity profile as a function of

the incident angle. This profile consists of the so-called Kiessig fringes, the periodicity and spacing of which depends on the film thickness (see Figure 2.10).

The film thickness is calculated based on Snell's Law ($\sin\theta_0 = n\ \sin\theta_1$) and Bragg's Law ($n\,\lambda\ = 2d\ \sin\theta_1$) [7, 8].

a) b)

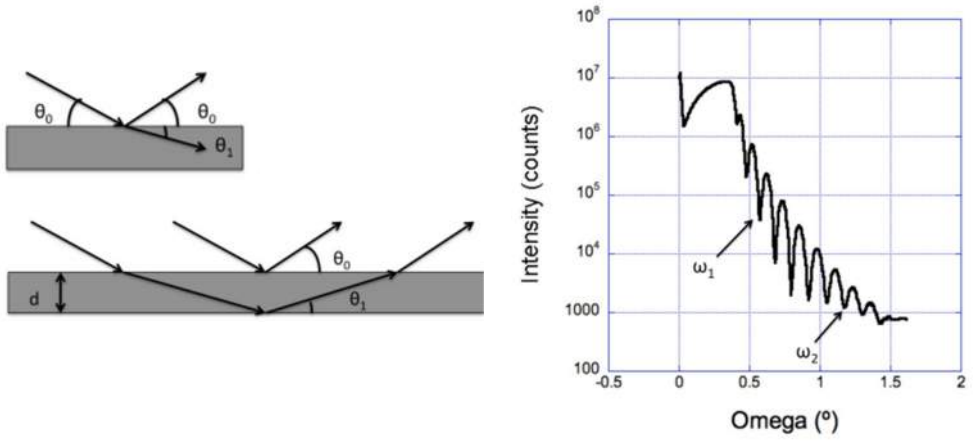


Figure 2.10. a) Schematic representation of Snell's law. The sketch on top represents the incident and reflected x-ray beams, with their corresponding angles. The one below, shows the reflection and penetration of the diffracted beam in a film of thickness "d", and a refraction index "n" (we have used the same notation in the corresponding equation). b) Kiessig fringes resulting from the measurement of the intensity of the reflected beam as a function of the incident angle. The instrument's software uses the incident angles (omega) corresponding to two fringes (for instance, ω_1 and ω_1 pointed with arrows) for calculating the thickness "d".

2.3.4. Atomic force microscopy (AFM)

The surface roughness of the deposited thin films and profiles of the nanostructures were occasionally measured with an AFM from Agilent Technologies.

AFM microscopy roughly consists of scanning a probe with a nanometrically sharp tip along the sample surface. Its basic principle relies in the attraction and repulsion forces acting between the sample and the tip. After scanning a certain area we obtain a 3D image of the surface topography with a resolution of around one nanometre (Figure 2.11).

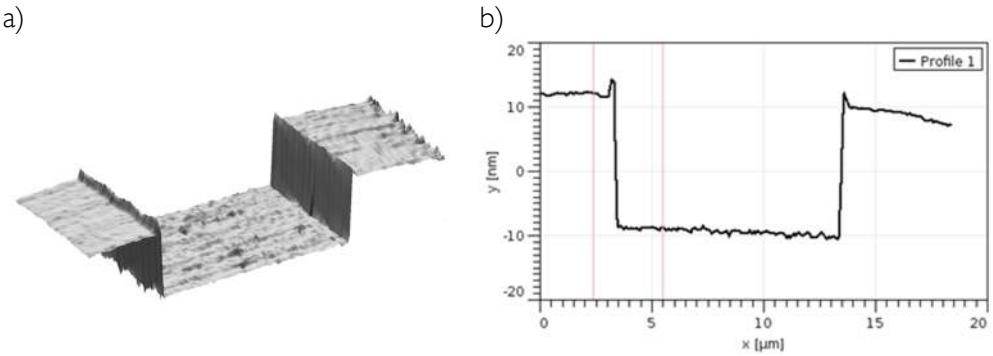


Figure 2.11. a) AFM topography image of a trench etched in SiO_2. b) Profile extracted from the image in a).

2.4. References

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Chapter 3

After describing the basics of electron beam lithography (EBL) in previous chapters (see Chapter 2), we focus on the fabrication of devices and nanostructures by EBL onto a range of different substrates. The fabrication procedure is fully explained in this chapter. Besides, we give an account of the strategies we used either to solve or to circumvent specific issues in each case.

Section 3.1 talks on the optimization of the EBL process on insulating substrates. In section 3.3, we establish a procedure for the fabrication of nanostructures on extremely thin silicon nitride membranes. In section 3.4, we report the patterning of nanostructures on exfoliated graphene flakes with a high resolution e-beam resist. To conclude, in section 3.5 we explore the limits of our in-house lithographic resources, trying to decrease the minimum feature size on different types of substrates.

Some of the devices described here have been developed for projects in collaboration with other research groups. This is the case of nanostructures on CaF_2 and Si_3N_4 substrates, which were fabricated for the Nanooptics Group in CIC nanoGUNE and the devices on exfoliated graphene, which were made in collaboration with the Nanocarbon Group in the Technical University of Denmark.

3. Fabrication of devices by electron beam lithography

Direct-write electron beam lithography (EBL) is one of the best candidates for the fabrication of devices for nanoscience research, due to its versatility and resolution. However, diverse procedures might be needed depending on the conditions in which this technique is going to be used and the properties of the material under study.

This chapter focuses on the search of suitable procedures and working conditions for performing EBL on substrates with very different properties, such as electrical insulators, extremely thin and electron-transparent membranes or graphene flakes.

3.1. EBL on insulating substrates

There are several side effects that can happen when exposing a material to an electron beam. Heating and electrostatic charging effects are the most common among them.

Depending on the nature of the exposed material, some effects are more pronounced than others, affecting the final outcome to a different extent. This is the case of electrical insulators, in which the charge accumulation repels and deflects the electron beam. Thus, electrostatic charging effects can cause serious distortions in the patterned features [1]. The most common strategy for performing EBL on insulating substrates is using a conductive coating for charge dissipation [2].

In the following sections we report the optimisation of the EBL process on glass substrates using an extremely thin gold coating for charge dissipation purposes on top of the resist. Afterwards, we have implemented the process on hafnium oxide (HfO_2) and calcium fluoride (CaF_2) substrates for several research applications.

3.1.1. Substrate preparation

Spin coating with resist

Glass, being a good electrical insulator, was the substrate of our choice for the optimization of the lithographic process. We used Pyrex (borosilicate glass) wafers that were diced into 10 x 10 mm chips.

The substrates were cleaned and coated with a PMMA resist bilayer to create an undercut for an easier lift-off, as explained in Chapter 2 (section 2.1.1.). 495 PMMA A2 and 950 PMMA A2 were used as bottom and on top resist layers, respectively, giving a total thickness of around 100 nm.

Application of a conductive coating

There are different conductive coatings that can be used for charge dissipation during the exposure. Depositing a thin layer of metal on top of the resist is the most common choice. As an alternative, conductive polymers that are water-soluble and can be applied by spin coating are also commercially available.

The conductive coating must meet certain requirements. First, the material itself and the deposition technique must be compatible with the EBL process. For example, sputtering metal on top of some negative resist could lead to partial cross-linking by the exposure to plasma. Second, the thickness of the conductive layer must be adequate for the exposure conditions and the required resolution. Thicker layers increase the scattering of electrons and thus, contribute to the increase of the beam size before it enters the resist. Therefore, working with higher beam energies allows the use of thicker conductive layers, since the electrons can cross it without major changes in their trajectory. Finally, the conductive material should be selectively removed before developing the resist.

We decided to use a thin layer of gold (Au) for charge dissipation although other metals (for instance chromium or aluminium) could have been used. We had to consider that our EBL system worked at moderate beam energies (with a maximum of 30 kV acceleration voltage), compared to other equipment that work at 100 kV, for instance. Therefore, we decided to try thinner gold layers instead of the ones usually employed (which can be above 15 nm thick), in order to minimize electron scattering within this layer. As a first test, 3 nm of gold (nominal thickness) were sputtered on several samples in a tabletop Leica sputter, using the deposition conditions shown in Table 3.1. We also prepared some control samples without any conductive coating, with the purpose of evaluating how the charging effects affected the lithography.

Table 3.1. Conditions for gold deposition by magnetron sputtering

Technique	P_{BASE} (mbar)	P_{Ar} (mbar)	Rate (Å/s)	Thickness (nm)
Sputtering	10^{-5}	1.2×10^{-3}	0.8	variable

The surface of the metallised resist showed a granular appearance when imaged with the electron beam at high magnification (Figure 3.1). This was already expected, since gold tends to grow in the shape of islands and the deposited film was very thin

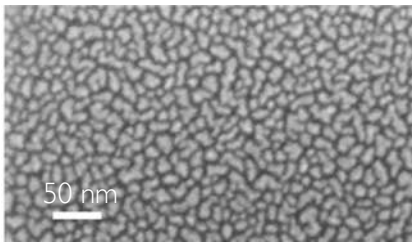

Figure 3.1. Scanning electron microscopy (SEM) image the resist surface after depositing 3 nm of sputtered gold. Sputtered gold islands cover the resist surface, giving a rough appearance.

3.1.2. Electron-beam exposure

The designed pattern consisted of a set of several electrodes with inter-electrode gaps ranging from 200 to 500 nm. This central feature, which fitted a 100 µm × 100 µm write field together with the alignment marks, comprised the first lithography layer. Each electrode was then connected through contacts that gradually grew in size and ended up into square shaped contact pads of 800 µm × 800 µm size. This was the second and last layer of lithography, which was divided into 1000 µm × 1000 µm write fields. Patterning the second layer by photolithography would be more efficient, given its feature-size. However, sometimes it is necessary to fabricate small batches of devices with custom designs, for

which buying a new photolithography mask would be rather costly. For this reason, we wanted to test if the charge dissipation method was valid for exposing large areas with higher currents.

The first lithographic layer was exposed using a small beam size (~ 2nm), since the biggest feature size was less than 5 microns across. The second layer was written with a higher current, in order to decrease exposure time. We were not concerned about the resolution in the second case, since the size of the features was ranging from tens to hundreds of microns. The utilised column conditions are shown in Table 3.1.

The detailed procedure for performing the write field alignment and the settings for the exposure parameters are explained in chapter 2 (section 2.1.3).

Table 3.2. Column conditions used for writing on Pyrex. Two different acceleration voltages were tested for patterning the nanoelectrodes. The value of the beam current is approximate, since it can fluctuate depending on the state of the filament.

Lithography Layer	Acceleration voltage (kV)	Aperture size (μm)	Beam current (pA)	Write field size (μm)
-Nanoelectrodes	10	10	~20	100
-Contacts	10	120	~3000	1000

First approach: writing directly on insulating samples

This first approach was intended for examining the behaviour of the insulating substrate under the electron beam. We wanted to know how the charging effects affected the exposure procedure and also to evaluate their impact on the final outcome of the EBL process. The test was only done for the first lithography layer, working at 10 kV acceleration voltage and 10 μm aperture.

To begin with, focusing the electron beam on the surface was almost impossible, due to the charging effects. The brightness of the imaged surface area started to increase until the detector saturated and we could not obtain any image. As expected, the write-field alignment could not be done in these conditions. Even though it was not the correct procedure, a test pattern was written using the write-field alignment parameters set for a silicon substrate.

We did a dose test by writing an array of electrodes with different doses (from 50 $\mu C/cm^2$ to 250 $\mu C/cm^2$). Some images of the pattern resulting after metal deposition and lift-off can be seen in Figure 3.2. Some features were clearly distorted and there were metallic streaks running across the pattern. Our interpretation was the following: the electric charge piled up around the exposed areas during the writing. When the charge accumulation grew enough, sudden dissipations occurred and the electrons exposed the

resist on their way to ground. Developing the resist gave way to streaks that filled up with metal during the deposition, resulting in short circuits (see panels a and b in Figure 3.2). On the other hand, the deflection of the electron beam by electrostatic repulsion of the accumulated charge gave way to the distortion and mismatching of features (Figure 3.2-c). This test confirmed that it was indeed impossible using the standard EBL procedure on insulating substrates.

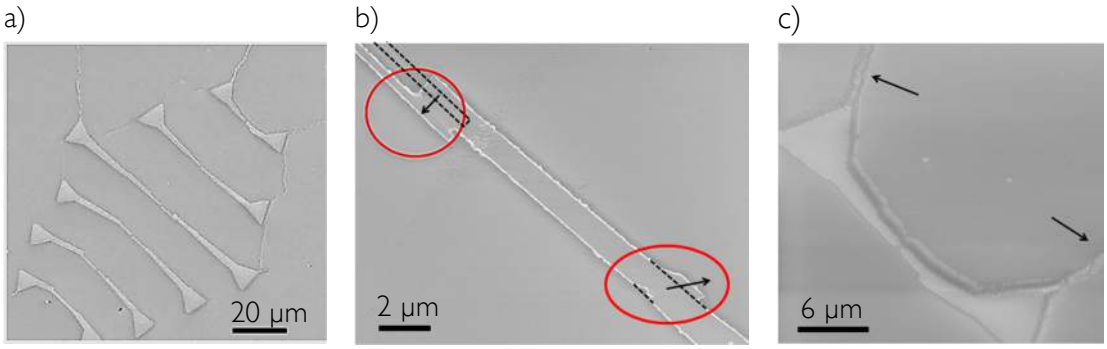

Figure 3.2. SEM image of test electrodes directly patterned on glass. a) A set of electrodes with streaks, resulting from sudden dissipation of the accumulated charge. b) Feature mismatching (circled) due to the deflection of the e-beam, which is caused by the electrostatic repulsion of the accumulated charge. c) Detail of a structure surrounded by streaks.

Second approach: writing through a conductive coating

Avoiding charge accumulation on the substrate was essential for performing the electron beam lithography. Therefore, we deposited a thin layer of gold of around 3 nm thickness on top of the resist for charge dissipation purposes (as explained in section 3.1.1.)

We repeated the electron beam exposure using the same column conditions (table 1) and similar writing parameters as when writing without the charge dissipation layer. The conductive coating allowed focusing the electron beam and performing the write field alignment properly. However, the substrate still got charged when the same spot was imaged for more than a few seconds. The accumulated charge originated artefacts due to the repulsion of the electron beam. For instance, the objects imaged in the screen appeared to be moving and getting brighter, if imaged for a long time.

3.1.3. Developing

As a general rule, the conductive coating used for charge dissipation must be selectively removed before developing the resist. However, some samples were directly developed (following the procedure explained in chapter 2, section 2.1.4) skipping the gold etching step, in order to serve as a control experiment.

We used a commercial gold etchant composed of potassium iodide and iodine in aqueous solution (KI/I_2 or KI_3 from Sigma-Aldrich) for removing the conductive coating. The chips were immersed for two seconds in the etchant solution and immediately rinsed in a beaker with around 500 ml of deionised water (DIW) for 1 minute. The reactions that take place with the gold etchant can be written as follows:

$$I^- + I_2 \rightarrow I_3^-$$

$$3\,Au + 3I^- \rightarrow 3Au\,I_2^-$$

Afterwards, the chips were once more rinsed with clean DIW for 10 seconds and finally, immersed in isopropyl alcohol (IPA) for another 10 seconds. The purpose was to make sure that the etchant was properly rinsed.

Once the thin metallic coating was eliminated, the resist was developed in MIBK/IPA 1:3 as usual. The developing seemed to have worked normally in all the samples (either with or without performing the gold etching step), as seen in Figure 3.3.

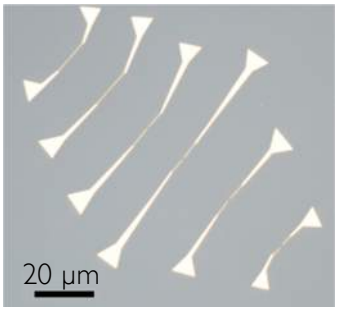

Figure 3.3. Optical microscopy image of developed sample. The image shows the developed pattern of a set of electrodes patterned on the resist layer. The image belongs to a sample in which the developing was done without previously performing the gold etching step.

3.1.4. Metal deposition and lift-off

The pattern was transferred to the substrates by metal evaporation and lift-off. 15 nm of cobalt were deposited by electron beam evaporation (see Table 3.3).

Table 3.3. Conditions for cobalt deposition by electron beam evaporation on glass.

Metal	P_{BASE} (mbar)	$P_{DEPOSITION}$ (mbar)	Rate (Å/s)	Thickness (nm)
Co	~2 x10^{-6}	~3 x10^{-6}	0.5	15

The lift-off was carried out by immersion in acetone for approximately two hours, after which practically all the metalised resist was removed. The samples were then transferred

into a petri dish with clean acetone and inspected with the optical microscope while still immersed in the solvent. The application of short cycles (~3 seconds) of ultrasounds and subsequent inspection under the optical microscope was repeated until the lift-off was complete, (as far as the optical microscope would allow seeing). Afterwards, the samples were rinsed with IPA and dried with a nitrogen gun. The time of immersion in acetone and ultrasounds needed could vary slightly from one sample to another. It must be noted that it is important to keep the sample immersed in the solvent until the lift-off is complete. If the remaining metal flakes are left to dry on the surface, they tend to adhere irreversibly to the substrate.

3.1.5. Solving edge roughness problems

SEM imaging of the fabricated structures showed that the edges were extremely rough in those samples in which the charge dissipation layer was not removed before developing the resist (Figure 3.4). On the contrary, the samples in which the conductive coating was removed before developing gave well defined electrodes with smooth edges.

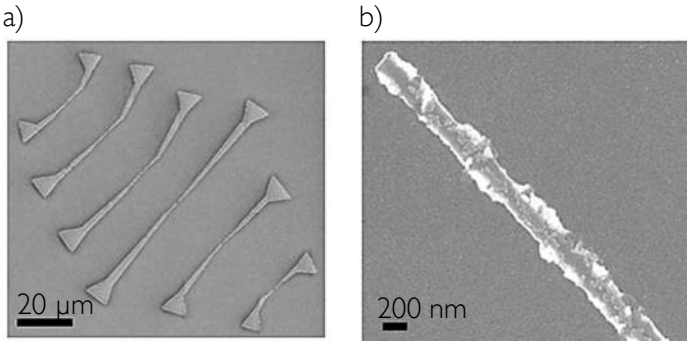

Figure 3.4. SEM image of the obtained electrodes after lift-off. The charge dissipation layer was not removed before developing and metal deposition. A close look at the electrode tips revealed a severe edge roughness and cracks all over the electrode surface.

We repeated exactly the same fabrication procedure, imaging with the SEM after each step for tracing back the appearance of the edge roughness. Once more, the resist was exposed and developed skipping the gold etching step. SEM imaging after developing showed that the pattern had not been properly transferred to the resist. In addition, it seemed that the thin gold layer still remained (at least partially) on top of the developed pattern.

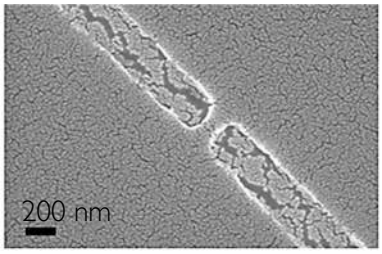

Figure 3.5. SEM image of a developed sample. The charge dissipation layer was not removed before developing. It seemed that the resist had been developed under the thin gold layer. The cracks in the gold surface might indicate that the thin conductive layer had partially collapsed onto the developed pattern.

We performed a control experiment by repeating the whole lithography process on a highly doped silicon chip. Same as in the insulating samples, we sputtered a 3 nm gold coating on top of the resist. This allowed us to compare our previous observations with a substrate that in principle should not present problems for charge dissipation. As expected, we observed that the pattern transfer was not adequate when using the 3 nm gold coating (Figure 3.6-a). For the sake of comparison we carried out the same patterning process in another silicon chip without the 3 nm gold coating. In this last case the obtained nanostructures presented well defined edges (Figure 3.6-b).

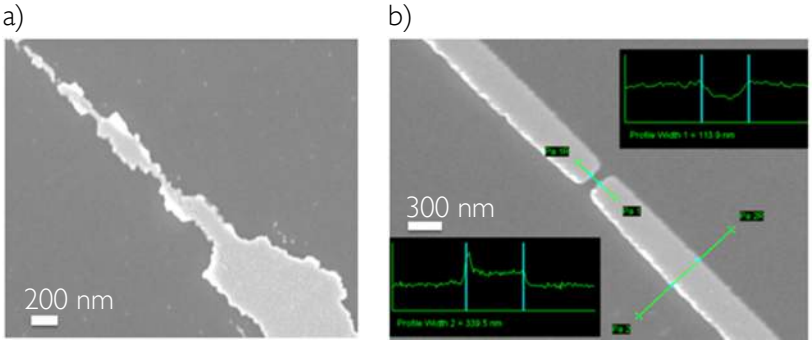

Figure 3.6. SEM image of a pattern on doped silicon substrate. a) The structures that were patterned on silicon employing a charge dissipation gold coating of 3 nm thickness presented a severe edge roughness. b) In parallel, the same structures were patterned on a silicon chip without the charge dissipation coating, giving as a result well defined edges.

The origin of the edge roughness was clear; the developing was hindered by the 3 nm of sputtered gold employed for charge dissipation purposes. Since this conductive coating was absolutely necessary for writing with the e-beam, a compromise had to be reached. There were two possibilities: either removing the conductive coating before developing (which worked well, as we observed in samples fabricated in parallel to this batch), or trying a thinner gold layer for charge dissipation. Trying the second possibility seemed attractive,

since it could shorten the EBL process by one step and save consumables (such as the gold etchant or the sputtered gold itself). We therefore repeated the process using a thinner gold layer (about 1.3 nm in thickness) and performed the developing without removing this thin conductive coating. The results confirmed that indeed, if the employed charge dissipation layer was thin enough, removing it was not strictly necessary for obtaining nicely defined features and smooth edges after lift-off (Figure 3.7).

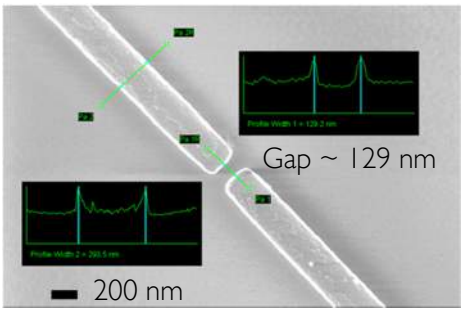

Figure 3.7. SEM image of electrodes on glass substrate. Employing 1.3 nm of sputtered gold for charge dissipation allowed obtaining well-defined structures, even if the charge dissipation layer was not removed before developing the resist. Interelectrode gaps of around 129 nm (200 nm in the design) were achieved by exposing with a dose of 250 μC/cm^2.

An exposure dose of 250 μC/cm^2 was found to be adequate in order to reduce the size of the interelectrode gaps by taking advantage of the proximity effect. However, we must note that it resulted in overexposed features, which might be unacceptable depending on the application of the devices.

3.1.6. Writing macroscopic electrodes with a high beam current

As mentioned before, the second lithography step consisted of bigger features (up to hundreds of microns in size). Thus, a bigger write-field size and a higher current were selected for the exposure (see Table 3.2 in section 3.1.2).

The procedure we followed for patterning macroscopic pads was similar to the one corresponding to nanometric features. We are going to describe the corresponding steps very briefly, referring to previous sections (3.1.1 to 3.1.5) for further details.

The substrates were prepared for exposure by sputtering a conductive coating (~1.3 nm thick gold) on top of the PMMA resist bilayer. The second lithography step was aligned with the first one utilising the three-point adjustment method, by means of alignment marks (consisting of cross-shaped metallised features) that were pre-patterned in the first lithography step, together with the small electrodes. These marks were also used for performing the write-field alignment (see details about the procedure in Chapter 2).

We found that the gold coating of 1.3 nm thickness was not enough to prevent the substrate from charging when working at a 3 nA current. Focusing the beam and doing the write-field alignment with these working conditions presented serious difficulties due to the charging effects. As a result, the alignment of the two lithography layers could be very time consuming and yet, not as accurate as it should be. The easiest solution would be simply employing a thicker gold layer for charge dissipation when writing with a high current.

Another alternative to achieve the fabrication of devices employing very different beam currents for the different lithography steps could be simply changing the order in which these steps were written. The design with large contact pads could be written in a first lithography step, together with the alignment marks. The charging effects were still present but they were not critical, since we did not need to align the pattern to any previous lithography step. Besides, we compensated the possible stitching errors in the macroscopic contacts by adapting the designed pattern. Writing the macroscopic pattern with a dose of 125 $\mu C/cm^2$ took around 1hour (see exposure parameters set in Chapter 2). The resist was directly developed, skipping the gold etching step, since we previously saw that it was possible doing so when using a charge dissipation layer of 1.3 nm.

The second lithography step could then be written using a low beam current. There were two possible paths, depending if the same or different materials were used for both lithography steps. If the same metal was required for both lithography steps, the pattern of the small electrodes could be directly aligned with the developed pattern of the big contact pads .The developed alignment marks could be easily found, since they presented an excellent contrast with respect to the rest of the surface. The alignment and exposure could be properly done, following the standard procedure. Afterwards, we could etch the conductive coating and develop the resist, as described before. Note that the first lithography layer was twice developed, although the overdeveloping did not make any practical difference in the quality of the macroscopic contacts. Following this procedure, the metal deposition and lift-off were done for the entire pattern (comprising both the macroscopic contacts and the nanodevice) at the same time, thus saving time and consumables.

However, if a different material was used for each lithography step, the metal deposition and lift-off had to be done independently (which implied repeating the whole lithography process from 3.1.1 to 3.1.4). In this case, the alignment of the second step was done on the metallised alignment marks.

3.1.7. Summary: General protocol for EBL on insulating substrates

We followed the most common strategy for performing EBL on insulating substrates, namely, using a conductive coating for charge dissipation. We optimized the lithography

process on glass substrates using an extremely thin gold coating (of 1.3 nm) on top of the resist. We found that the gold coating did not need to be etched before developing (which is usually necessary) if its thickness was low enough. Testing the same process with gold coatings of slightly different thicknesses (initially 3 nm, and afterwards, 1.3 nm) demonstrated that the results were extremely sensitive to this parameter.

The process was optimized for working at an acceleration voltage of 10 kV and a beam current of around 20 pA. It could occasionally be used for writing with higher currents (we were able to write with 3 nA). However, performing the deflection calibration or an accurate alignment with pre-existing lithographic steps became difficult tasks, due to the more pronounced charging effects at higher beam currents.

The general fabrication protocol for a two-step lithography process employing different beam currents for macroscopic and nanometric features is summarized in the following table.

Table 3.4. General procedure proposed for EBL on insulating substrates. Note that the steps 6 to 9 can be by-passed if the same metal is going to be used in both lithography layers.

STEP		PROCEDURE
1)	Substrate preparation	Cleaning of 10 X 10 mm glass chips with the application of ultrasounds in acetone and IPA (5 minutes in each solvent). Drying with nitrogen gun.
2)	Resist processing	Application of a 495 PMMA A2 /950 PMMA A2 resist bilayer. Spin coating at 4000 rpm for 60 seconds, followed by 1 minute baking in a hot plate at 195°C (repeat for each layer).
3)	Conductive coating	Deposition of 1.3 nm gold by sputtering at 1.5×10^{-2} mbar Ar pressure and a rate of 0.8 Å/s
4)	e-beam exposure	Exposure of macroscopic contacts with a current of ~3 nA (corresponding to an aperture of 120 µm and an acceleration voltage of 10kV). Utilised dose: 125 µAs/cm^2.
5)	Developing	Immersion in MIBK/IPA 1:3 for 1 minute, followed by an IPA rinse for ~10 seconds and drying with a nitrogen gun.
6)	Metal deposition	Deposition of 15 nm cobalt by electron beam evaporation at 2×10^{-6} base pressure and a rate of 0.5 Å/s.
7)	Lift-off	Immersion in acetone for around 1 hour followed by 3-second cycles of ultrasounds (stopping for inspection with optical microscope) until all the metal was removed. Immersion in IPA for rinsing. Drying with a nitrogen gun.
8)	Resist processing	Repeat step 2
9)	Conductive coating	Repeat step 3
10)	e-beam exposure	Exposure of nanometric features with a current of ~20 pA (corresponding to an aperture of 10 µm and an acceleration voltage of 10 kV). Utilised dose: 250 µAs/cm^2.
11)	Au etching	Immersion in Au etchant (KI/I_2) for 2 seconds, followed by immersion in 500 ml DIW for 1 minute. Thoroughly rinse with clean DIW and IPA (10 seconds in each). Drying

	(optional)	with a nitrogen gun.
12)	Developing	Immersion in MIBK/IPA 1:3 for 1 minute, followed by an IPA rinse for 10 seconds and drying with a nitrogen gun.
13)	Metal deposition	Repeat step 6
14)	Lift-off	Repeat step 7

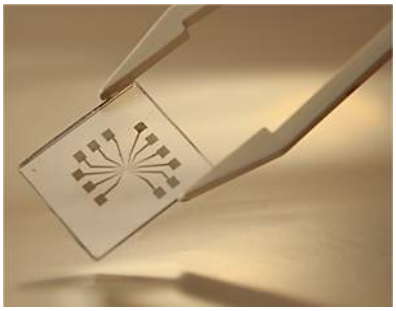

Figure 3.8. Photograph of a device patterned on a glass substrate.

3.2. Applications for the optimized EBL protocol on insulating substrates

After optimising the EBL process on glass substrates, we implemented the proposed protocol on hafnium oxide (HfO_2) and calcium fluoride (CaF_2) substrates for two specific applications.

3.2.1. Nanogap electrodes on hafnium oxide.

As a first example of application, we carried out the fabrication of devices on hafnium oxide-coated glass substrates. Transition metal oxides, such as hafnium oxide (HfO_2), are among the candidate materials for developing new solid-state memory devices. Moreover, HfO_2 was the choice of the semiconductor industry for the gate oxides in sub-45 nm nodes [3, 4]. HfO_2 thin films are being extensively studied and hence, our interest of using it as a substrate for EBL.

Other members of our group carried out the preparation of the oxide thin films in a parallel project. HfO_2 films with a total thickness of approximately 20 nm were deposited on glass substrates by atomic layer deposition (ALD) [5]. The design consisted on lateral electrode pairs, with a separation in the range of 100 nm. The lithography process is not explained in detail because it was done as reported in section 3.1. However, some

additional optimization was done to match the requirements for the final application of the devices.

HfO_2 memory devices belong to the category of resistive memory. Their principle to store information is based on transitions between two distinct resistance states by applying suitable voltages. Based on this principle, the device could be improved for its application as a memory cell by decreasing the inter-electrode gap size. Smaller gaps would allow applying a lower voltage for changing the resistance state of the oxide between them [6]. Thus, we reduced the range of inter-electrode distances in the designed pattern and we followed the EBL procedure proposed in Table 3.4. The biggest features of the device, namely the contact pads, were patterned by photolithography beforehand and the nanometric pattern was overlayed on top. We obtained inter-electrode gaps of around 40 to 100 nm, setting nominal distances between 110 nm and 180 nm in the designed pattern. We selected a dose of 250 $\mu As/cm^2$, which resulted in overexposed features but allowed obtaining a smaller gap size (around 40 nm) by taking advantage of the proximity effect. The patterned features had smooth and regular edges, as it can be seen in Figure 3.9.

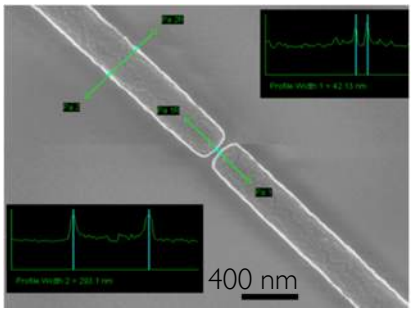

Figure 3.9. SEM image of an electrode pair on HfO_2-coated glass substrate with a gap size of around 40 nm.

3.2.2. Plasmonic nanostructures on calcium fluoride

We report the fabrication of optical antennas on calcium fluoride (CaF_2) substrates as a second practical example of the optimised EBL process. These nanostructures were fabricated for the Nanooptics Group in CIC nanoGUNE, under the direction of Prof. Rainer Hillenbrand. All the experiments and structures shown in this section were conceived and designed by members of the Nanooptics Group. Our work consisted on adapting the nominal distances and sizes of the designed structures in order to make them achievable by EBL and carrying out the complete lithography process. The fabricated structures were aimed for scanning near-field optical microscopy experiments (SNOM), which required robust structures (consisting of 40 nm thick gold) and the smallest possible inter-feature distance for obtaining optimal results.

An optical antenna is a device designed to transmit and receive electromagnetic waves in the range of visible or infrared light. This devices have the ability to focus light into dimensions that are orders of magnitude below the limit of conventional lenses. Thus, they show potential applications in single molecule spectroscopy and imaging, for instance [7].

A metallic rod can be considered as the most simple dipole antenna. Matching visible or infrared wavelengths requires patterning metallic rods with its longest dimension in the range of microns. In previous works we successfully fabricated such nanostructures on silicon substrates by conventional electron beam lithography [8]. However, it was expected that these antennas would show much more intense signals onto calcium fluoride (CaF_2) insulating substrates. This happens because CaF_2 has a lower dielectric constant than silicon, which means having a weaker damping of the optical fields into it [9]. Our contribution to this work was related to the fabrication of optical antennas and other structures with application in plasmonics on CaF_2 insulating substrates.

We fabricated the devices following the protocol summarised in Table 3.4, except for the metal deposition step. The patterned structures consisted of 40 nm of thermally evaporated gold, on top of a 1.5 to 3 nm adhesion layer of electron beam evaporated titanium. The evaporations were carried out in a Univex Oerlikon evaporator (see Table 3.5).

Table 3.5. Conditions for the evaporation of titanium and gold by electron beam evaporation and thermal evaporation, respectively.

Technique	P_{BASE} (mbar)	$P_{EVAPORATION}$ (mbar)	Rate (Å/s)	Thickness (nm)
Ti	$\sim 10^{-6}$	$\sim 10^{-4}$	0.3	1.2
Au	$\sim 10^{-6}$	$\sim 10^{-4}$	0.6	40

The exposure dose on CaF_2 was slightly different from the one on glass/HfO_2, partly due to the different nature of the substrate. On the other hand, having more densely packed features in the design contributed to a higher proximity effect. We did not apply computational methods for proximity effect correction. Instead of that, we performed a dose test and adapted the design and the exposure dose for approaching the desired results, which is a common practice when the designed structures consist of simple and regular shapes, as in the present case. We took advantage of the proximity effect for decreasing the distance between features. Several types of structures, varying from closely packed discs to isolated thin rods, were patterned on CaF_2. Each type of structure had to be separately treated, since the varying shapes and sizes required very different doses.

For instance, we patterned optical antennas consisting on dimers of elongated rods with several microns length and a minimum separation of around 30 nm by, performing the exposure with doses ranging from 112 to 130 $\mu C/cm^2$. The overexposure of features was

not an issue for the final application and therefore, we slightly increased the dose when possible, with the aim of decreasing the inter-feature gaps.

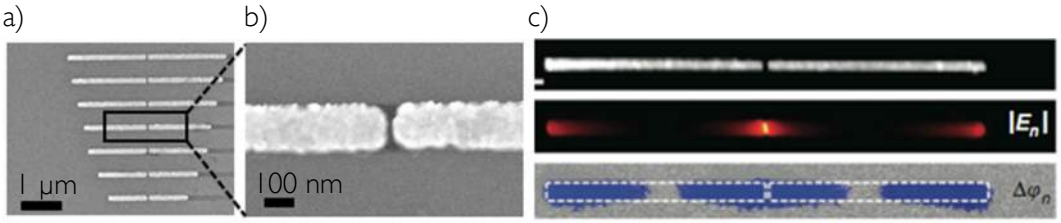

Figure 3.10. Optical antennas patterned on CaF_2. a) Scanning electron microscopy (SEM) image of an array of optical antennas with nanogaps. b) Detail of a gap of around 25 nm in a single structure. c) Topography, amplitude |En| and phase shift $\Delta\phi$n maps of a resonant gap antenna measured with a scattering type-scanning near-field optical microscope (s-SNOM), taken with permission from: Pablo Alonso-Gonzalez et al., Nature Communications 3, 684 (2012) [20].

Some of these structures were designed with tips that ended up in a tapering shape, which sometimes presented undesired asymmetries, as seen in Figure 3.11.

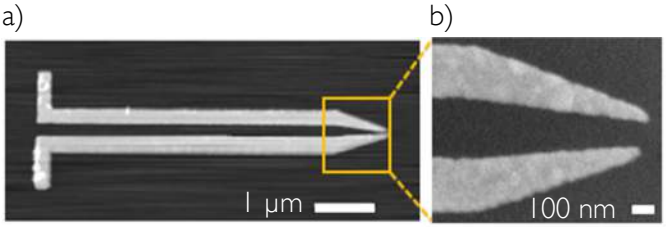

Figure 3.11. Optical antennas coupled to tapering transmission lines patterned on CaF_2. Taken with permission from: P. Sarriugarte et al., Optics Communications 285, 3378 (2012) [21].

These asymmetries were due to shadow-masking effects, which typically appear when the profile of the developed features in the resist has a high aspect ratio (as it was the case of the tapering tips) and the utilised metal deposition technique is highly directional. The easiest way of correcting these asymmetries would be rotating the sample during metal deposition. However, no rotation was used in this case because it increased the chances of depositing metal below the undercut profile of the double layered resist. This could result in a difficult lift-off, damaging the most delicate features, such as the pointy ends of the tapering tips.

The issue of the undesired asymmetries improved by controlling the orientation of the patterned features with respect to the evaporation sources. In the present case we had to repeat this operation for each metal (titanium and gold, respectively), since they came from different evaporation sources and consequently, they had different evaporation angles. This led to not only shadow masking, but also mismatching between the two evaporated metal

layers. The chips were placed as close as possible to the titanium evaporation source when loading the samples in the evaporator. After the titanium adhesion layer was deposited, the sample holder was rotated until the chips were placed near the gold evaporation source. We tried to keep the same orientation for the pattern in both cases, with the longest dimension of the features pointing towards the centre of the evaporation sources. Note that all these operations had to be done without opening the evaporation chamber, in order to avoid the oxidation of the deposited titanium layer. Unfortunately, the mismatching could not be totally suppressed, since the evaporator did not allow putting the samples directly above the evaporation sources, neither accurately controlling the orientation of the samples. If the mentioned precautions were not taken, the mismatching between the titanium adhesion layer and the gold could be as large as 30 nm, which could lead to overlapping between closely spaced features. .

A different example of the patterned structures consisted on closely packed groups of discs (see Figure 3.12). These structures had an enhanced proximity effect, due to their large areas and the close distances between the different features. Therefore, the dose had to be sensibly reduced in comparison to the other structures. Doses ranging between 25 to 100 $\mu As/cm^2$ gave the best results, achieving minimum inter-feature distances between 30 and 40 nm.

We must note that in some cases the inter-feature distance could be further decreased by depositing a thinner layer of metal for the pattern transfer, since it would probably allow performing the lift-off for features patterned at distances slightly below 30 nm. However, the application of the structures as plasmonic devices required having around 40 nm of gold for an optimum performance. Due to the thickness of the metallic layer and the small inter-feature distances the lift-off had sometimes to be assisted by extraordinarily long times of ultrasounds (around 60 seconds in the case of disc-like structures, for instance) that risked detaching the whole pattern from the surface.

In conclusion, the protocol proposed for general use with insulating substrates was successfully adapted for this particular case, yielding well defined and functional structures.

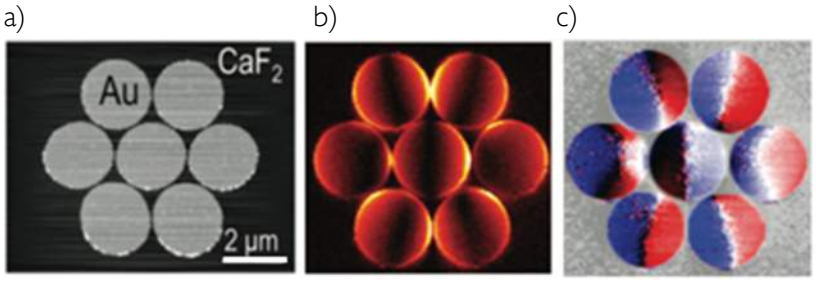

Figure 3.12. Disk-like plasmonic structures patterned on CaF_2. a) AFM image of the topography of an array of gold discs on CaF_2. b) Experimental near-field amplitude and phase images corresponding to the structures in a). Images taken with permission from: Pablo Alonso-Gonzalez et al., Nano Lett. 11, 3922 (2011) [22].

3.3. Patterning nanostructures on Si_3N_4 membranes

Silicon nitride (Si_3N_4) membranes are commonly used as substrates for transmission electron microscopy (TEM) imaging.

Typically, thin Si_3N_4 membranes are supported on a silicon disc of 3 mm in diameter (standard size for a TEM holder), which is covered by a Si_3N_4 film of around 200 µm in thickness. The substrate is etched away from the back side in order to create one or more windows in which thin Si_3N_4 membranes are suspended. Membranes of different thicknesses and sizes are commercially available (Figure 3.13).

Fabricating electronic devices on these membranes would allow combining multiple characterisation techniques offered by the TEM with the simultaneous measurement of charge transport properties. Moreover, the TEM offers the opportunity of manipulating materials at the atomic scale. For instance, we could create localised defects in a controlled manner by displacing individual atoms in a thin layer of material, such as graphene, dichalcogenides, or another member of the vast family of 2D materials, and correlate them to the effects in charge transport. In conclusion, building electronic devices on thin Si_3N_4 membranes could lead us to new and exciting experiments. Motivated by these prospects, we decided to work in the optimization of the EBL process for obtaining devices on Si_3N_4 membranes.

We used Si_3N_4 membranes of 15 nm thickness (Ted Pella Inc.) for optimising the EBL process. The membranes had a square shape with a lateral size of 100 µm and they were arranged in a 3 x 3 matrix in a standard silicon disc.

Figure 3.13. SEM images of Si discs (3mm in diameter) with Si_3N_4 membranes of different sizes. The images show a view of the windows etched into the Si substrate at the back side of the membranes. (taken from www. Ted Pella. com).

3.3.1. Substrate preparation

Cleaning

The as-received Si_3N_4 membranes had some kind of debris or particles on top, as we observed by optical microscopy (Figure 3.14). These particles could affect the uniformity of the resist coating and as a consequence, they could decrease the quality of the patterned structures. Immersion in solvents, such as acetone and isopropanol, did not remove these particles and the use of mechanical methods, such as ultrasound baths was out of the question, as the fragile Si_3N_4 membranes would be immediately shattered to pieces. No further attempt was made to remove the particles due to the risk of breaking the membranes.

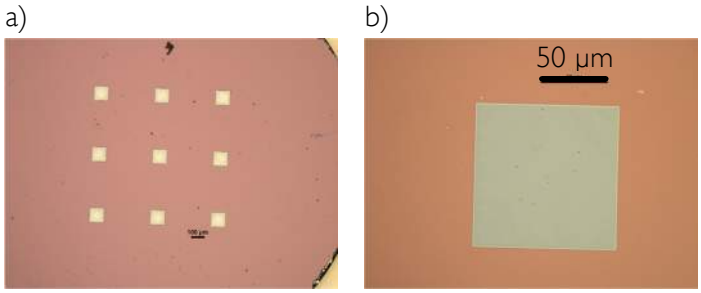

Figure 3.14. Optical microscopy image of the as received chips with 9 Si_3N_4 membranes (top view). Note that the surface is covered by some kind of debris or particles that might affect the resist coverage and therefore, the quality of the ultimate pattern. However, any attempt to remove them risks breaking the membranes.

The selected lithographic resist poly(methyl methacrylate) or PMMA showed a very poor adhesion to the Si_3N_4 surface. The adhesion improved after the membranes were cleaned by an oxygen plasma treatment before applying the resist. The details of the treatment are shown inTable 3.6.

Table 3.6. Conditions for oxygen plasma cleaning

P_{BASE} (mbar)	Oxygen flow (sccm)	Power (W)	Time (min.)
1	10	100	10

Spin coating with resist

The substrates were coated with a poly(methyl methacrylate) PMMA resist bilayer. Resists with different molecular weights were selected for favouring the formation of an undercut profile after developing and making the lift-off process easier, as explained in Chapter 2 (section 2.1.1). Thus, 495 PMMA A2 and 950 PMMA A2 were used as bottom and top resist layers, respectively, giving a total thickness of around 110 nm (measured with a profilometer).

We used a spin coater with a special chuck that held the chips by centrifuge force, instead of by vacuum, to avoid breaking the thin Si_3N_4 membranes (Figure 3.15). Each resist layer was spread at 3500 rpm for 5 minutes, followed by a baking step of 1 hour at 170°C in a convection oven. Baking in the oven allowed setting slow rates for warming up and cooling down the samples to room temperature, in order to prevent breakage by thermal shocks.

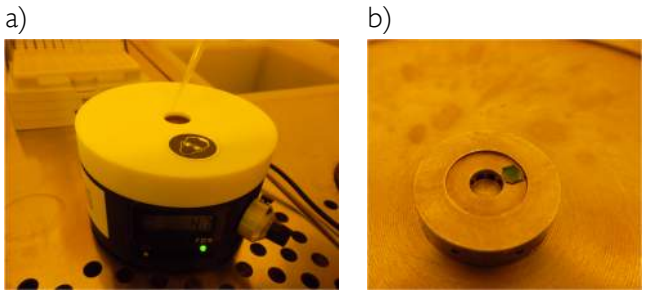

Figure 3.15. Chip with Si_3N_4 membranes on the spin coater. a)Spin coater. b) Detail of the chuck, where a chip is held by centrifuge force while spin coating with resist.

The chips were held by centrifuge force instead of by vacuum. This prevented breaking the membranes during spin coating. Optical microscopy imaging of the coated chips (Figure 3.16) showed that the particles observed in the as-received chips were still present all over the surface, causing an inhomogeneous coverage in localised areas. After spin coating with resist small wrinkles in the surface of the thin membranes were also more visible. We did not observe these wrinkles when working with membranes of 30 and 50 nm thicknesses. Both the particles and the wrinkles could affect negatively to the final results of the lithography but we did not find any possible way to eliminate them without damaging the fragile membranes.

We must note that the spin coater was not originally prepared for the small size and round shape of these chips. One of the consequences was that the resist formed a thicker layer in the area where the chips were lined against the wall of the chuck. We placed the chips with the same orientation when coating with the second layer of resist, in order to have as uniform as possible resist films near the membranes in the central area.

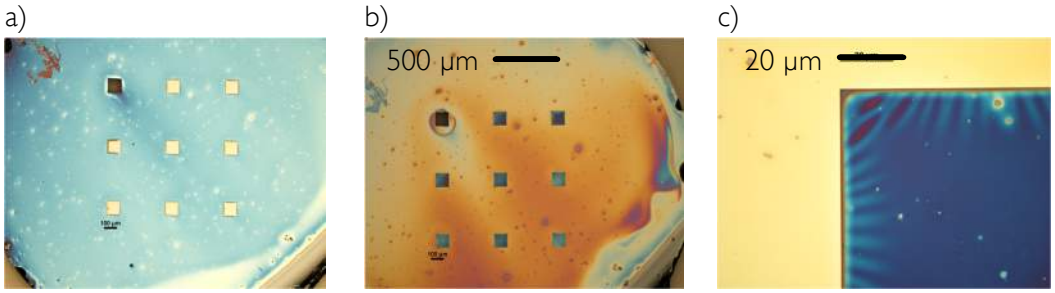

Figure 3.16. Optical microscopy image of the surface of a chip after spin coating with resist and baking. a) All 9 membranes coated with the bottom resist layer. b) and c) were taken after coating with the double layer of resist. The particles that were present on the surface of the as-received chips are more visible after coating with resist, since the thickness of the resist is slightly different around them. Missing membranes (accidentally broken during manipulation of the chips) also lead to inhomogeneity in the resist thickness, as it can be seen in a) and b). The thin membranes present wrinkles on their surface, especially in the edges, as it can be seen in c).

3.3.2. Electron-beam exposure

Thin Si_3N_4 membranes are almost transparent to the electron beam, meaning that the substrate causes a negligible back scattering of the incident electrons. This is in principle favourable, since it leads to a lower proximity effect and a higher resolution (see section 2.1.3 in chapter 2). As a consequence of the reduced scattering, exposing the resist requires a higher dose than in the case of thicker substrates.

We used a test pattern consisting of parallel rectangle arrays with a size of 100 nm in width and 300 nm to 5 µm in length. We also added closely separated rectangle pairs, since we had the future prospect of fabricating devices with the smallest possible inter-electrode gaps. The structures were written with 10 kV and 20 kV acceleration voltages and 10 µm aperture, (corresponding to around 20 pA and 40 pA currents, respectively). At higher voltages the resolution capability of EBL increases, due to a smaller beam size and reduced forward scattering of the electrons inside the resist layer. On the other hand, lower voltages lead to more forward scattering and give a more pronounced undercut profile when a resist of higher sensitivity is used as bottom layer, making the lift-off easier. The purpose was to find a compromise between an adequate definition of the structures and a gentle lift-off that would preserve the integrity of the thin Si_3N_4 membranes.

The TEM chips we used were approximately round shaped, and they did not have pre-patterned alignment marks. Thus, we had to carefully place the origin of the coordinate system and perform the tilting correction of the x and y axis using the corner of two Si_3N_4 membranes. In addition, a 3-point adjustment was performed for a more accurate alignment of the pattern, using the two mentioned reference points and the corner of a third membrane (see Figure 3.17). This meant that we partially exposed the corner of three membranes, where the metal attached strongly during deposition and could eventually result in a difficult lift-off.

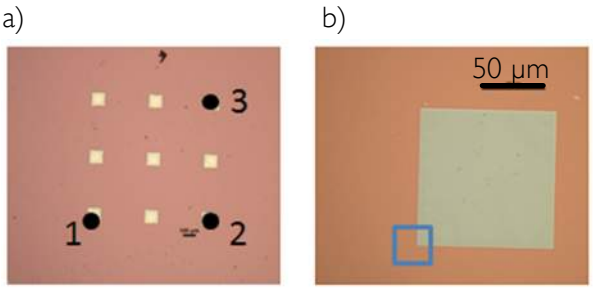

Figure 3.17. Alignment of the pattern on the membranes. a) Optical microscopy image with a representation of the reference points used for the adjustment of the coordinate origin, the correction of tilting and the alignment of the pattern on the membranes. b) Square at the corner of a membrane indicating the spot used for alignment purposes.

Doses ranging from 150 to 450 $\mu C/cm^2$ were used with the 10 kV voltage and 300 to 900 $\mu C/cm^2$ with 20 kV voltage, respectively. As the sensitivity of PMMA is roughly proportional to the employed voltage, the dose needed for exposing PMMA at 20 kV is about twice as much as the one needed at 10 kV. The corresponding exposure parameters were calculated as shown in section 2.1.3 of Chapter 2.

3.3.3. Developing

The developing of the exposed resist was carried out by immersion in a mixture of methyl isobutyl ketone and isopropyl alcohol (MIBK/IPA 1:3) for 1 minute. After quenching the developing process by immersion in IPA the chips were dried with a N_2 gun. The developed pattern was inspected by optical microscopy (see Figure 3.18).

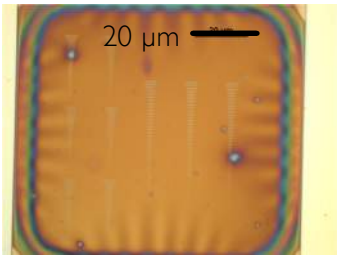

Figure 3.18. Developed pattern on 15 nm Si_3N_4 membranes. Optical microscopy image of a membrane after electron beam exposure and developing of the resist.

3.3.4. Metal deposition and lift-off

The pattern transfer was carried out by metal evaporation and lift-off. An adhesion layer of e-beam evaporated titanium followed by thermally evaporated gold were deposited on top of the resist mask. Table 3.7 shows the evaporation conditions.

Table 3.7. Conditions for metal deposition on Si_3N_4 membranes

Material	P_{BASE} (mbar)	$P_{EVAPORATION}$ (mbar)	Rate (Å/s)	Thickness (nm)
Ti	$\sim 10^{-6}$	$\sim 10^{-5}$	0.3	2.5
Au	$\sim 10^{-7}$	$\sim 10^{-5}$	0.3-0.5	40

The chips were held with Kapton tape onto a glass slide for optical microscopy, which was then clamped to the holder inside the evaporator (see Figure 3.19 a). The metal deposition presented the problem of having different evaporation angles for titanium and gold with respect to the samples. As explained in previous sections (see 3.2.2), this forced us to change the position of the samples for the evaporation of each material, in order to reduce the mismatching between the two deposited layers (Figure 3.20). The chips were placed as close as possible to each evaporation source and the pattern was oriented with the elongated features pointing towards the centre of the source (Figure 3.19 b).

Figure 3.19. Procedure for metal evaporation. a) The chips were held with Kapton tape on a glass slide for optical microscopy and clamped in the sample holder inside the evaporator chamber (1). The samples were

placed close to the electron beam evaporation source (2), where titanium was deposited. Afterwards, the holder was rotated until the samples were placed near the thermal evaporation source (3), where gold was deposited. In both cases we fixed the orientation of the pattern with the longitudinal dimension pointing towards the evaporation source, as accurately as possible (represented by the straight arrows in the positions 2 and 3).The dashed circles are a qualitative representation of the front of the evaporated material when it reaches the samples at a distance from each evaporation source.

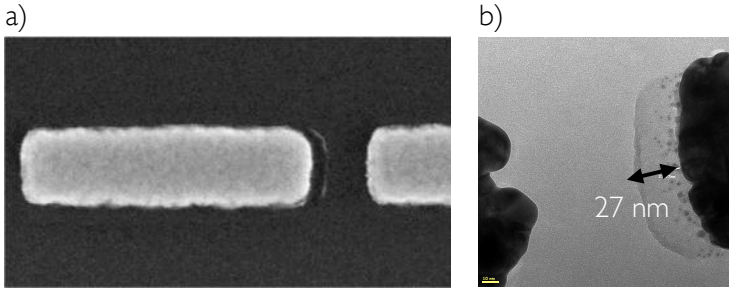

Figure 3.20. Mismatching of deposited Ti and Au layers. a) SEM image and b) TEM image of a gap between the patterned structures showing a mismatching of around 30 nm between the Ti adhesion layer and the Au layer due to the different evaporation angles.

No rotation was used during the evaporation, since we wanted to benefit from the undercut profile of the double layer resist system in order to have an easier lift-off (see Figure 3.21 b). Having a mild lift-off process was critical in the case of the extremely fragile Si_3N_4 membranes, since the process could not be assisted with the application of ultrasounds.

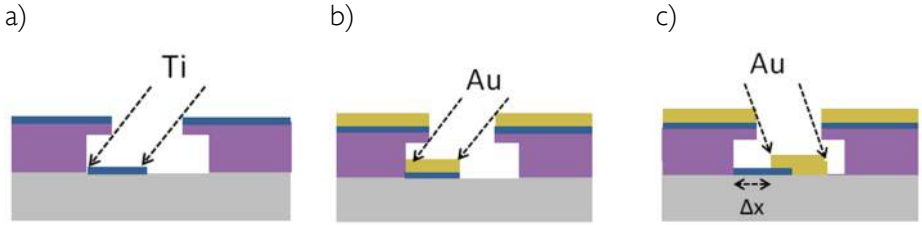

Figure 3.21. Evaporation of Ti and Au layers. Sketches representing the evaporation of Ti and Au on a resist mask with undercut profile. a) Ti is evaporated at an angle, resulting in a shadow masking effect. b) Au is evaporated at a similar angle as Ti (ideally we should use the same angle, although it is not possible to control it with accuracy in the utilised evaporator). This situation, in which the two deposited layers would have a minimum mismatching, is represented in Figure 3.19 b. c) If the Au has a very different evaporation angle, it leads to a large mismatching (Δx).

The resist mask was lifted off after an overnight immersion in acetone, assisted by squirting gentle acetone jets around the chips (but never directly on top of them) with a rinsing flask, for removing the metal that could still remain partially attached. The total

soaking time needed for lift-off in acetone varied from around 2 hours to a whole night. The samples were inspected with the optical microscope (while still immersed in acetone) and left for a longer time or gently squirted with acetone, until the remaining metal was removed.

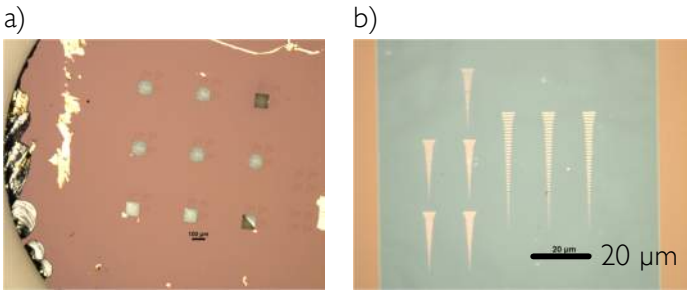

Figure 3.22.) Optical microscopy image of a patterned chip surface after meal deposition and lift-off. Two membranes broke down during the process. b) Detail of the pattern on one of the thin Si_4N_3 membranes.

The lift-off was equally effective for patterns written with 10 kV and 20 kV. The contour of the structures was in general well defined for either of the utilised exposure conditions (Figure 3.23). We did not observe a substantial reduction of the proximity effect when working with 20 kV, opposite to what we observed when patterning on silicon substrates, for instance. This probably happens because the back scattering of electrons in the thin membrane, which is the principal responsible for proximity effect, was low for both employed beam energies. We finally selected 10 kV and a dose of around 400 µC/cm^2 as adequate working conditions for patterning electrodes with nanometric gaps. However, we sometimes wrote sets of electrodes with the same nominal gaps employing higher doses (425 or 450 µC/cm^2). Thus, we slightly overexposed the resist on purpose, taking advantage of the proximity effect in order to decrease the gap size. Lower doses (around 150 µC/cm^2) were needed for patterning structures with a larger area (>1 µm^2), such as contact pads.

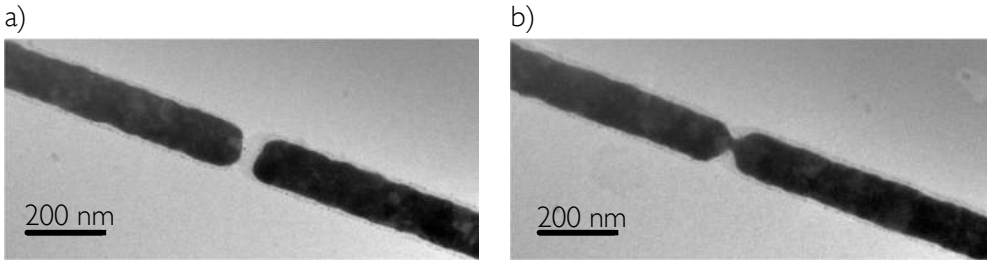

Figure 3.23. TEM image of structures patterned on Si_3N_4 membranes. The gap in a) had a nominal size of 70 nm, while the real size is close to 40 nm after the whole lithography process. The image in b) was originally a

gap of 60 nm but turned out to be closed after lift-off, resulting in a constriction of around 25 nm. Both structures were written with 10 kV voltage and a dose of 400 μC/cm^2.

3.3.5. Solving mechanical stability issues

Having 15 nm in thickness and 100 μm lateral dimensions, the thin membranes could present mechanical stability issues for certain applications of the patterned structures. Moreover, we observed that these membranes acquired a curvature when air was trapped by PMMA in the cavity behind them and the samples were subjected to low pressure environments, as it happened during exposure and metal deposition steps (Figure 3.24). This might affect negatively the final results, since it could lead both to distortion of the patterned features during exposure and uneven shadow masking effects during metal evaporation.

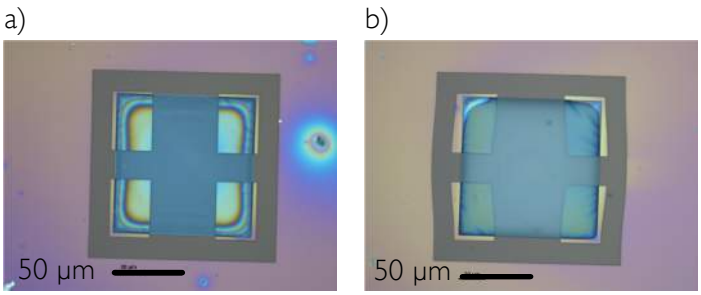

Figure 3.24. Pattern distortion due to mechanical instability. Optical microscopy image showing a developed pattern of a frame around two membranes. The membrane in a) kept the original shape while the one in b) had clearly acquired a convex shape during exposure, leading to a distorted pattern.

This problem could be entirely avoided by preventing the PMMA from entering the windows etched at the back side of the membranes, although we did not find a safe way to do it. Fortunately, the blocking of membranes by PMMA did not happen systematically in all the samples. The mechanical stability issue was partially solved by patterning robust metallic frames in a previous lithography step in order to hold more tightly the membranes. The thick frames could also help for heat dissipation during the characterisation of the structures with a high energy electron beam in the TEM, for instance.

The metallic frames were patterned using essentially the same procedure as for the nanostructures presented in this section. However, a higher current was used for the electron beam exposure of the frames, since their dimensions were in the order of 100 μm. We also patterned four alignment marks around each membrane, in order to correctly match the subsequent lithography layers (as explained in section 2.1.3 of chapter 2). The shape of the windows opened on the frames was adapted depending on the nanostructures we needed to fit inside them.

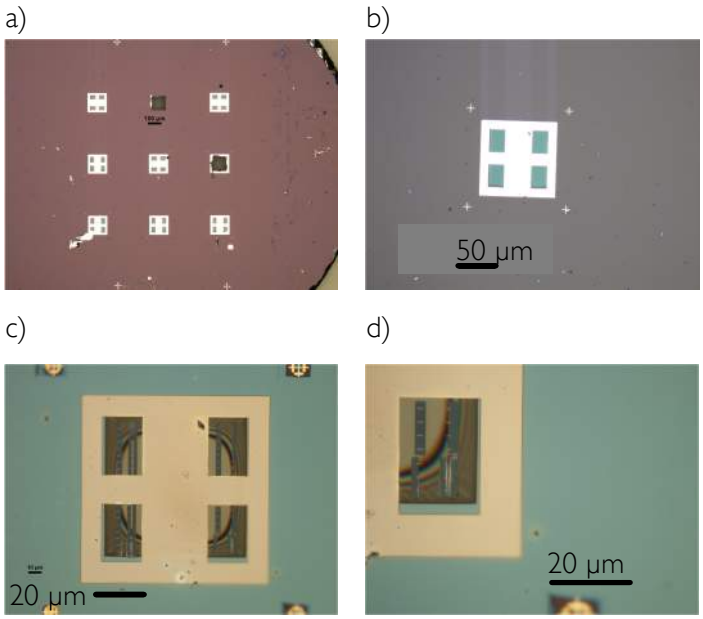

Figure 3.25. a) Optical microscopy image of a chip after patterning metallic frames around the membranes. b) Detail of a membrane with four alignment marks, (small crosses at each corner). c) Optical microscopy image of a membrane after patterning metallic nanostructures inside the frames in a second lithography process. d) Detail of structures in a smaller framed area of a membrane.

The employed beam conditions are shown in Table 3.8 . A dose of 150 µC/cm^2 was found to be sufficient for exposing the resist with a higher current. We deposited palladium on the frames by magnetron sputtering. We chose sputtered palladium because in our experience, it results in a quick and mild lift-off. However, other metals could have been employed, provided that the deposited layer was thick enough for stabilising the membranes. In our case, 60 nm of palladium served well for this purpose. We could also employ a thicker resist for an easier lift-off (for instance, 495 PMMA A4 as bottom layer 950 PMMA A2 as top layer, which would result in around 250 nm of a total film thickness), especially if a thicker metallic layer was desired for the frames.

Table 3.8. Column conditions for electron beam exposure of frames on Si_3N_4 membranes

Acceleration voltage (kV)	Aperture size (µm)	I_{BEAM} (pA)	Write field size (µm)
10	30	~900	200

Table 3.9. Conditions for Pd deposition on Si_3N_4 membranes

Technique	P_{BASE} (mbar)	P_{Ar} (mbar)	Rate (Å/s)	Thickness (nm)
Sputtering	4×10^{-6}	6×10^{-3}	2.5	60

3.3.6. Summary: General protocol for EBL on Si_3N_4 membranes

In conclusion, we patterned nanostructures consisting on 40 nm thick gold (with a titanium adhesion layer of around 2 nm) on top of suspended Si_3N_4 membranes. The lithography was successfully performed on membranes of 15 nm, 30 nm and 50 nm thicknesses. We followed the same procedure for EBL in all the cases, although an additional lithography step was performed for patterning reinforcement frames on 15 nm thick membranes. The steps of the lithography process are summarised in Table 3.10.

Table 3.10. General procedure proposed for EBL on Si_3N_4 membranes. The procedure presented in this table includes the patterning of stabilising frames (steps 1 to 7) which may not be always needed (for instance, they were not required in the case of 30 or 50 nm thick membranes).

STEP	*PROCEDURE*
1) Substrate preparation	Commercial chips with Si_3N_4 membranes were treated with oxygen plasma for promoting the adhesion of the resist. Conditions: 100 W power, 1 mbar pressure, 10 sccm O_2 flow, 10 minutes.
2) Resist processing	Application of a 495 PMMA A2 /950 PMMA A2 bilayer. Spin coating at 3500 rpm for 5 minutes (use special chuck for holding the chips by centrifuge force), followed by 60 minutes baking in a convection oven at 170°C (repeat step 2 for each layer).
3) e-beam exposure	Exposure of stabilising frames and alignment marks with a current of 900 pA (corresponding to an aperture of 30 µm and an acceleration voltage of 10 kV). Utilised dose: 150 $\mu As/cm^2$.
4) Developing	Immersion in MIBK/IPA 1:3 for 1 minute, followed by an IPA rinse for 10 seconds and drying with a nitrogen gun.
5) Metal deposition	Sputtering 60 nm of Pd at an argon pressure of 6×10^{-3} mbar and a rate of 2.5 Å/s.
6) Lift-off	Immersion in acetone (1 to 2 hours). Gently squirt with acetone (while still immersed and not directly on top) for removing the attached metal, periodicallly inspecting with optical microscope. Immersion in IPA for rinsing. Drying with a nitrogen gun.
7) Resist processing	Repeat step 2
8) e-beam exposure	Exposure of nanostructures with a current of ~20 pA (corresponding to an aperture of 10 µm and an acceleration voltage of 10 kV). Utilised dose: 150 to 450 $\mu As/cm^2$ depending on the structures.
9) Developing	Repeat step 4
10) Metal deposition	Thermal evaporation of 40 nm Au (with 2 nm of electron beam evaporated Ti adhesion layer) at a base pressure of 10^{-6} mbar and a rate of 0.3 Å/s and 0.5 Å/s for Ti and Au, respectively.
11) Lift-off	Repeat step 6

3.4. Patterning nanostructures on exfoliated graphene flakes

Graphene is a 2D allotrope of carbon with suitable physical and chemical properties for a wide range of potential applications. Its flexibility, optical transparency and high mobility make it an excellent candidate for constructing novel devices for optoelectronics, spintronics, etc. However, as it refers to its charge transport properties, graphene is a zero bandgap semiconductor material. This is regarded as a main drawback when it comes to logic electronic applications, in which distinct on /off states are needed.

There are several references in literature about intentionally creating a bandgap in graphene by means of lithographic patterning [10]. Therefore, our main motivation for the fabrication of devices based on patterned graphene was trying to create a bandgap. The designed pattern was based on previous works that show how structuring the graphene into nanoribbons with a width in the sub-30nm range could lead to a bandgap opening. The cited work was focused on measurements on single nanoribbons [11-12]. We proposed patterning grid-like structures, where the width of the single grid bar is in the sub-30nm range to test if the bandgap could be tuned by changing the dimensions of the grid.

On the other hand, the obtained devices could also help understanding the nature of the charge transport through the graphene sheet. More specifically, they could be used for determining if the charge transport happens in a uniform 2D fashion before and after patterning the graphene (as it is usually assumed in theoretical calculations).

The fabrication of devices comprised two lithographic processes. In the first process, we defined metal electrodes for contacting the graphene flakes, employing a positive e-beam resist and an Au/Cr metal deposition. In the second lithographic process we used negative resist to pattern a mask that protects the graphene underneath during the etching of the unprotected graphene areas.

The work described in this section was carried out during an external stay of three months in the Nanocarbon Group of DTU Nanotech (the Micro and Nanotechnology department of the Tecnical University of Denmark in Kongens Lyngby, Denmark), under the direction of Professor Peter Bøggild.

The whole experimental process was carried out at the fabrication facilities of DTU-Danchip (Denmark's national centre for micro and nanofrabrication). DTU-Danchip has a class 100 to 10 cleanroom of 1350 m^2, endowed with a JEOL 9500 electron beam lithography writer. This instrument works at 100 kV acceleration voltage, which has the advantage of both high resolution and high speed.

3.4.1. Preparing the substrates: graphene exfoliation

The procedure for substrate preparation was quite different from the usual steps described in previous sections. We performed the lithography on a whole wafer scale, instead of using smaller chips and obtaining graphene flakes added several preparatory steps.

There are a few methods for obtaining graphene flakes on top of a silicon wafer coated with a thin layer of silicon dioxide (from now on Si/SiO_2 wafer). In this case we used the micromechanical cleavage method, also known as physical exfoliation. Currently, physical exfoliation still stands among the most popular methods for obtaining graphene crystals of microscopic size onto Si/SiO_2 wafers. The main drawback is its low yield, which limits its use to scientific research.

The whole process of preparing graphene flakes for lithography consisted of four main steps: (1) preparation of the Si/SiO_2 wafers, (2) graphite exfoliation, (3) transfer of the graphite flakes to the SiO_2 substrate and (4) single layer graphite (in other words, graphene) flake identification and selection.

Highly doped silicon wafers with a thermally grown silicon oxide layer of 90 or 300 nm thickness were used as substrates. The oxide layer provides electrical insulation for performing gated electrical measurement using the doped silicon substrate as a back gate. On the other hand, using certain oxide thicknesses allows optically identifying the graphene, as it will be explained later in this section.

DTU-Danchip provided us with wafers that had been patterned with index marks. The index marks consisted of unique symbols (crosses and numbers) made of gold (around 100 nm in thickness) and defined by photolithography. They were distributed all over the wafer surface in an orthogonal grid with a 500 μm pitch. These marks were used as coordinates for the identification of graphene flakes, as well as for the accurate alignment of different lithographic layers.

Immediately before performing the transfer of the graphene flakes, the wafers were baked and cleaned in order to avoid any traces of moisture and organic molecules that could be adsorbed onto the silicon dioxide surface. The baking was done in a hot plate at 200 °C for around 30 minutes, immediately followed by a plasma treatment in a plasma asher oven (see conditions inTable 3.11).

Table 3.11. Conditions for oxygen plasma cleaning of SiO_2 before graphene transfer

P_{BASE} (mbar)	O_2 flow (sccm)	N_2 flow (sccm)	Power (W)	Time (min.)
0.7	200	50	400	10

Regarding the preparation of graphene flakes, the micromechanical cleavage or physical exfoliation method consists on using two adhesive surfaces for splitting graphite crystals into thinner layers. Employing materials that leave fewer residues, such as a dicing tape ("blue tape") used in our case, is much preferred. Cleaving graphite repeatedly between two stripes of adhesive tape yields much thinner crystals, in which perfectly clean and atomically flat surfaces are exposed. These newly exposed surfaces can adhere very tightly to a clean silicon oxide surface thanks to the van der Waals interactions. In fact, properly transferred graphene flakes can stand spin coating with resists and immersion in several solvents without detaching from the wafer.

We employed an entirely manual process for graphene exfoliation and therefore, we do not have exact data for exactly reproducing this operation, such as the amount of pressure applied, etc. The skills for obtaining adequate graphene flakes are acquired by trial and error, with much care, patience and a great deal of good luck.

Natural graphite crystals with dimensions of around 1 cm^2 and 1 mm in thickness were used in this project. First, the crystal surface was repeatedly cleaved by manually pressing it against a piece of blue tape (as if it were a stamp) and carefully lifting it with the aid of tweezers. Crystals of a large area and a few microns in thickness can be cleaved from the initial graphite crystal if this operation is repeated applying the adequate pressure and cleaving with care. A piece of tape the size of a 4 inch wafer was thus covered with thin graphite crystals. Another piece of tape of the same size was then placed on top, covering the flakes and taking care not to leave bubbles in between the two tapes. A manual roller was used for assisting this step by applying gentle pressure. The two pieces of blue tape were detached from each other just before doing the transfer to the wafers. This ensured that the graphite crystals were cleaved one last time and freshly exposed surfaces were applied on the wafers.

We transferred the graphene to the wafers by applying the adhesive tape with freshly cleaved flakes onto the silicon dioxide wafer surface. Additionally, a gentle and uniform pressure was applied on top with a manual roller. It is important doing this step as quickly as possible, while the wafers are still hot from the plasma treatment and the cleaved graphene surfaces have barely been exposed to the environment. This improves the adhesion and minimises the contamination of the interface between graphene and silicon oxide. After a few minutes, we placed the wafer on a hot plate at 70 °C for about 15 seconds and slowly peeling off the adhesive tape assisted by the gentle heating. As a result, a distribution of graphitic flakes of different sizes and thicknesses covered the wafer surface. However, only a few among them were single layer graphene flakes with proper conditions for lithography (i.e. without cracks and with a minimum lateral dimension of around 20 μm). Typically, the yield of physical exfoliation was of fewer than 10 usable single layer flakes per wafer.

The detection and selection of suitable flakes was done by inspecting the wafers under the optical microscope. Graphene flakes absorb an appreciable amount of the incident light, so they can be optically identified by the contrast change with respect to the silicon dioxide substrate. An optimum optical contrast of 5-10% is observed for oxide thicknesses of 90 nm and 300 nm. Taking advantage of this property, the Nanocarbon Group at DTU has developed its own software for automatically identifying single, double and triple layer flakes on optical microscopy images of the wafer surface.

An optical microscope with a motorised stage was set for scanning the whole wafer surface and taking an image every 1000 μm. Afterwards, all the captured images were analysed by the home-made software, in which the optical contrast indexes of the single layer graphene flakes had been inserted. The contrast indexes were calculated by subtracting the RGB index values of the background image to those corresponding to an image of a single layer graphene flake. The software found the areas with the entered RGB index values and generated new images where the contour of the graphene flakes were marked (Figure 3.26). It took around 4 hours to map a 4 inch wafer, so usually 2 wafers were left scanning overnight. The selected images were then loaded into a program for pattern design, in which the required lithographic layers could be directly drawn on the graphene flakes.

After selecting the most suitable specimens, all the rest of the wafer surface was stripped clean of the unwanted flakes with the use of adhesive tape, a pair of tweezers and the optical microscope. The manual cleaning procedure is the most effective but yet, time consuming alternative for selectively cleaning the wafer surface. This step is necessary in order to have a uniform coverage when spin coating the whole wafer with the lithographic resists.

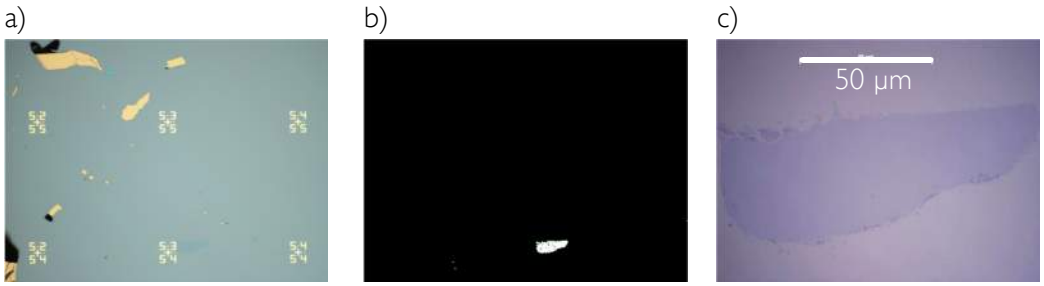

Figure 3.26. Identification of single layer graphene flakes. a) Optical microscopy image of the surface of a wafer after transferring exfoliated graphene flakes. Most of the transferred flakes are thicker than a few monolayers. A single layer graphene flake is laying near the 53, 54 index mark. b) Image generated from a) after optical constrast analysis for single layer graphene detection. The single layer graphene flake was identified and its contour marked by the software (light area at the bottom of the image). c) Closer image of the identified single layer graphene flake (translucent blue contour).

3.4.2. Patterning electrodes for contacting graphene flakes

Once the substrates had been prepared for lithography, the next thing to do was patterning metallic electrodes for electrically contacting the graphene flakes. This was done by an additive lithographic process employing the positive resist poly(methyl methacrylate) or PMMA. Our main target was obtaining high quality metallic contacts in a reproducible manner.

3.4.2.1. Spin coating with resist

One of the main difficulties of performing lithography on graphene is that no ultrasounds can be applied in the lift-off step, as the flakes may detach from the surface. Therefore, a suitable combination of resists must be used, especially when working at high acceleration voltages, which give very sharp resist profiles with a small undercut effect. We chose a double layer PMMA resist system of very different molecular weights and concentrations, in order to enhance the undercut effect that leads to an easier lift-off. After testing several combinations of resists, a bottom layer of 25 kDa PMMA (15% in anisole) and a top layer of 996 kDa PMMA (2% in methyl isobutyl ketone) were selected. The higher concentration and lower molecular weight of the bottom resist provided a thick layer with a high sensitivity to the electron beam. In contrast, the low concentration and high molecular weight of the top layer resulted in a thinner and less sensitive film. On the other hand, the use of a different casting solvent for each resist layer avoided intermixing and consequently, provided more uniform films throughout the whole wafer surface.

The wafers were coated with 25 kDa PMMA (15% in anisole) and 996 kDa PMMA (2% in methyl isobutyl ketone), employing a spin coater at 4000 rpm for 1 minute. A baking step of 5 minutes in a hot plate at 195 °C was done after applying each layer.

Finally, a thin layer of aluminium was thermally evaporated on top of the resist for avoiding charging effects during the e-beam exposure (seeTable 3.12). In principle, this step is not necessary when using highly doped silicon substrates and silicon oxide thicknesses below 300 nm, however, it is mandatory in the protocol for EBL at Danchip.

Table 3.12. Evaporation of Al for charge dissipation purposes

Material	P_{BASE} (mbar)	$P_{EVAPORATION}$ (mbar)	Rate (Å/s)	Thickness (nm)
Al	$\sim 10^{-5}$	$\sim 10^{-4}$	5	15

3.4.2.2. Electron beam exposure

The electrodes were designed and distributed depending on the size and shape of the flakes, as well as on the type of experiments that had been proposed in each case. The smallest feature size in the pattern was 700 nm (width of the electrode tips) and the biggest contact pads were 800 μm across. The electron beam (a JEOL 9500) was set for performing the exposure at a current of 60 nA (see Table 3.13). These conditions resulted in a beam size of about 25 nm.

Table 3.13. Column conditions for electron beam exposure on graphene flakes

Acceleration voltage (kV)	Aperture size (μm)	I_{BEAM} (nA)	Write field size (μm)
100	200	~60	1000

A film of 995 kDa PMMA should have a clearing dose of around 1000 μC/cm^2 for an electron beam working at 100 kV. An exposure dose of 1200 μC/cm^2 was selected as the most adequate after testing several values between 1000 μC/cm^2 and 1400 μC/cm^2, the former of which was slightly underexposed and the latter seemed a bit excessive.

3.4.2.3. Developing

After the exposure, the 15 nm Al layer was etched by 1 minute immersion in MF-CD26 (a commercial solution of tetramethyl ammonium hydroxide) and rinsed immediately for 2 minutes in a flowing deionised water bath. The wafer was then blown dry with a nitrogen gun.

The exposed resist was then developed by immersing the wafer for 1minute and 30 seconds in MIBK/IPA 1:3 (methyl isobutyl ketone / isopropyl alcohol), and rinsed in IPA for 2 minutes. After this step the wafer was again dried by blowing with a nitrogen gun. The MIBK/IPA selectively dissolved the exposed areas, revealing the electrodes patterned on the PMMA. The chosen combination of resists resulted in a deeply undercut profile at the edges of the pattern (Figure 3.27).

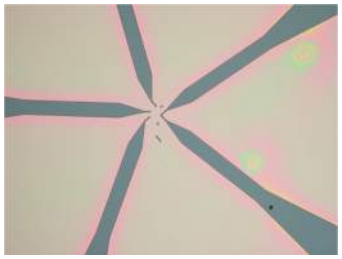

Figure 3.27. Electrodes patterned on PMMA. Optical microscopy imaging of the developed pattern revealed that the electrodes written a dose of 1200 μC/cm^2 had well-defined features and a considerable undercut (hinted by the change in the contrast of the resist at the edges of the pattern).

3.4.2.4. Metal deposition and lift-off

The pattern on the resist mask was transferred to the wafers by metallisation and lift-off.

The developed wafers were loaded into a *Wordentec QCL 800* evaporator. An adhesion layer of titanium followed by 30 nm of gold were deposited by electron beam evaporation (details in Table 3.14).

Table 3.14. Conditions for metal deposition on graphene flakes

Technique	P_{BASE} (mbar)	$P_{EVAPORATION}$ (mbar)	Rate (Å/s)	Thickness (nm)
Ti	~3 x 10^{-6}	~10^{-4}	0.5	2
Au	~1 x 10^{-6}	~10^{-4}	0.5	30

When inspecting the metallised wafer surface under the optical microscope we found that it was covered with bubbles, as shown in Figure 3.28. It was initially thought that the bubbles were due to the degassing of the resist. However, after doing tests with different post baking times (up to 1 hour), we found out that the bubbles produced during gold deposition were due to the degradation of the resist by the radiation coming from the evaporation source. This theory was confirmed after observing that the lift-off worked well when using a thick (25 kDa PMMA of 15% concentration) bottom resist layer and however, it did not work when a thinner resist (25 KDa PMMA of 8% concentration) was used. This meant that in the second case, the whole thickness of the resist was hardened and therefore, it did not dissolve in acetone, even after applying ultrasouds. On the contrary, employing a thicker resist layer preserved the original solubility characteristics of the polymer that was in contact with the substrate, allowing the lift-off with acetone.

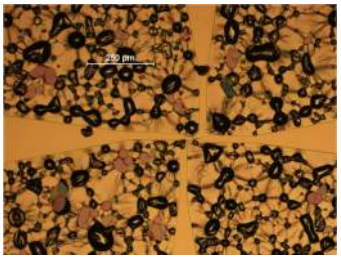

Figure 3.28. Bubbles on the surface of the metallised resist. The surface of the resist was totally full of bubbles after evaporation of titanium and gold, although it did not cause any distortion of the pattern.

The metallised resist was then lifted off by immersion in acetone. The metal was easily removed after about 5 minutes, by gently squirting a jet of acetone (using a rinsing flask) while keeping the wafer under the same solvent in a shallow petri dish. We checked carefully under the optical microscope if the lift-off was complete around the smallest features of the electrodes, while still immersed in acetone. When all the metal was removed, we transferred the wafer to a beaker with a big volume of clean acetone (200-300 ml) and kept it there overnight. Afterwards, the acetone was warmed up to 40 °C for around 2 hours in order to remove as much PMMA as possible by increasing its solubility. We must note that it is very important not to let the wafer surface dry at any moment during the lift-off, especially until all the metal has been removed. If the metal flakes that float into the solvent are allowed to dry on the surface, they attach to it almost irreversibly.

The wafer was finally rinsed by immersion in milli-Q water and IPA (for around 30 seconds in each) and dried on a hot plate at 50 °C for approximately 3 minutes.

The process resulted in well-defined electrodes with a minimum feature size (width) of approximately 1 µm. The graphene flakes were in general not damaged during the process (see Figure 3.29).

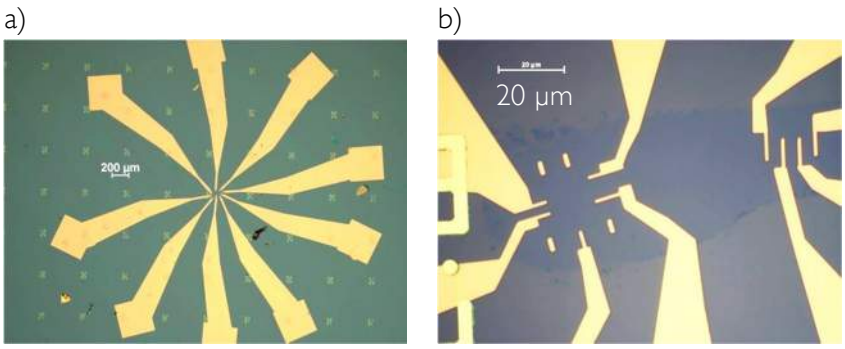

Figure 3.29. Electrodes patterned onto a graphene flake. a) Optical microscope image of a graphene flake on which two sets of electrodes have been patterned by electron beam exposure, metal evaporation and lift-off. b) A closer view of the same devices.

3.4.3. Patterning nanostructures with high resolution resists

Once the electrodes for contacting the graphene flakes had been defined, we proceeded to patterning arrays of low dimensional structures on the flakes. We chose to do it by a subtractive patterning process, employing a negative tone resist. The patterned structures were transferred to the graphene by reactive ion etching, using the resist as a hard mask. The designed patterns consisted on arrays of lines forming orthogonal grid-like structures. The width of the lines and pitch size were varied as shown in Table 3.15.

Table 3.15. Linewidth and pitch size utilised in the tests with HSQ

Grid	Linewidth (nm)	Pitch size (nm)
G1	50	100
G2	50	150
G3	20	100
G4	20	75
G5	10	100

We selected Hydrogen silsesquioxane (HSQ) as the most suitable resist for several reasons. First, patterning a design with a minimum feature size of 10 nm required a high resolution resist, as it is the case of HSQ. Second, being a negative resist it should act as a hard mask, protecting the patterned areas and allowing the selective etching of the exposed graphene areas. Finally, the chemical composition of the cross-linked HSQ, similar to that of silicon dioxide, made it a suitable material for the encapsulation of the patterned graphene [13,14]. However, HSQ has some disadvantages, such as its high sensitivity to moisture and air. Aging can affect the exposure dose needed and therefore, it should be taken into account for reproducibility, especially when working near the resolution limit of the resist [15].

3.4.3.1. Spin coating with the resist

The wafers were first baked for approximately 2 minutes on a hot plate at 100°C for desorbing the moisture from the surface, in order to improve the adhesion of the resist. An HSQ solution of 2% concentration in MIBK (XR-1541 from Dow Corning) was spun onto the wafers at 3000 rpm for 1 minute, followed by a baking step of 3 minutes in a hot plate at 100°C and another one of 3 minutes at 200°C. Performing several baking stages with increasing temperature helps minimising mechanical stress inside the resist and provides more stability for the patterned structures. The final thickness was of approximately 30 nm in the applied conditions.

The HSQ coated wafers were metallised with 15 nm of thermally evaporated Al (at a rate of 5Å/s) for avoiding charging effects during electron beam exposure. The metallisation with Al was done immediately after applying the resist, in order to minimize its exposure to air.

3.4.3.2. Electron beam exposure

The patterning on HSQ was performed in a JEOL 9500 EBL writer working at 100kV acceleration voltage.

The writing was performed at a current of 2 nA and an approximate beam size of 4 nm. The electron beam settings are shown in the following table. We did a dose test between 10 mC/cm^2 and 38 mC/cm^2 (increasing in steps of 2 mC/cm^2), in order to determine the most suitable conditions for patterning the grid-like structures.

Table 3.16. Column conditions for patterning with HSQ

Acceleration voltage (kV)	Aperture size (μm)	I_{BEAM} (nA)	Write field size (μm)
100	60	~2	500

3.4.3.3. Developing

After the exposure, the Al layer on top of the resist was etched by 1 minute immersion in MF-CD26 (a commercial aqueous solution of tetramethyl ammonium hydroxide). As the HSQ resist was developed by the same solvent, the wafer was immediately transferred into another container with clean MF-CD26 and kept there for 90 seconds. This change of solvent was done to minimize the contact with the dissolved Al complexes, which may adsorb onto the graphene. Afterwards, the wafer was thoroughly rinsed by immersion in a flowing deionised water bath for at least 4 minutes and dried with a nitrogen gun.

The areas where the resist had been exposed to the electron beam stayed as solid structures, while the rest of the layer was dissolved by de developer.

We first performed SEM imaging of some grids patterned on silicon dioxide for determining the most appropriate doses. We added parallel line arrays which stemmed (horizontally and vertically) from the grids with the same linewidth and pitch size (Figure 3.30). These lines needed a higher exposure dose than the grid, since there was a lower proximity effect (due to a lower pattern density). We decided to define a lower limit for the exposure dose of the grids based on the amount of dose needed for defining these

parallel line arrays. In this manner, we ensured a minimum robustness of the patterned grids. Table 3.17 contains a summary of the dose test experiments.

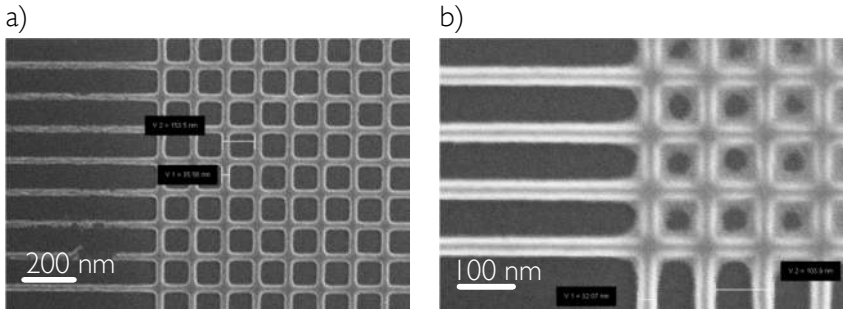

Figure 3.30. Examples of underexposed and overexposed patterns. SEM images of HSQ grids patterned on silicon dioxide for dose testing. We added parallel line arrays which stemmed (horizontally and vertically) from the grids with the same linewidth and pitch size. We decided to set a lower limit for the exposure dose based on the minimum amount needed for defining these parallel line arrays. a) Grid with a dose considered as insufficient, since the parallel line array is not fully exposed. b) Pattern with an excessive dose, leading to the partial exposure of the area inside the grid.

Table 3.17 Results of the dose tests with HSQ on silicon dioxide. The tabulated values have been extracted from SEM images and are approximate. We refer as *minimum dose* to the one necessary for obtaining well defined grids and line arrays (the latter are patterned at the edge of the grids, as previously shown in Figure 3.30). We have called *optimum dose* the one that results in a linewidth as close as possible to the nominal value. We do not know the minimum dose value for 10 nm linewidth, since we tested a smaller range of doses (from 22 to 26 mC/cm^2) in this case.

Nominal linewidth (nm)	Nominal pitch (nm)	Minimum dose (mC/cm^2)	Minimum linewidth (nm)	Optimum dose (mC/cm^2)
50	100	10	38	16
50	150	12	39	18
20	75	16	16	18
20	100	16	14	20
10	100	No data	14	22

We aimed at obtaining grids with linewidths ranging from 10 nm to 20 nm. The structures that best matched our requirements resulted from patterning grids with 10 nm and 20 nm nominal linewidth and 100 nm pitch size. Figure 3.31, Figure 3.32 and Figure 3.33 show some examples of patterned grids where the obtained feature sizes were smaller than the designed ones.

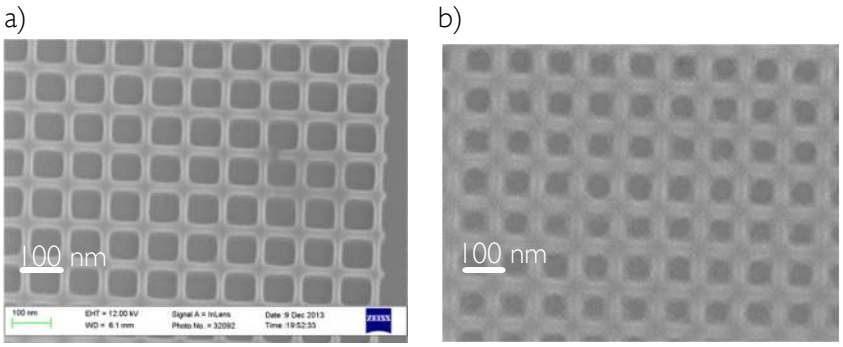

Figure 3.31. Tests with 10 nm linewidth grids. SEM images of HSQ grids of 10 nm linewidth and 100 nm pitch size patterned with HSQ on silicon dioxide. a) Image corresponding to an exposure dose of 22 mC/cm^2, where the obtained linewidth and pitch size were of around 14 nm and 101 nm, respectively. b) Shows the same pattern written with 26 mC/cm^2, where the holes of the grid are partially closed due to overexposure. A test with 24 mC/cm^2 (not shown here) resulted in a similar situation.

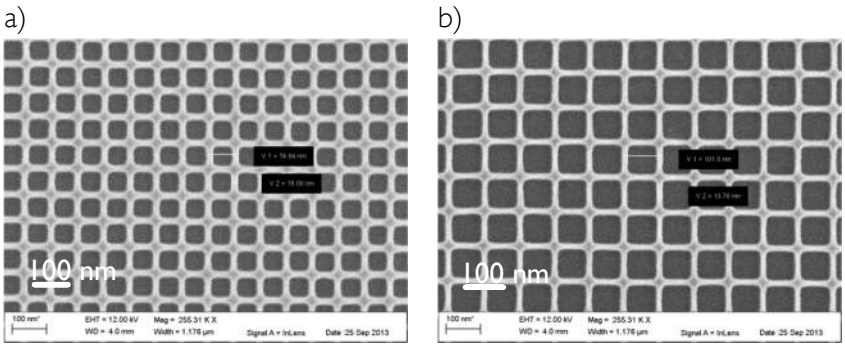

Figure 3.32. Tests with 20 nm linewidth grids. a) SEM image of a grid with a nominal linewidth of 20 nm and a pitch size of 75 nm patterned with a dose of 16 mC /cm^2. The obtained linewidth and pitch were of around 16 nm and 75 nm, respectively. b) Grid with a nominal linewidth of 20 nm and 100 nm pitch size patterned with the same dose. In this case we obtained around 14 nm and 100 nm, respectively.

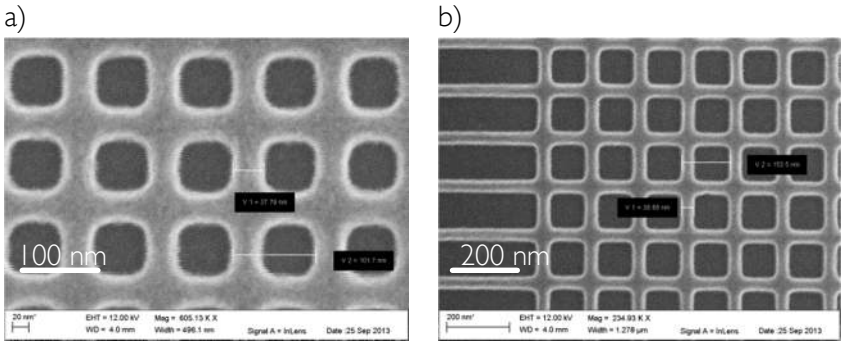

Figure 3.33. Tests with 50 nm linewidth grids. a) SEM image of a grid with a nominal linewidth of 50 nm and a pitch size of 100 nm patterned with a dose of 10 mC /cm^2. The obtained linewidth and pitch were of around

38 nm and 101 nm, respectively. b) Grid with a nominal linewidth of 50 nm and 150 nm pitch size patterned with the same dose. In this case we obtained around 39 nm and 153 nm, respectively.

Lowering the pattern density (by increasing the pitch size and shrinking the linewidth) and consequently, reducing the proximity effect, allowed obtaining grids with linewidths in the order of 15 nm. Although being below the nominal size of the pattern, the structures seemed robust enough to act as a hard mask for etching the graphene. As an example, Figure 3.34 (corresponding to the SEM image in Figure 3.32-a) shows the profile of a structure from which we estimated an approximate thickness of 25 nm.

We measured the thickness in a parallel line array patterned at the edge of the grid, since the tightly packed lines only allowed the AFM tip to touch the substrate when scanning along the same direction as the lines. We were aware that performing the measurement in this area could lead to a slight underestimation of the thickness, since the parallel line arrays had received a lower effective dose, due to a lower proximity effect when compared to the grids. As said before, we measured a thickness of about 25 nm. Taking into account that the thickness of the applied HSQ layer was originally of around 30 nm, we considered that the exposure had been adequate and a dose of around 16 mC/cm^2 was a good starting point for patterning these structures on graphene.

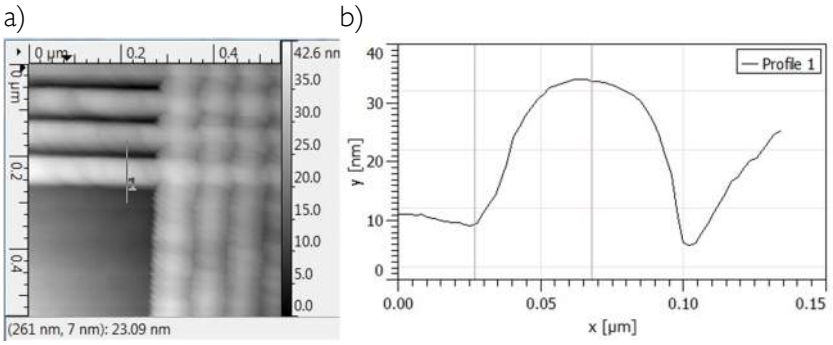

Figure 3.34. Topography image and profile of a patterned HSQ grid. a) AFM image of the lines at the edge of a grid in Figure 3.32-a. The tightly packed lines only allowed the AFM tip to touch the substrate when scanning along the longitudinal direction (therefore, the horizontal lines in this image are better defined than the vertical lines). The height of the developed HSQ structures was roughly around 25 nm for a dose of 16 mC /cm^2, as estimated from the profile in panel b).

We patterned the grids on the graphene flakes and on the silicon dioxide surface next to them, in order to see the influence of graphene in the exposure of the resist (Figure 3.35). After comparing both patterns we found that the effective dose was slightly higher on the bare oxide surface, as deduced from the difference in linewidth (28 nm, instead of 22 nm measured on top of graphene). We attributed the decrease in linewidth on

graphene to more efficient charge dissipation and to less scattering of electrons (since it is composed of lighter atoms).

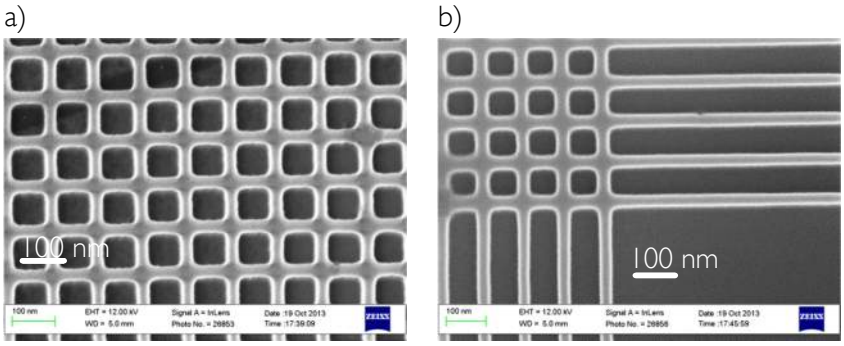

Figure 3.35. HSQ grids patterned on graphene and silicon dioxide. a) SEM images of grids with a nominal linewidth of 20 nm and a pitch size of 100 nm patterned with a dose of 16 mC /cm^2. The obtained linewidth and pitch were of around 22 nm and 97 nm, respectively. b) Grid with the same nominal dimensions patterned on silicon dioxide surface next to the graphene flake. A linewidth of 26 nm and a pitch size of 98 nm were obtained.

We noticed that in general, the HSQ grids did not seem to attach to the graphene surface as tightly as to silicon dioxide, especially in the corners (Figure 3.36). The edges of the grids appeared to detach during the developing process. We supposed that the attachment became stronger once the surface was dried after the developing, although we did not do any test to determine the degree of adhesion.

In order to hold the HSQ structures as tightly as possible to the graphene, we extended the edges of the grids beyond the inter-electrode area and attached them either to the surrounding silicon dioxide or to the previously patterned gold electrodes, as shown in the devices of Figure 3.37.

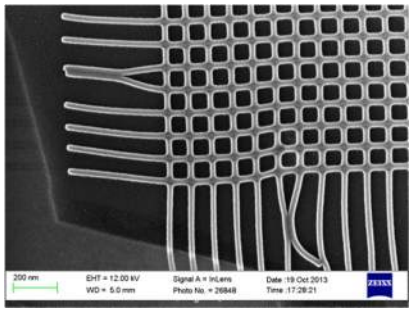

Figure 3.36. HSQ on graphene flakes: adhesion problems. a) SEM image of a HSQ grid patterned on a graphene flake. The corner of the grid had been detached from the graphene at some point during the developing process.

After the grids had been patterned on the selected graphene flakes as explained along this section, the resultant devices comprised two superposed lithographic layers. The first one consisted of metallic electrodes for electrical contact of the graphene and the second one was formed of HSQ structures covering the area between the electrodes (Figure 3.37).

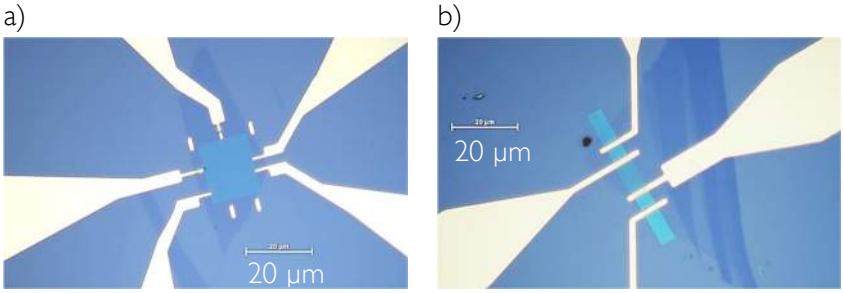

Figure 3.37. Devices patterned on top of graphene flakes in two lithography steps. Optical microscopy images of devices consisting of metallic electrodes for electrical contact of the graphene flake and HSQ nanostructured grids (seen as a square shaped pattern in the area between the electrodes).

Electrical measurements and Raman spectroscopy performed in the obtained devices accounted for the charge transport and structural properties of the graphene flakes after two lithographic processes (Figure 3.38).

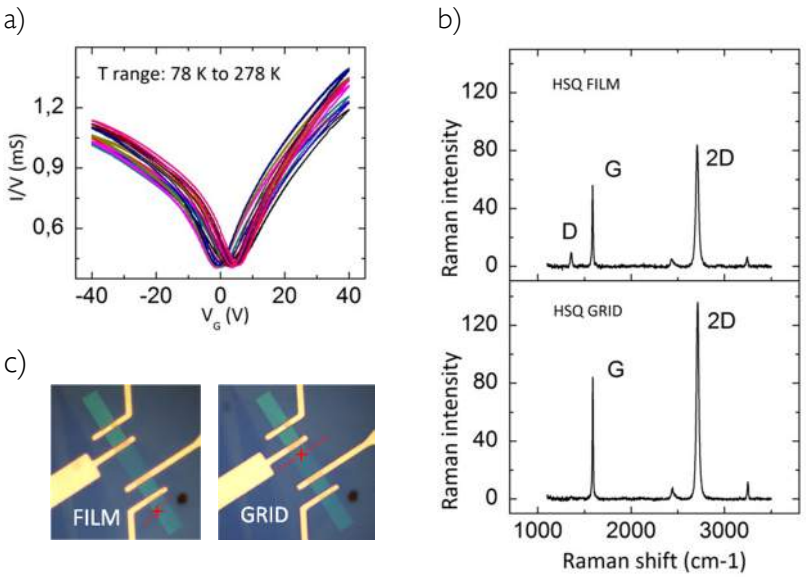

Figure 3.38. Characterisation of devices after lithography. a) Conductance (I/V) versus gate voltage curves at different temperatures corresponding to the device in Figure 3.13 (recorded at an applied source drain bias of 3 mV). b) Raman spectra of the graphene recorded in areas covered by a continuous HSQ film and below the HSQ grid. c) Optical microscopy images showing the spots at which the Raman spectra were recorded.

The conductance of the devices was measured in a four point configuration, using the doped silicon substrate as a back gate. The obtained data must only be used for guidance, since at this stage the current could circulate through the graphene sheet around the HSQ patterned area (see Figure 3.37 b). The aim of these measurements was to ensure the correct operation of the fabricated devices and to check the quality of the graphene (regarding to a massive doping or the appearance of defects) before performing the pattern transfer by reactive ion etching (RIE).

A drain voltage of 3 mV was applied while sweeping the gate (V_G) from 40V to -40V (subsequently performing a sweep in the opposite sense, -40V to 40V) at temperatures ranging from 78 K to 278 K. The relatively small hysteresis when changing the direction of the gate voltage sweeps and the small variation with temperature indicated a low density of defects. In fact, defects are reported to generate variable range hopping mechanism and thus, significant temperature dependence [16]. Moreover, the proximity of the charge neutrality point to V_G=0 meant that the doping level of the graphene was relatively low. These observations were confirmed by the Raman spectra recorded in different areas of the same device.

The Raman spectra were measured directly through the HSQ, since it did not give any signal in this range of the spectrum. Two sets of measurements were performed, in order to compare the areas underneath the continuous film of HSQ and the ones below a patterned HSQ grid. The images in Figure 3.38 c show the spots at which the two measurements in Figure 3.38 b were recorded. When comparing the spectra, the most remarkable result was the absence of the D peak (only active in the presence of defects in the graphene sheet) in the area under the HSQ grids, while it was present (although it was not very intense) in the area fully covered by HSQ. The lack of defects under the grid was consistent with the negligible temperature dependence of transport charateristics of the samples. Moreover, the G peak (around 1590 cm^{-1}) was close to the theoretical position corresponding to a graphene sheet with no doping (1585 cm^{-1}) in both measured areas. This fact was consistent with the conclusions of the electrical measurements, which indicated the charge neutrality point to be close to zero [17,18].

3.4.3.4. Reactive ion etching

The structures patterned on HSQ were used as a hard mask for etching the graphene flakes. We employed a recipe for reactive ion etching (RIE) that had previously been optimized in the Nanocarbon Group. This RIE recipe had been conceived for selectively etching single layer graphene flakes (Table 3.18). The images in Figure 3.39 show a single layer graphene flake before and after RIE. We observe that a fragment of double layer

graphene (such as the bent corner of a flake seen as a darker area in Figure 3.39-b and -d) remained after the RIE treatment, while the single layer flake was completely etched.

Table 3.18. Conditions for RIE of single layer graphene flakes

P_{BASE} (mbar)	O_2 flow (sccm)	Ar flow (sccm)	Power (W)	Time (s)
1	45	5	20	17

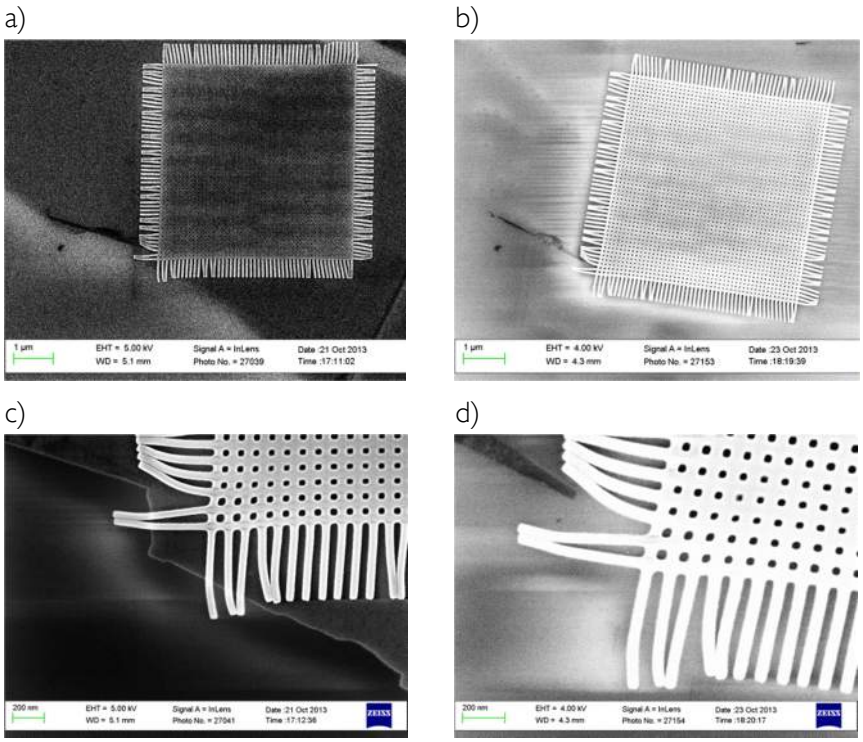

Figure 3.39. RIE on single layer graphene flakes. SEM images of single layer graphene flakes with a grid-like HSQ structure patterned on top. a) and b) show a graphene flake before and after RIE. The optimised RIE recipe selectively etches graphene monolayers, while thicker layers are preserved, such as the bent edge of the flake (therefore, a double layer) situated near the left bottom corner of the grid (seen as a darker area). c) and d) are higher magnification images of a) and b) in which we can better observe that the double layer of graphene (darker part) remains after RIE.

The electrical measurements were repeated after the RIE. However, no electrical current was getting through the patterned graphene. A possible explanation for this was that the etching treatment might have affected the graphene, laterally penetrating below the lines that formed the HSQ grid and damaging to some extent the areas near the edges. Thus, a few nanometres of lateral damage would be enough for interrupting the conduction path in the structures with smallest linewidth (~10-15 nm). On the other hand, adhesion

problems of the HSQ structures on graphene could have led to a direct and more extensive damage of the graphene flake.

This step would require further optimisation. On one hand, adjusting the conditions of RIE for obtaining a more stable etching rate would probably make the process more controllable and reproducible. On the other hand, performing etching tests and electrical measurements with HSQ masks of bigger linewidth (in the order of 100 nm, or bigger) would also be necessary in order to determine the extent of the damage produced by RIE in the graphene below the HSQ grids. Additionally, we should do a control tests with a mask consisting of a continuous square of exposed HSQ, covering all the area between the electrodes. If this last test gives a negative result, we could think that the RIE affects the graphene directly through the HSQ mask and that it would be necessary to increase its thickness.

3.4.4. Summary: general procedure for EBL on exfoliated graphene flakes

The the preparation of silicon wafers with physically exfoliated graphene flakes for EBL is summarised inTable 3.19.

Table 3.19. Preparation of graphene flakes on silicon wafers for EBL

STEP	PROCEDURE
1) Substrate cleaning	Dehidration and cleaning of 4" silicon wafers (with 300 nm SiO_2 coating and pre-patterned gold index marks): -Baking for 30 minutes at 200°C in a hot plate. -Plasma ashing for 10 minutes at 400 W power, O_2/N_2 gas flow of 200/50 sccm and P = 0.7 mbar.
2) Graphene exfoliation	-Cleaving of graphite crystal by repeatedly applying pressure and lifting it over the surface of blue tape, covering an area equivalent to a 4" wafer. -Cover the exfoliated flakes with another piece of blue tape and apply gentle and uniform pressure with a manual roller.
3) Graphene transfer	-Detach both halves of blue tape from each other and immediately apply them on top of freshly cleaned (and still hot) surface of a wafer, pressing with the manual roller. -Wait until the wafers cool down and place them on a hot plate at 50 °C. After around 15 seconds, peel off the blue tape slowly.
4) Graphene detection	-Imaging of the whole wafer surface in a microscope with a motorized stage. -Calculation of the optical contrast by subtraction of the background RGB indexes to the ones corresponding to a single layer graphene flake. -Graphene detection by analysis of the optical contrast in the RGB channels of the captured images (using home-made software, property of DTU).
5) Selective cleaning	-Manual striping of the unwanted flakes by adhesive tape under the optical microscope.

The following table compiles all the necessary steps for patterning electrodes on graphene flakes.

Table 3.20. General procedure proposed for EBL on graphene flakes

STEP	PROCEDURE
1) Resist processing	Application of 25 PMMA 15% (bottom layer) and 996 PMMA 2% (top layer): Spin coating at 4000 rpm during 1 minute, followed by 1 minute baking in a hot plate at 195°C (for each layer).
2) Conductive coating	Thermal evaporation of 15 nm aluminum at a rate of 5 Å/s
3) e-beam exposure	Exposure with a current of 60 nA (corresponding to an aperture of 200 μm and an acceleration voltage of 100 kV). Utilised dose: 1200 $\mu C/cm^2$.
4) Al Etching	Immersion in MF-CD26 for 1 minute, followed by immersion in flowing DIW bath for 2 minutes and drying with a nitrogen gun.
5) Developing	Immersion in MIBK/IPA 1:3 for 90 seconds followed by immersion in IPA for 2 minutes and drying with a nitrogen gun.
6) Metal deposition	Electron beam evaporation of 2 nm Ti (adhesion layer) followed by 30 nm of Au at a base pressure of 10^{-6} mbar and a rate of 0.5 Å/s.
7) Lift-off	-Immersion in acetone for around 5 minutes for removing most of the metal. Keep immersed overnight in 300 ml of clean acetone. Further cleaning of PMMA residues by warming up the acetone to 40 °C for 2 hours. -Rinse with milli-Q water and IPA (immerse for 30 seconds in each). Dry the wafer on a hot plate at 50 °C for 3 minutes.

Table 3.21 summarises the procedure for patterning nanostructures with HSQ on graphene flakes.

Table 3.21. General procedure for patterning with HSQ on graphene flakes

STEP	PROCEDURE
1) Resist processing	Application of HSQ (2% in MIBK) by spin coating at 3000 rpm for 1 minute; baking for 3 minutes in a hot plate at 100 °C and another 3 minutes at 200 °C.
2) Conductive coating	Thermal evaporation of 15 nm Al at a rate of 5 Å/s
3) e-beam exposure	Exposure with a current of 2 nA (corresponding to an aperture of 60 μm and an acceleration voltage of 100 kV). Utilised dose: in the order of 10000 $\mu C/cm^2$.
4) Al Etching	Immersion in MF-CD26 for 1 minute and immediately transfer the wafer into a petry dish with clean MF-CD26 for developing.
5) Developing	Immersion in MF-CD26 for 90 seconds, followed by immersion in a flowing bath of DIW for 4 minutes and drying with a nitrogen gun.

3.5. Exploring the limits of the EBL process

After establishing general protocols for performing EBL on diverse substrates, we wanted to test our capability for obtaining nanodevices with extremely small features. The tests were done using uniquely the nanolithography facilities in CIC nanoGUNE and working at the conditions that are commonly used in our equipment (10 to 20 kV of acceleration voltage and 10 μm aperture).

We must keep in mind that the ultimate resolution of EBL does not only depend on the lithographic equipment itself, but on the whole process, including the properties of the employed materials as well as the specific working conditions utilised. Therefore, the achievements obtained in a particular case might not be directly transferred to any other pattern and material.

The strategies for obtaining the smallest possible features with EBL can differ considerably depending if we want to pattern isolated objects (meaning that the distance between adjacent features is much larger than the size of the features themselves) or structures surrounded with a high pattern density (such as nanogaps and nanoconstrictions). The main difference between the two mentioned cases is the proximity effect, which is much more pronounced in the latter.

Nanogaps and nanoconstrictions

We focused our efforts in the patterning of electrodes with nanogap separations and metallic wires with nanoconstrictions, which are relevant for the current research lines of our group.

Obtaining electrodes with a separation in the order of 10 nm by EBL is feasible if the required aspect ratio is relatively low. Note that in this context the aspect ratio (W/L) refers to the quantity obtained when dividing the width (W) of the inter-electrode channel by its length (L). High aspect ratio nanogaps are desirable for many applications, such as field-effect transistors (FETs). Having an inter-electrode channel with high aspect ratio results in a higher drain current and in principle, better signal to noise ratio. At the same time, the effect of fringe currents in the transistors is also reduced. However, achieving such structures by conventional EBL is very challenging [19].

The study of nanoconstrictions has also attracted considerable attention. The charge transport in nanoconstrictions enters the ballistic regime and shows conductance quantization when the cross section of the conducting path is sufficiently decreased. Nanoconstrictions are interesting systems for studying magnetoresistance effects or the motion and pinning of magnetic domain walls, among other examples.

3.5.1. Substrate preparation

The lithography was carried out employing 950 PMMA A2, which is the most widely used positive resist in our group for high resolution patterning. As a general rule, the resist thickness should be in the order of the smallest feature size of the designed pattern (the lateral resolution of PMMA is around a third of the film thickness, according to the specifications). For this reason, we used a resist solution of 2% concentration, which gave a film thickness of around 50 nm after spin coating.

We chose highly doped silicon with 150 nm of thermal oxide and Si_3N_4 membranes of 15 nm thickness as substrates for our tests. They were both of great interest for the current research in our group and besides, they were expected to interact very differently with the incident electron beam, as we will explain in the next section.

The PMMA was applied onto the clean silicon substrates by spin coating at 4000 rpm for 1 minute, followed by baking at 195°C in a hot plate for another minute. In the case of Si_3N_4 membranes the PMMA was applied at 3500 rpm in a special spin coater and the baking was done in an oven at 170ºC for an hour (further details in section 3.3.1).

3.5.2. Exposure and developing

We designed a test pattern consisting of electrode pairs with aspect ratios ranging from 1 to 20, with a minimum inter-electrode distance of 30 nm. On the other hand, we included in the design several electrodes with tapering tips forming bowtie shaped constrictions of different lengths.

The targeted inter-electrode distances were smaller than the designed ones. However, we expected to reduce them substantially throughout the lithographic process, mainly due to the proximity effect. As explained in chapter 2 (section 2.1.3), the proximity effect (PE) causes variations in the shape and size of the patterned features with respect to the designed ones. In the case of closely separated electrodes the PE leads to round-shaped electrode tips and irregular inter-electrode gaps (the distance between electrodes in much shorter in the centre than in the corners). This effect increases in the case of nanogaps with large aspect ratio.

Decreasing the resist thickness and increasing the beam acceleration voltage reduces the PE. Hence, we used a 950 PMMA A2 film of 50 nm in thickness and we exposed with an acceleration voltage of 20 kV. Due to the simplicity of our design, we did not perform computational calculations for proximity effect correction. Instead of that, we patterned a large array of test structures with different doses and inter-feature distances, in order to determine the conditions that best matched our requirements.

The two chosen substrates had very different characteristics. The silicon substrates had a thickness of 500 µm, while the Si_3N_4 membranes were just 15 nm thick. The extremely thin Si_3N_4 membranes were practically transparent to the electron beam, producing a much lower backscattering of electrons. Therefore, we expected to see a considerable reduction of the proximity effect in the membranes in comparison to the thicker silicon substrates, resulting in a higher resolution.

The column conditions and exposure parameters were set as shown in Table 3.22 and Table 3.23. Exposure doses ranging from 275 to 450 µC/cm^2 were tested on silicon and 400 to 900 µC /cm^2 on Si_3N_4.

Table 3.22. Column conditions for electron beam exposure. The value of the beam current is approximate, since it can fluctuate depending on the state of the filament.

Acceleration voltage (kV)	Aperture size (µm)	I_{BEAM} (pA)	Write field size (µm)
20	10	~40	100

Table 3.23. Exposure parameters

I_{BEAM} (pA)	Exposure dose (µC/cm^2)	Step size (nm)	Dwell time (ns)	Beam speed (mm/s)
~35	100	3.2	~279	~10.77

The developing was done by 1 minute immersion in MIBK/IPA 1:3, followed by an IPA rinse and drying with a nitrogen flow.

3.5.3. Metal deposition and lift-off

We deposited 20 nm of palladium or gold (with a titanium adhesion layer for the latter) on the patterned resist (see Table 3.24).

Table 3.24. Metal deposition on test samples. Note that the abbreviations *MS* and *EB* in the second column stand for magnetron sputtering and electron beam evaporation, respectively.

Substrate	Metal	Technique	P_{BASE} (mbar)	$P_{DEPOSITION}$ (mbar)	P_{Ar} (mbar)	Rate (Å/s)	Thickness (nm)
Si_3N_4	Pd	MS	6×10^{-8}	-	6×10^{-3}	2.5	20
Si/SiO_2	Pd	EB	1×10^{-6}	9×10^{-6}	-	0.7	20
Si/SiO_2	Ti	EB	3×10^{-9}	1×10^{-8}	-	0.1	3
Si/SiO_2	Au	EB	3×10^{-9}	1×10^{-7}	-	0.2	20

In the case of palladium deposition by magnetron sputtering, the samples were perpendicularly oriented towards the metal target. We performed the evaporation of titanium and gold in an ultrahigh vacuum evaporator (*Createc*) where both metals had the same evaporation angle with respect to the samples (the exact angle was unknown, although it should be fairly close to perpendicular). The electron beam evaporation of palladium was carried out in the *Oerlikon* evaporator, keeping the samples at a fixed angle (close to perpendicular) from the source. In all the cases, the metal deposition was carried out without rotation of the sample holder. The samples were placed with the longest direction of the patterned features pointing towards the metal evaporation sources, as explained in section 3.3.4.

The samples were immersed in acetone for around 2 hours for lifting off the metallised resist mask. The removal of metal was assisted by squirting acetone on the patterned surface. Afterwards, the silicon samples were transferred into clean acetone and subjected to around 10 seconds of ultrasounds to help removing the smallest bits of metal from the nanogaps. The Si_3N_4 membranes were spared from this last step, due to their brittleness. Finally, all the samples were rinsed with IPA and dried with a nitrogen gun.

3.5.4. Summary of the results

The results achieved with single layer of PMMA and thinner metallic layers might not always be applicable to the designed experiments. For instance, performing certain electrical measurements implies having robust structures as electrodes, in order to avoid electromigration and excessive heating when the electrical current is circulating.

Structures on Si/SiO_2 substrates

On one hand we performed tests in which we used palladium for metallisation. The choice of palladium can be advantageous because in general it does not need an adhesion layer, which eliminates the possible mismatching between multiple layers deposited with slightly different evaporation angles. This mismatching can lead to short circuits between closely spaced electrodes.

In a first test we deposited 20 nm of palladium by sputtering. Unlike it happens with directional metal evaporation techniques, the deposition by sputtering is fairly homogeneous in all directions. This means that the whole surface of the patterned resist (including the areas that are not directly facing the sputtering source) are covered with the metal. This can sometimes lead to inefficient lift-off and to the formation of some metal fringes that could produce shortcuts between structures (Figure 3.40).

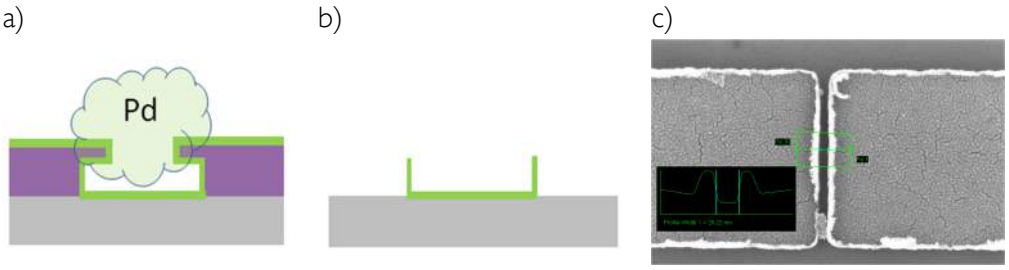

Figure 3.40. Disadvantages of metal deposition by sputtering. a) Sketch representing the deposition of palladium by sputtering. b) Metal deposited on the resist walls leads to fringes remaining after lift-off. c) Example of an electrical shortcut occasioned by the remaining metallic fringes.

The next images show the smallest inter-electrode gaps achieved in the tests with sputtered palladium on silicon substrates (Figure 3.41). Gaps with minimum sizes below 20 nm could only be achieved with a relatively low aspect ratio. We could hardly decrease the gap size below 27 nm with the maximum aspect ratio employed in our tests (namely, W/L=18.5). The smallest constrictions were of around 20 nm width. The obtained data are compiled in Table 3.26.

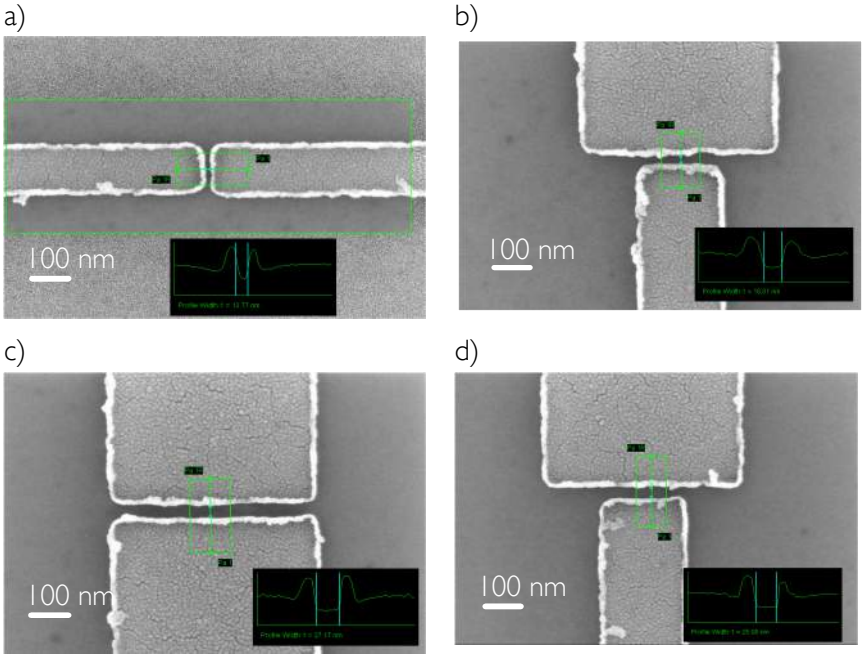

Figure 3.41. Nanogap electrodes with sputtered palladium on silicon substrates. The deposited palladium layer had a thickness of 20 nm. The data extracted from the images is shown in the following table.

Table 3.25. Nanogaps with sputtered palladium on silicon. The tabulated values have been extracted from the SEM images in Figure 3.41 and are therefore approximate.

Image	Nominal gap (nm)	Measured gap (nm)	Aspect ratio (W/L)
a)	35	14	9.5
b)	45	18	11.7
c)	55	27	18.5
d)	50	25	8.4

Regarding to nanoconstrictions, the minimum width obtained with sputtered palladium was of around 30 nm, as observed in the following figure.

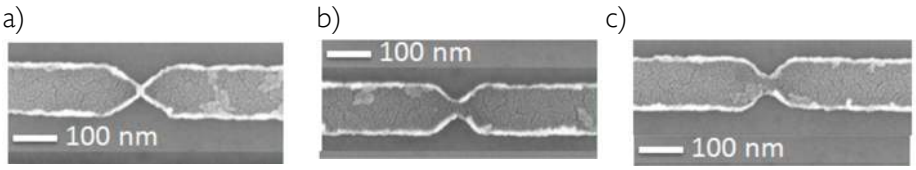

Figure 3.42. Palladium nanowires with nanoconstrictions on silicon substrates. Structures with different shapes made of 20 nm sputtered palladium, where the constrictions had a minimum width of around 30 nm.

The next test structures consisted of 20 nm of gold with a titanium adhesion layer of 3 nm (both metals were deposited by electron beam evaporation). Smaller gaps and higher aspect ratios could be obtained in comparison to the tests with sputtered palladium. As an example, the minimum gap size was of around 12 nm, with an aspect ratio of 43.9. On the other hand, the edges of the structures were more regular and free of fringes, unlike in the case of sputtered metal.

The images in Figure 3.43 show some of the smallest inter-electrode gaps we achieved. Note that the titanium layer extends about 5 nm along the whole perimeter of the gold layer. We attributed this homogeneous mismatching to the diffusion of metal below the slightly undercut profile in the single layer of PMMA, since the evaporation angle in the utilised equipment was the same for both metals. We speculate that the thin titanium adhesion layer would penetrate more easily below the undercut, while the growth of the larger gold grains in this reduced space would be hindered to some extent. The results are summarised in Table 3.26.

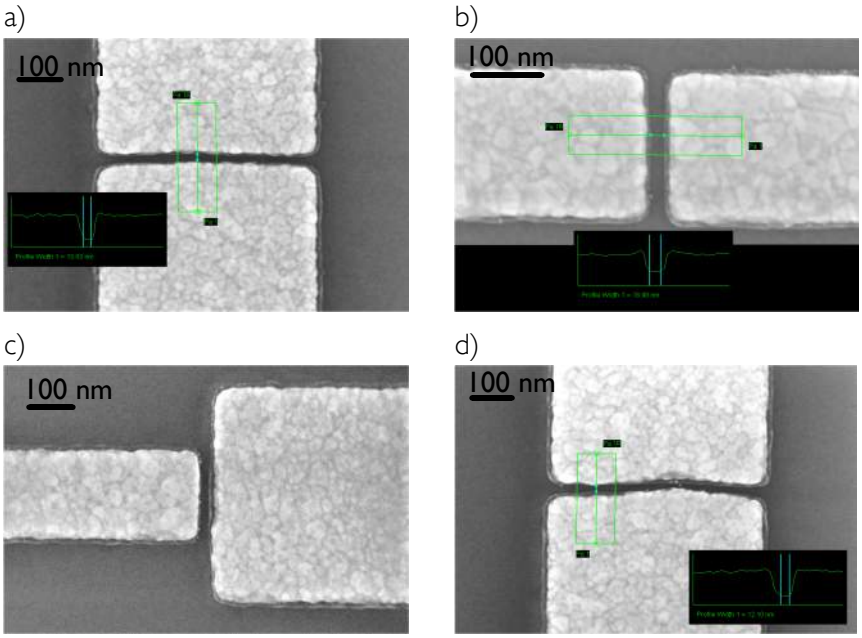

Figure 3.43. Nanogap electrodes with evaporated gold on silicon substrates. The deposited gold layer had a thickness of 20 nm (on top of a titanium adhesion layer of 3 nm). The data extracted from the images is shown in Table 3.26.

Table 3.26. Nanogaps with evaporated gold on silicon. The tabulated values have been extracted from SEM images and are therefore approximate.

Image	Nominal gap (nm)	Measured gap (nm)	Aspect ratio (W/L)
a)	50	13	41.0
b)	50	19	11.6
c)	50	19	12.3
d)	50	12	43.9

We also patterned gold wires with nanometric constrictions of different shapes. We found that gold could have difficulties to grow on the constricted features, while the titanium adhesion layer could uniformly cover the same area (Figure 3.44-a and -b). We attributed this behaviour to the tendency of gold to grow in islands (the so-called columnar growth), which might preferably nucleate outside the constricted areas, forming larger grains. We improved the results by thermal evaporation and depositing a thicker layer of gold (of around 40 nm) as shown in Figure 3.44-c. A double layer of PMMA (950 PMMA A2 on top of 495 PMMA A2, with a total thickness of 100 nm) had to be used in this last case, in order to enable lifting-off the thicker deposited gold layer. We obtained minimum constriction widths of around 20 nm with these conditions, as observed in Figure 3.44 c.

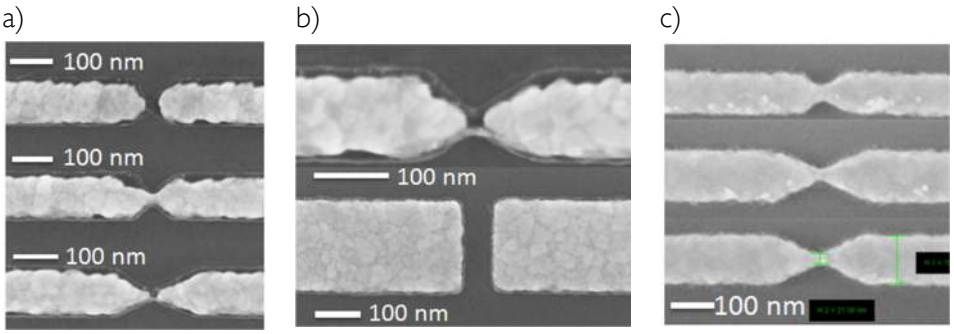

Figure 3.44. Gold nanoconstrictions on silicon. a) SEM images exemplifying the occasional difficulties for the growth of gold into constrictions. The structures consist of 3 nm of titanium and 20 nm of gold onto silicon substrates. b) Image of a similar structure at a higher magnification compared to a structure without constriction patterned on the same chip (the exposure dose was 355 μC/cm^2 in both cases). The gold grains did not grow in the constriction, while the titanium adhesion layer filled the whole patterned structure uniformly (observed as a line surrounding all the perimeter). c) Similar structures obtained after patterning on double layer PMMA and depositing 40 nm of thermally evaporated gold. We measured a minimum constriction width of around 20 nm, which is the smallest one we have been able to achieve in all our experiments.

In the case of nanoconstrictions we found that the main limitation for obtaining extremely small structures was the metal deposition step. In the case of very directional deposition methods, such as electron beam evaporation, shadow masking effects often lead to open gaps instead of constrictions. This could be corrected by an adequate evaporation angle, although it might be difficult to control depending on the utilised equipment. The shadow masking effects should be less pronounced when decreasing the resit thickness, since the aspect ratio of the patterned features was also reduced (in this case referring to the thickness of the resist layer divided by the width of the pattern). The lateral resolution capability of PMMA is roughly a third of the film thickness (according to the specifications), which in our case should be of around 17 nm. Therefore, the obtained structures are close to the achievable resolution limit.

We concluded that the best method for patterning extremely narrow constrictions and nanogaps is mostly limited by the metal deposition step. The deposition method and deposited metal thickness can change the results dramatically. Regarding to the fabrication of nanogaps, sputtering resulted in general in a lower yield when compared to metal deposition by more directional methods, due to the appearance of fringes that can lead to electrical shortcuts. However, directional methods could have the disadvantage of causing undesired shadow masking effects and mismatching of the different deposited layers, if the evaporation angle is too different and the sample is not rotated. Rotating the sample during metal evaporation yields a more uniform filling of the pattern and less mismatching but it can lead to metallic fringes around the structures, similar to the ones observed with sputtering (Figure 3.41).

Structures on Si_3N_4 membranes

We deposited 20 nm of palladium by electron beam evaporation in the test structures patterned on Si_3N_4 membranes. We decided to use evaporation instead of sputtering because it yielded the highest aspect ratio nanogaps in the tests on silicon substrates and it also avoided the formation of fringes.

Unlike the structures patterned on silicon, the ones patterned on the 15 nm thin membranes did not deviate so much from the nominal sizes. For instance, the structure in Figure 3.45-a and -b (patterned on silicon with an exposure dose of 450 $\mu C/cm^2$) is composed of two elements of 300 nm x 200 nm and inter-feature gap of 50 nm (nominal sizes). In the case of silicon substrates the size increases around a10% in length and 15% in width, while the gap shrinks down to 19 nm. In contrast, the structure in Figure 3.45-c is patterned on a Si_3N_4 membrane (with an exposure dose of 800 $\mu C/cm^2$). In this case it only increases around a 6% in width and height, while the gap decreases to around 33 nm The smaller deviation in size is due to a lower proximity effect in the case of thin membranes. Similarly, patterning the same design with 10 or 20 kV acceleration voltage on Si_3N_4 membranes yields similar results (regarding shape and size of the structures), because the backscattering of electrons (and therefore, their contribution to proximity effect), is negligible in both cases.

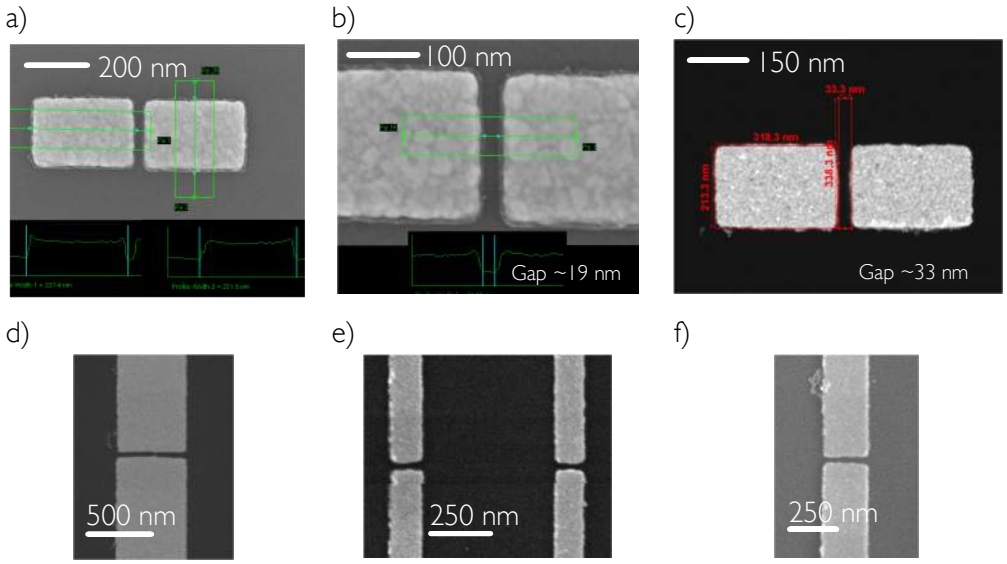

Figure 3.45. Comparison of structures on silicon and Si_3N_4 membranes. a), b) Structures patterned on silicon substrates with an exposure dose of 450 $\mu C/cm^2$ (consisting on 20 nm of electron beam evaporated gold with 3 nm titanium for adhesion). c) Same design patterned on a 15 nm thick Si_3N_4 membrane with a dose of 800 $\mu C/cm^2$ (consisting on 20 nm of electron beam evaporated palladium). d), e) and f) are different examples of the same type of palladium structures on membranes. The data extracted from these images is shown in Table 3.27.

Table 3.27. Nanogaps fabricated with sputtered palladium on Si_3N_4 membranes. The tabulated values have been extracted from SEM images in Figure 3.45 and are therefore approximate.

Image	Nominal gap (nm)	Measured gap (nm)	Aspect ratio (W/L)
c)	50	33	6.5
d)	45	36	21.3
e)	40/35	37/21	3.6/5.8
f)	40	29	7.8

Regarding to the patterned nanoconstrictions, we obtained a minimum width ranging from 20 to 30 nm depending on the size of the bowtie-shaped structure, as observed in Figure 3.46. The smallest cross-sections were obtained in the constrictions with the longest and most pointy tapers (as in Figure 3.46-b or d-). The edges were well defined and unlike in the case of some gold nanoconstrictions (Figure 3.44), we did not find problems for the deposition of metal in the constricted area, probably due to differences in the growth mechanism of the metallic grains.

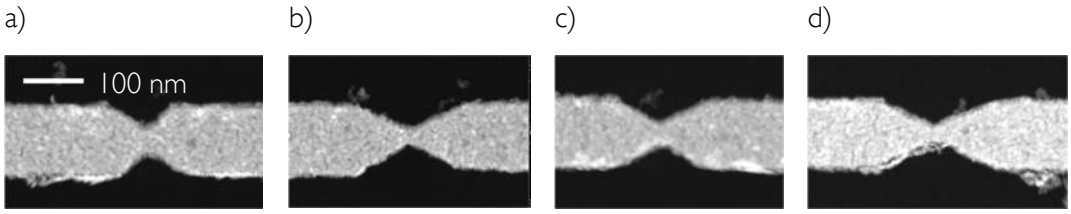

Figure 3.46. Palladium nanoconstrictions on Si_3N_4 membranes. Bowtie shaped structures with slightly different shapes consisting of 20 nm of evaporated palladium. The constrictions obtained in figures a) to d) had a minimum width of around 35 nm, 30 nm, 31 nm and 20 nm, respectively. Note that the scale bar (in panel a) is the same for all structures. We attributed their irregular shape to the uneven growth of the metal grains in the constricted area, same as observed in Figure 3.44.

After analysing all the results obtained, we conclude with the following general observations:

- The pattern transfer constitutes the main limitation for obtaining the smallest possible feature sizes with our current lithographic procedure. Problems in metal growth or lift-off processes decrease the resolution capability of a given resist.
- Some metals may present difficulties to grow homogeneously in constricted areas. For instance, we had difficulties for the homogeneous growth of a 20 nm gold layer by electron beam evaporation, leading to open gaps instead of constricted nanowires. We relate this effect to the mechanism for grain growth at those particular deposition conditions.
- In general, similar gap sizes and aspect ratios are obtained by metal evaporation or sputtering. However, in the former case the edges of the nanostructures are better defined and have fewer metallic fringes after lift-off.
- Performing the exposure with 10 kV or 20 kV did not change appreciably the results on the thin membranes, since unlike it happens in conventional substrates, the back scattering of electrons (which is the principal responsible for proximity effect), is low for both beam conditions.
- The obtained sizes in thin silicon nitride membranes are closer to the nominal values, due to the lower proximity effect presented by these substrates. However, the achieved feature sizes were still limited by the pattern transfer by lift-off, same as in the case of silicon substrates.

3.6. Conclusions

- Patterning on insulating substrates

In the present work, we implemented the use of a thin gold coating on top of the resist for charge dissipation purposes. After optimizing the thickness of the charge dissipation layer (~ 1.3 nm), we could perform the electron beam exposure adequately, obtaining nanostructures with well-defined features by metal deposition and lift-off. As a practical example, we present closely separated electrodes for the study of resistive memories in oxides (HfO_2) and several nanostructures for plasmonics applications patterned by EBL on CaF_2 insulating substrates. The smallest obtained feature size and inter-feature distance were in the order of 100 nm and 30 nm, respectively.

In conclusion, the protocol proposed for general use with insulating substrates was successfully adapted for these particular cases, yielding well defined and functional structures.

- Patterning on electron transparent Si_3N_4membranes

We successfully patterned metallic structures on Si_3N_4 membranes of 15 nm, 30 nm and 50 nm thicknesses. As expected, patterning on the thinnest membranes was more challenging, since apart from being extremely fragile, their surface was mechanically less stable and more wrinkled.

Robust metallic frames were patterned in a previous lithography step in order to confer mechanical stability and favour heat dissipation in the case of 15 nm membranes. The procedure used for this lithography step was essentially the same as for patterning the nanostructures, although a higher beam current was employed.

- Patterning on graphene flakes

We patterned nanostructures on graphene flakes by performing EBL at 100 kV acceleration voltage and employing a high resolution negative resist (namely, HSQ). We obtained grid-like structures with minimum linewidth ranging from 10 to 20 nm. The fabricated devices were meant for subtractive patterning of the graphene by RIE using the HSQ nanostructures as a hard mask. The aim was creating a gap in the band structure of graphene.

We carried out the fabrication process at a whole wafer scale, starting from graphene exfoliation, followed by patterning of electrical contacts with good reproducibility and minimum damage for the graphene flakes and finishing with the patterning of nanostructures with HSQ on top of the flakes. Electrical measurements of the obtained devices demonstrated that the graphene conserved its intrinsic properties after two

lithography steps. The next step (transferring the pattern to graphene by RIE) is currently under optimisation at the Nanocarbon Group of the Technical University of Denmark.

- Resolution capability experiments

We performed a few experiments in order to determine the smallest feature sizes achievable with our in-house lithographic resources and our typical working conditions. Thus we performed the tests on silicon (highly doped, with 150 nm oxide coating) and on Si_3N_4 membranes of 15 nm thickness, working at moderate beam energies (20 kV) and using a high resolution positive resist (950 PMMA A2).

We patterned closely separated electrodes with the smallest possible inter-electrode gaps and metallic nanoconstrictions with the smallest possible cross section. We concluded that the main limitation for scaling down the patterned feature size was the pattern transfer by metal deposition and lift-off. The smallest gaps and narrowest constrictions achievable were of around 15 nm and 20 nm, respectively, working at 20 kV acceleration voltage and an aperture of 10µm, without making use of computational tools for proximity effect correction.

3.7. References

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Chapter 4

In this chapter we explore the possibilities of electromigration as a fabrication technique for nanostructures that are difficult to obtain by conventional lithography.

We obtain different types of nanostructures that are already integrated into devices by combining electron beam lithography and electromigration at low temperatures. We perform electromigration experiments in different metals and alloys, such as palladium, gold, copper, nickel, platinum, permalloy and palladium-nickel. The electrical characterisation is carried out in situ, revealing signatures of nanoconstrictions, tunnelling gaps and single electron transport in the obtained devices.

In section 4.1 we introduce the basic concepts of electromigration, including the variables that affect the process and the most common strategies employed for the fabrication of nanostructures by this technique. In section 4.2 and 4.3 we explain the procedure employed for the fabrication of devices by electron beam lithography and electromigration. Finally, the main conclusions of the chapter are compiled in section 4.4.

4. Fabrication of devices beyond the limits of electron beam lithography

The capability of nanofabrication for research applications is always ahead of the one for industrial manufacturing in terms of the minimum feature size of the produced devices. This happens because more innovative (although usually less reliable) fabrication strategies are employed for research applications.

The constant miniaturization of integrated circuit (IC) components and the demand for adequate platforms for the Characterisation of materials at the molecular level are some of the driving forces of this research field. Some applications imply contacting a nano-object (e.g., a nanoparticle, a molecule or a nanotube) to suitable metallic electrodes, which is a necessary prerequisite for studying its electronic transport properties [1-2]. Such metallic contacts can sometimes be patterned by well-established nanofabrication techniques such as electron beam lithography (EBL) or focused ion/electron beam induced deposition (FIBID/FEBID) [3-4]. Recent advances in instrumentation, such as the appearance of the helium ion microscope (HIM) in the market or the use of resists based on block co-polymers have allowed patterning smaller feature sizes [5]. However, most of these techniques are inadequate when the final applications require devices with inter-electrode

distances of the order of 1 nm, which is the case in the field of single molecule electronics [6-7].

Novel fabrication strategies often involve the combination of conventional lithography with alternative techniques [8, 9], as explained in Chapter 1 (Section 1.2.2). In this chapter we explore the possibilities of electromigration for pushing the device fabrication beyond the limits of electron beam lithography. Our aim was to obtain devices with different nanostructures as their active element, which could be used in multiple nanoelectronics applications, from ballistic transport to electrodes for molecular electronic devices.

4.1. Electromigration; from reliability issue to nanofabrication technique

Electromigration has been one of the main reasons for the failure of contacts and interconnects in integrated circuits. The phenomenon basically consists on the atomic motion in a metal under the influence of an applied electric field. This diffusion of mass within the solid metal leads to the formation of voids and accumulation of material at different places. The first reports on electromigration date to 1861[10] but it was not intensively studied until a century later, when it started to be technologically relevant [11].

The migration or movement of metallic ions is driven by the energy and momentum transferred by the constant collisions with the incoming electrons. Increasing the electrical current density speeds up the failure of the material by electromigration. Hence, it became a major reliability issue in the constantly shrinking components of integrated circuits.

Even if it still continues being an issue, in the last decades electromigration has also found a practical application as a novel nanofabrication technique. It has mainly been employed for transforming metallic nanowires into electrodes separated by gaps of a few nanometres. This allowed building single molecule transistors (SMT), for which the use of electromigration was considered a breakthrough in the field of nanoelectronics [12,13].

Most conveniently, the newly obtained nanostructures are already contacted by electrodes, which allow performing their electrical charaterization without further manipulation. Electromigration could constitute a simple strategy for the fabrication of nanodevices, if it was not for a major drawback: its low yield. Employing feedback-controlled techniques can lead to certain degree of control, although the outcome of this technique is practically statistical, especially in those experiments that aim at contacting single molecules. The formation of SMTs by electromigration has typically less than a 10 % success rate. In contrast, some groups have reported a yield of around 90% in the formation of bare tunneling nanogaps [9].

In this section we give a simple description of the electromigration phenomena and we refer to literature for further information [14, 15]. We then focus on the strategies that

have been developed in order to exploit electromigration as a fabrication technique [12, 13].

4.1.1. Electromigration in thin metallic wires

When an electric current circulates through a conducting wire, there are several forces acting on the individual metallic ions. In a simplified picture we can distinguish two main components: First, the electrostatic force exerted by the electrical field (F_{FIELD}) and second, the so-called electron wind (F_{WIND}), which is occasioned by the momentum transfer between conduction electrons and the metallic ions in the crystal lattice [15] (see Figure 4.1). The F_{FIELD} component becomes negligible compared to the F_{WIND}, since the positive metallic ions are mostly shielded by the conduction electrons in the metallic structure. As a result, the metallic ions are dragged by the electron wind, mostly along the grain boundaries. This mass flux creates local depletions and accumulations of atoms, leading to the nucleation of voids and hillocks. Sites with inhomogeneities in the microstructure, temperature or geometry are more likely to nucleate these voids and accumulations.

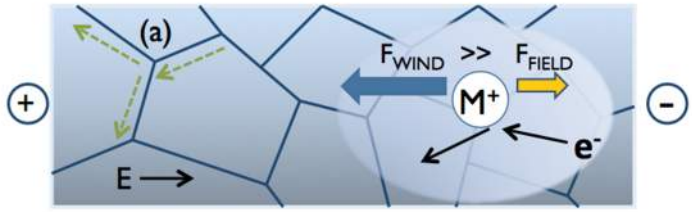

Figure 4.1. Schematic picture of the interior of a metallic nanowire during the electromigration process. The imbalance between the forces F_{WIND} and F_{FIELD} that act on the individual metallic ions (M^+) lead to their displacement towards the anode. The green dashed arrows in (a) represent the direction of the mass flux along several grain boundaries. Voids and accumulations of atoms are likely to appear when reaching divergence sites, such as the grain boundary "triple points" in which several grains join.

Electromigration is triggered when a critical current density (J_C) is reached within the nanowires. When J_C is of the order of 10^{12} A/m^2 F_{WIND} becomes strong enough to displace the metallic ions. The current density is related to the critical current (I_C) via the nanowire cross-section (A) by the relation $J_C = I_C / A$. At the same time, the critical voltage (V_C) at which electromigration takes place is determined by the product of I_C and the total resistance of the device (R_{TOTAL}); $V_C = I_C \times R_{TOTAL}$. We note that R_{TOTAL} is the sum of the nanowire resistance (R_{NW}) and the resistance in series with it (R_S); thus, $R_{TOTAL} = R_{NW} + R_S$. Changing the value of R_S is a common strategy for tuning the breaking conditions (Figure 4.2), which have a strong influence in the size and morphology of the created nanostructures [19-21].

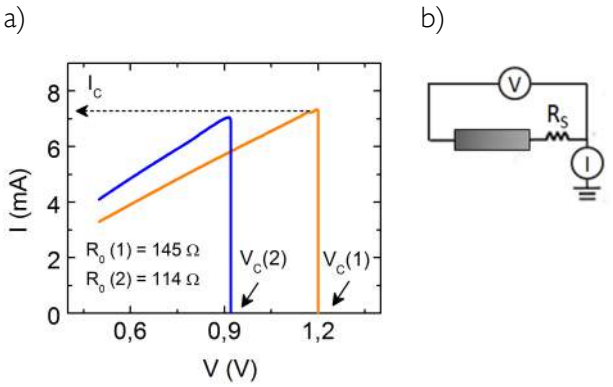

Figure 4.2. Tuning the conditions at the onset of electromigration of metallic nanowires. a) Graph displaying the measured current as a function of voltage I(V) in two nanowires during electromigration. The nanowires have an ohmic behaviour when we start increasing the applied voltage. The starting point of electromigration is marked by an abrupt decrease of the measured current, indicating that the nanowire cross-section is rapidly decreasing. At this point we measure the critical current (I_C, defined by the nanowire cross-section) and the critical voltage (V_C), which can be tuned by changing the total resistance of the device, as shown in the graph. b) Schematics of the experimental setup for electromigration experiments, where the resistance of the circuit and contact pads (R_S) is added in series to that of the nanowires.

The susceptibility to electromigration of polycrystalline wires can be quantified by the mean time to failure (MTTF), given by Black's equation [16]:

$$MTTF = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{K_B \cdot T}\right)$$

This empirical model describes the endurance of a conducting wire under certain temperature and current conditions. Black's equation shows all the variables that directly affect the electromigration process; namely, the current density (J), the temperature (T) and the activation energy of the material for electromigration (E_a). *A* is a material constant related to structural, electrical and diffusional properties of the conductor and *n* is a scaling factor (usually n = 2, according to literature) [17].

In the following points we briefly explain the effects of these variables in electromigration:

- High temperatures enhance the mobility of metallic ions and increase the chances of failure by electromigration. The circulation of a high current density through a thin conductor can result in a considerable increase of temperature by Joule heating. Therefore, having efficient heat dissipation increases the MTTF for a given current density [18]. Related to this, we must be aware that the thermal conductivity of the surrounding medium can play an important role in the electromigration processes.

- Independently of the experimental conditions or the dimensions of the circuit components, some metals (for instance, aluminium or silver) are more likely to experience electromigration than others. The susceptibility to electromigration is related to the activation energy needed for the process. For instance, we can find values between 0.81 and 0.88 eV for gold [19], 0.4 to 0.8 eV for aluminium [20], and 0.8 to 2.3 eV for copper [15]. The activation energy is different for surface diffusion, diffusion in the bulk or grain boundary diffusion of the metal atoms.
- The diffusion of metallic ions in thin films takes place mostly through the grain boundaries. When the cross-section of a nanowire approaches the size of the metallic grains, small variations in the distribution of the grain boundaries can affect critically the diffusion of matter. This partly explains the randomness of the electromigration process and the difficulty for having a complete control of the results.[15]

4.1.2. Feedback controlled processes

The migration or movement of metal ions has certain inertia, especially at higher temperatures, where the mobility of ions is enhanced. This means that the process goes on for a while even after the applied voltage is supressed. Thus, having a method for an early detection and response at the onset of electromigration is very important. This is achieved by employing programs with adequate feedback algorithms for controlling the process [9].

The controlling program basically continuously monitors the charge transport across the nanowires and stops the electromigration when the input variables fulfil a given condition. We prepared a LabVIEW program that comprised the following three conditions that could be independently used for stopping the process:

- 1st condition. If the measured current changed above a certain percentage during the applied voltage ramp (typically below a10 %) the voltage was reset to zero and the process was stopped. A new voltage ramp was started after allowing a relaxation time of around 5 seconds.
- 2nd condition. If the current changed above a certain value in the last measured N data points (typically around 1% change in N = 40), the voltage was reset to zero and the process was equally stopped. A new voltage ramp was started after a relaxation time of 5 seconds.
- 3rd condition. If the resistance (or conductance) of the device reached a set limit, the voltage was reset to zero and the process was brought to an end. We note that the low bias resistance of the resulting devices usually differs from the value set as a limit

in the controlling program, which is measured at higher voltages (typically in the order of V ~1V).

These three conditions (represented in Figure 4.3) could be independently activated, depending on the requirements of each experiment. The first condition was soon discarded and substituted by the second one, since it allowed for a better control. Note that the parameters mentioned above have been optimized for our particular experimental conditions (in general, T< 10K and the voltage ramped up at a rate of 3 to 6 mV/s).

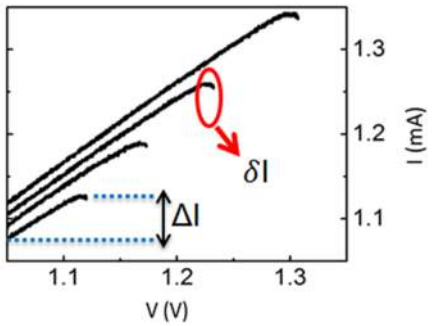

Figure 4.3. Stop conditions in feedback controlled electromigration processes. Representation of the 1st stop condition (blue dotted lines) and the 2nd stop condition (red circle) utilised by the feedback algorithm of our LabView program for controlling the electromigration process. Essentially, they both reset the voltage to zero depending on the amount of change measured in the current across the device. The 1st condition takes into account the amount it changes from the beginning of each voltage ramp and the 2nd condition only monitors a determined amount of the last measured data points.

4.1.3. Electromigration strategies

Apart from using different feedback algorithms, we can employ several strategies for electromigration. On one hand, we can distinguish those involving self-breaking or active breaking, depending on the absence or presence of an applied voltage. On the other hand, the most common methods among the active breaking processes consist on performing either a gradual electromigration or a continuous electromigration. We are going to explain briefly each case and more details will be given in the following sections:

- Active breaking. It refers to breaking metallic nanowires by applying a voltage across their two ends [21,22]. The process can be done gradually or in a continuous fashion.

  In a gradual electromigration experiment the voltage is applied in a series of increasing ramps. The process is controlled by limiting the extent to which the nanowires are broken in each voltage ramp and allowing a relaxation time after

each cycle. Instead, in a continuous electromigration process the nanowires are broken in a single voltage ramp. The electromigration is carried out in a continuous manner, stopping the process only when the target conductance or resistance is reached in the device.

- Self-breaking. The ability of certain metallic nanowires for "self-breaking" has been exploited by some research groups [23,24]. This is the case of gold or platinum nanowires, which continue to break down slowly even in the absence of an applied voltage, once they have been electromigrated to a certain point. The spontaneous breaking occurs due to the high mobility of the metal ions and the residual stress on the electromigrated few-atom constrictions. Electromigrated gold nanoconstrictions self-break at room temperature, while platinum needs higher temperatures (roughly, T = 400 K) [25]. In principle, the absence of bias voltage in the last breaking stage increases the probability of obtaining smaller gaps and avoids the formation of metallic clusters. In addition, it allows observing quantized conductance steps before the failure of the nanowires.
- Combined strategies. Actively pre-breaking the nanowires at a certain temperature and completing the electromigration process at the same or lower temperatures (either by self-breaking or by active breaking) is also a common practice. This strategy is useful when the voltage required for electromigration at low temperature is too high.

We performed gradual electromigration experiments in which the feedback mechanism stopped the breaking process according to the second and third stop conditions explained in section 4.1.2. Meanwhile, in the continuous electromigration experiments we only employed the third stop condition.

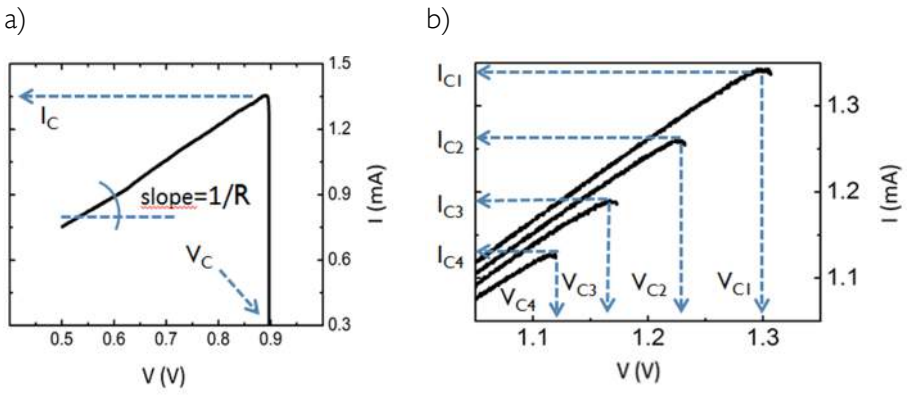

Figure 4.4. Different electromigration strategies for active breaking processes. a) Extraction of the critical current (I_C) and voltage (V_C) at the onset of electomigration in a continuous breaking process (in other words, using a

single voltage ramp). b) I_C and V_C values in the successive voltage ramps of a gradual electromigration process. The values of both parameters decrease as the cross-section of the nanowire is reduced.

4.2. First fabrication step: Patterning nanowires by electron beam lithography

First of all, we fabricated devices with adequate dimensions and shape for performing electromigration experiments.

Subjecting metals to high electrical current densities (in the order of 10^{12} A/m^2) induces electromigration. Thus, employing metallic wires of small cross-section allows achieving the necessary current density at relatively low voltages. Moreover, breaking a metallic nanowire by electromigration ideally yields a pair of closely separated nanoelectrodes, which could be used for electrically contacting nano-objects.

Based on the phenomenological description of electromigration given in Section 4.1 and the references found in literature [14-15], we have considered the following points when designing our devices:

- Inducing electromigration is harder (a higher current is needed) for a bigger nanowire cross-section
- A higher current density is needed for electromigration when the cross-section of the nanowires is smaller than the average size of the metallic grains. In this situation the grain boundaries are mostly perpendicular to the circulating current, which act as barriers that hinder the diffusion of material [26]. Usually, the electromigration in polycrystalline films occurs mostly along grain boundaries, since the activation energy is lower than the one for electromigration through the bulk of the grains.
- In general, increasing the length of the nanowires makes the process more difficult to control, since the heat dissipation is less efficient. An excessive thermal activation can speed up the diffusion of metal ions, making the process les controllable. It can also lead to partial melting of the material, which can destroy the work done during the electromigration process.
- Connecting the nanowires to large contact pads can be helpful to better control the electromigration process. On one hand, it favours an efficient heat dissipation and avoids an excessive thermal activation. At the same time, it helps reducing the total resistance in series along the device, which allows breaking the nanowires at lower voltages [18].

Electron beam lithography (EBL) has the necessary resolution for patterning metallic wires with nanometric cross-section. Hence, we chose this technique for fabricating our devices on top of a p-type silicon substrate covered by 150nm of thermally grown silicon

oxide. We exposed a double layer of polymethyl metacrylate (PMMA) resist, followed by metal deposition and lift-off (see the detailed procedure in Chapter 2). Each chip contained several devices consisting of a nanowire with a rectangular-planar geometry, which was contacted by a pair of triangle-shaped microscopic electrodes (see Figure 4.5). The as-produced devices showed linear I(V) characteristics.

We prepared devices employing different metals and alloys, as shown in Table 4.1. All the produced devices were cleaned with acetone and isopropyl alcohol immediately before the electromigration experiments. The gold and palladium devices were also subjected to an additional oxygen plasma treatment in order to get rid of all possible organic residues remaining from lithography. However, we also performed experiments skipping this last step, confirming that it did not affect the results. The plasma treatment was skipped in devices made of other metals, due to the risk of oxidation. All the devices were stored in inert atmosphere and they were used for electromigration experiements in a period of a few days after the lithography (especially those that were not composed of noble metals).

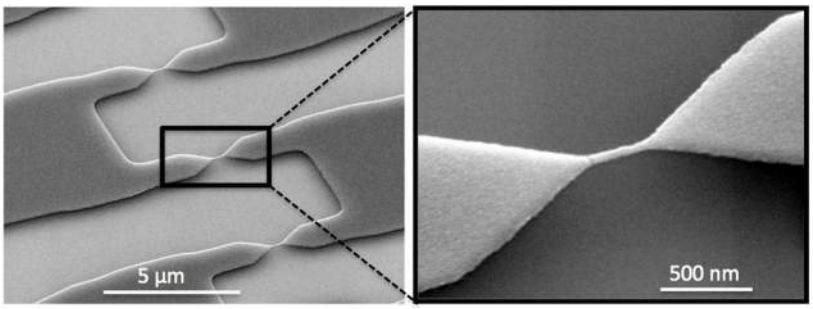

Figure 4.5. Scanning electron microscopy image of palladium devices on Si/SiO_2 substrate. Array of several devices on a chip, each consisting on a nanowire contacted by a pair of electrodes (only the microscopic part is shown). A closer image shows the detail of a nanowire contacted with the triangle-shaped ends of the microscopic electrodes.

Table 4.1. Nanowire dimensions and deposition methods utilised for different nanowire materials. a) Relation of utilised materials and nanowire dimensions. Note that the abbreviations for the deposition techniques listed in the table correspond to electron beam evaporation (EB), Thermal evaporation (TE), and magnetron sputtering (MS). The nanowire dimensions are approximate values, extracted from SEM images and X-ray reflectivity measurements. b) Deposition parameters utilised for each material in table a).

Nanowire material	Deposition technique	Nanowire cross-section: Thickness x width (nm^2)
Pd	MS	20 x 60 to 120
$Pd_{0.5}Ni_{0.5}$	MS	25 x 65
Ni	MS	25 x 65
Pt	MS	15 x110
Cu	TE	25 x 160
Py	EB	25 x 85
Ti/Au	EB/ TE	20 x 80 to 90

b)

Metal	Technique	P_{BASE} (mbar)	$P_{DEPOSITION}$ (mbar)	P_{Ar} (mbar)	Rate (Å/s)	Thickness (nm)
Pd	MS	3×10^{-6}	-	4×10^{-3}	2.5	25
$Pd_{0.5}Ni_{0.5}$	MS	$\sim 10^{-8}$	-	8×10^{-3}	1.6	25
Ni	MS	$\sim 10^{-8}$	-	8×10^{-3}	1.4	25
Pt	MS	$\sim 10^{-8}$	-	8×10^{-3}	1.3	10
Cu	TE	$\sim 5 \times 10^{-9}$	$\sim 3 \times 10^{-8}$	-	2	25
Py	EB	$\sim 4 \times 10^{-9}$	$\sim 2 \times 10^{-8}$	-	0.7	25
Ti	EB	$\sim 2 \times 10^{-6}$	$\sim 4 \times 10^{-6}$	-	0.4	1.2
Au	TE	$\sim 2 \times 10^{-6}$	$\sim 3 \times 10^{-6}$	-	0.8	20

4.3. Second fabrication step: Creating nanostructures by electromigration

Most of our electromigration experiments were carried out at low temperatures (ranging from T=1.8 K to T=10 K) in a liquid helium cryostat with 10 mTorr helium atmosphere. We only utilised active breaking techniques, which basically consisted on applying increasing voltage ramps while measuring the current across the devices in a two-wire configuration. We carried out a series of experiments employing different electromigration strategies, (see sections 4.1.1 to 4.1.3).

Regarding the studied materials, we mainly focused on palladium (Pd) and afterwards, we extended the experiments to palladium-nickel alloys ($Pd_{0.5}Ni_{0.5}$). We also performed a

few experiments with several other materials that have been more extensively studied in literature [9, 12-13], namely, gold (Au), nickel (Ni), copper (Cu), permalloy (Py or $Ni_{0.8}Fe_{0.2}$) and platinum (Pt).

4.3.1. Palladium devices

We performed a comparative study in which we tested different electromigration strategies in devices with palladium nanowires. All the experiments were done at a temperature of T= 4K.

Palladium is a chemically noble metal that has no effective magnetism in the bulk state. However, it has been reported to display size-dependent magnetism when it forms nanoparticles [22, 27]. There have been reports on unusual conductance features attributed to the onset of magnetization in bare Palladium nanojunctions [22], as well as predictions on the induction of surface ferromagnetism by strong electric fields [28]. All this characteristics make it a potentially interesting material for building nanostructures, since it might confer additional features to their charge transport [29-30].

It has been proved experimentally that the values of current and voltage at the onset of electromigration (I_C and V_C) are strongly related to the size and morphology of the created nanostructures [31-32]. Taking advantage of this fact, we performed a series of experiments in which V_C was varied with the purpose of obtaining devices with different characteristics. We fabricated devices with different designs for the contacts (Figure 4.6) in order to change the resistance in series with the nanowires (R_S). This resulted in the variation of V_C, which can greatly influence the outcome of the electromigration process (as explained in Section 4.1.1). Apart from this, we tested two different strategies in our experiments; continuous electromigration and gradual electromigration (described in Section 4.1.3).

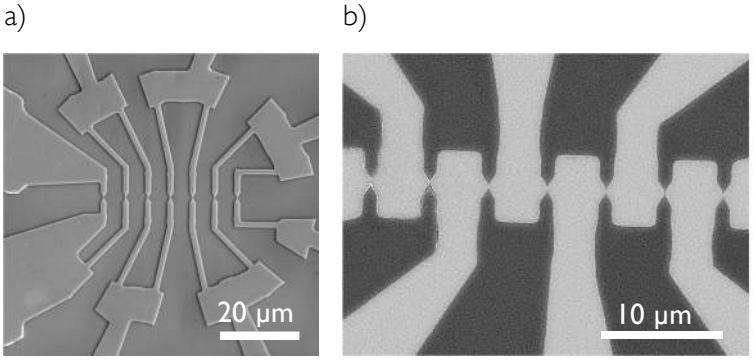

Figure 4.6. SEM images of microscopic electrodes used for contacting the nanowires. We usually had an array of seven nanowires in the same chip. Different designs were used for varying the resistance in series with the

nanowires (R_S), obtaining a total resistance that ranged from around 300 Ω to 2 kΩ. a) Thin and elongated electrodes result in a large R_S. Sometimes we introduced different types of electrodes in the same chip in order to make a direct comparison (the leftmost electrode in this image has a lower resistance than the other six). b) Short and wide electrodes (displaying a darker contrast than the substrate in this image) result in a lower R_S.

4.3.1.1. Strategy 1: Continuous electromigration

We carried out a feedback-controlled electromigration process by applying an increasing voltage ramp at a rate of 3 mV/s until the measured current dropped suddenly and a target resistance value was reached in each device.

In most cases the current measured across the devices dropped to a negligible value immediately after the onset of electromigration (Figure 4.7-a, curves 2 to 5). However, some devices experienced a first abrupt drop in current followed by a second stage, at which the current decreased in smaller random jumps (Figure 4.7-a, curve 1). Quantized conductance steps were often observed (Figure 4.7-b), indicating the formation of shrinking constrictions during the electromigration process.

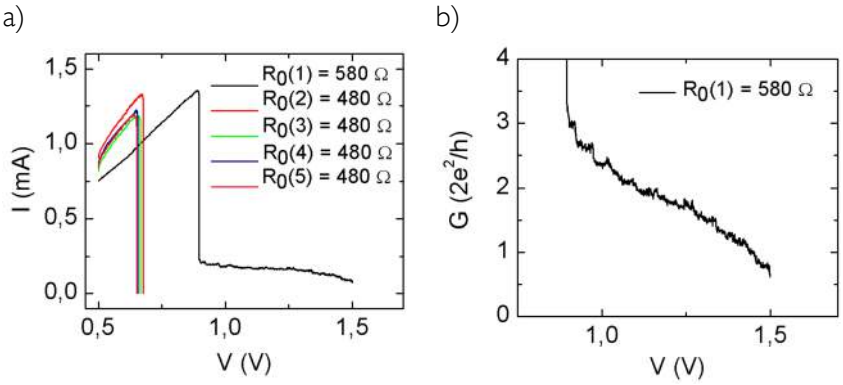

Figure 4.7. Continuous electromigration process in palladium nanowires. a) I(V) curves of five different devices belonging to the same chip are represented in the graph. In four cases the current increases linearly with the applied voltage, until the critical values at the onset of electromigration (V_C, I_C) are reached and the current drops abruptly. Having a similar resistance (R_0) and cross-section results in similar values of V_C and I_C for all four devices. However, the device with a higher initial resistance has the onset of electromigration at a higher V_C and besides, it shows two stages in the breaking process. b) Last stage of the electromigration process of the first device in panel a, represented in units of quantized conductance ($G_Q=2e^2/h$). Reminiscences of quantized conductance steps can be observed.

We note that when the nanowires break in two stages, the electromigration process can be stopped to electrically characterise the devices and afterwards, it can be resumed by applying a new voltage ramp. The new breaking cycle always continues exactly at the same voltage in which we stopped the previous cycle (see Figure 4.8), meaning that the geometry

of the breaking point does not experience important changes during the relaxation periods between voltage ramps [13].

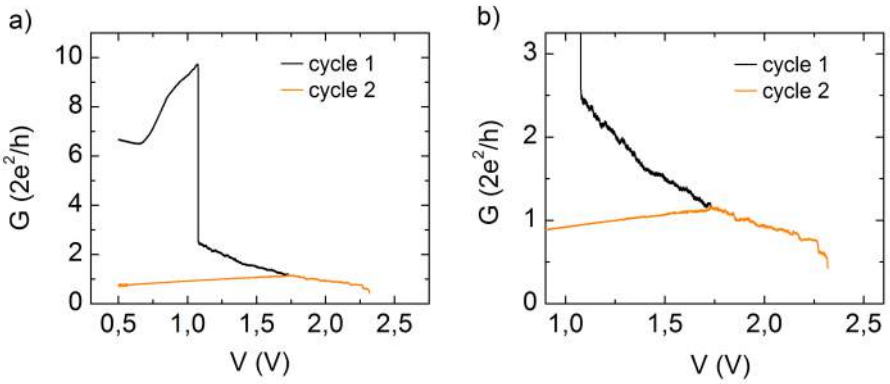

Figure 4.8. Electromigration of a palladium nanowire carried out in two cycles. a) Evolution of the conductance of a palladium device (represented in quantized units) during a continuous electromigration process. We observe two stages in the breaking process (same as in Figure 4.7, curve 1). At some point during the second stage, we stopped the process and reset the applied voltage to zero. Afterwards, we resumed the electromigration by starting a second ramp of increasing voltage. b) Zooming into the graph in a) shows that the second cycle continues exactly at the same voltage in which we stopped the first cycle.

As explained earlier, we fabricated by EBL devices that had a different resistance in series with the nanowires (R_S), resulting in a variation of the total initial resistance (R_0). We fabricated a total amount of around 200 palladium devices with nanowires, although it took some time until we found the adequate design and dimensions for performing our study. Around half of the fabricated devices were not suitable or simply broke down before carrying out any electromigration experiment. In most cases, the simultaneous failure of all the nanowires in the chip occurred due to electrostatic discharges during their manipulation, wire bonding, etc., even if we took precautions to avoid this as much as possible. In some other cases, the fabricated nanowires were too robust (the cross section was too big) and they required prohibitively high voltages for electromigration. This usually resulted in an excessive heating and finally, in the catastrophic failure of all the nanowires in the device.

In Figure 4.9-a we present a graph with the V_C and I_C measured at the onset of electromigration in 75 different devices. We divided the data into several intervals according to R_0 (represented with a different code as shown in the graph legend).

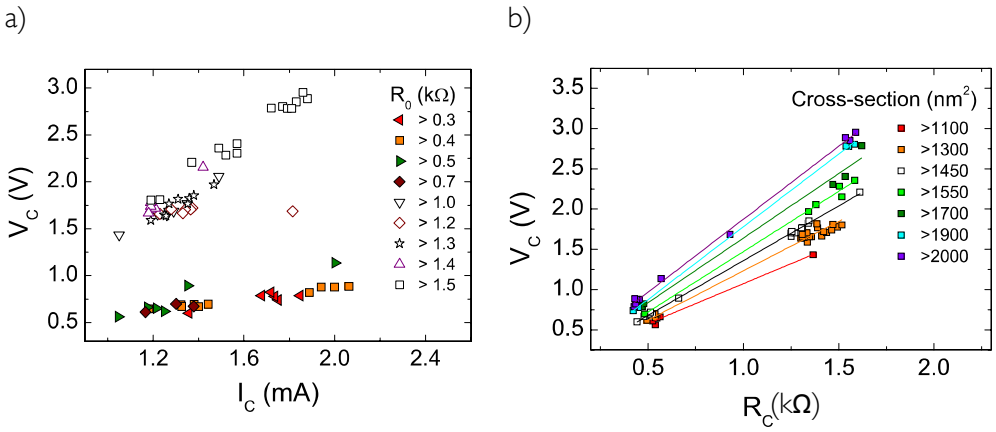

Figure 4.9. Experimental conditions at the onset of electromigration of palladium nanowires. a) Critical voltage and current (V_C, I_C) measured at the onset of electromigration of palladium nanowires in 75 devices. The initial total resistance of the devices (R_0, in kΩ) is divided into several ranges that are represented with a different code. The graph shows two distinct groups of data. b) Critical voltage (V_C) as a function of total device resistance at the onset of electromigration (R_C) corresponding to the data represented in panel a). The colour code represents different intervals in the cross-section of the nanowires. The data corresponding to nanowires with a similar cross-section fall in a straight line of slope equal to I_C.

The experimental data tend to form groups as a function of R_0, confirming that we can indeed tune the onset of electromigration by changing the total resistance of the devices. Through further analysis, we observe that the data gather into two distinct groups. This segregation could indicate the existence of a threshold R_0 value (approximately around 1 kΩ) dividing two different trends in electromigration. As observed in the graph, the onset of electromigration takes place at $V_C > 1.5$ V in devices with $R_0 > 1$ kΩ. Meanwhile, in devices with $R_0 < 0.7$ kΩ the electromigration starts approximately between $V_C = 0.5$ and 0.8 V.

Figure 4.9-b shows the critical voltage as a function of the device resistance at the onset of electromigration (R_C). The cross-sections of the corresponding nanowires have also been represented with a colour code in the same graph. The cross-sections were measured from electron microscopy images of the nanowires and x-ray reflectivity measurements of the thickness of thin palladium films deposited simultaneously with the nanowires. We observe that nanowires with a similar cross-section fall in straight lines with slope equal to their corresponding average I_C value (Figure 4.9 b). Table 4.2 displays the average J_C calculated for each group, according to the I_C extracted from the linear fittings to the data in Figure 4.9 b and their corresponding range of nanowire cross-section. The total average critical current density (J_C) we get from the values in table I is $(8.8\pm0.4)\times10^{11}$ A/m^2. According to literature, J_C should remain constant when the nanowire cross-section is bigger than the average grain size [26] (more details in Section 4.1.1).

Table 4.2. Experimental values of the average critical current density (J_C) of palladium nanowires and their corresponding cross-section range, extracted from the graph in figure 4.

Nanowire cross-section (nm^2)	>1100	>1300	>1450	>1550	>1700	>1900	>2000
J_C (A/m^2)/ 10^{11}	8.0	9.0	9.1	9.2	8.8	9.2	8.6

The charge transport characteristics shown in Figure 4.10 represent the general trend in devices belonging to each of the two distinct groups of data observed in Figure 4.9. The behaviour observed in Figure 4.10-a is a significant example from the group with R_0 < 0.7 kΩ, whereas the devices corresponding to panels b and c of the same figure belong to the group with R_0 > 1 kΩ. We conclude that the electromigration of nanowires resulted in devices with very different charge-transport regimes depending on the initial total resistance (R_0).

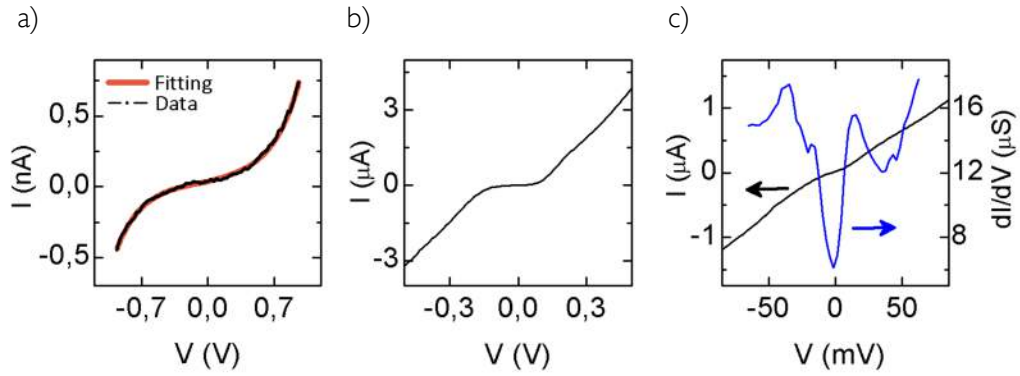

Figure 4.10. Electrical characterisation of palladium devices after electromigration. a) I(V) curve of a device with a final low-bias resistance of R ≈10 GΩ showing the typical characteristics of a tunnel junction. The fitted curve was calculated using the Simmons equation for tunneling current across an insulating barrier (vacuum, in this case). b) I(V) curve of a device in the Coulomb blockade state (R ≈1 MΩ), characterised by a plateau of negligible current in the zero bias region. c) I(V) curve of a device with a final resistance of R ≈100 kΩ, showing the characteristic steps of a metallic nanoconstriction. These features are more easily observed as peaks in the corresponding differential conductance curve (plotted in the same graph as dI/dV).

In general, we observe that in devices with R_0 < 0.7 kΩ the nanowires tend to break in a single step (observed as an abrupt current drop in Figure 4.7-a, curves 2 to 5). The obtained devices have a low bias resistance ranging from 100 MΩ to GΩ. For example, the graph in Figure 4.10-a (corresponding to a device with R ~10 GΩ) shows a non-linear current I(V) curve that fits with the characteristics of a tunnel barrier. We obtain a value of 1.6 ± 0.3 nm for the inter-electrode gap size by fitting this curve with the Simmons equation [33]. We attribute this behaviour to the formation of a bare inter-electrode nanogap. The charge transport takes place by tunnel effect in gaps < 2 nm, while gaps of

bigger size show negligible inter-electrode current and a resistance higher than about 100 GΩ.

Instead, the devices with R_0 >1 kΩ showed a different behaviour. In this case, most of the nanowires tend to break in two stages, consisting on a fist abrupt drop of the measured current and a subsequent slower decrease in random jumps (Figure 4.7-a, curve 1). In general, the low bias resistance in the obtained devices ranges from 100 kΩ to 10-100 MΩ, depending on the moment at which the process is stopped. We performed experiments setting different values of the final device resistance as a stop condition in the feedback algorithm (R_{LIMIT}), which gave as a result devices with different charge transport regimes. The observed transport characteristics ranged from slightly non-linear I(V) curves to a strong suppression of the low-bias conductance. For instance, when setting R_{LIMIT} between 4 and 13 kΩ we mainly obtained devices with slight steps in the measured I(V) curves (Figure 4.10-c), more clearly observed as peaks in the corresponding differential conductance curves. We interpreted these features as a possible signature of metallic nanoconstrictions. Instead, the graph in Figure 4.10-b shows a curve with a plateau of negligible current at low bias voltage, corresponding to a device in the Coulomb blockade state (obtained by setting $R_{LIMIT} \approx$ 20 to 40 kΩ).

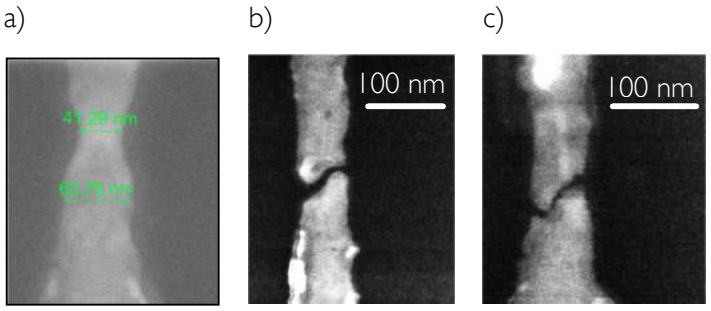

Figure 4.11. SEM images of nanostructures obtained by electromigration. a) We observed the formation of constrictions, such as the one starting to form in this partially electromigrated nanowire. We note that the constrictions are usually broken (probably by electrostatic discharges) when manipulating the devices or while bringing them back to room temperature. We also obtained electrodes with minimum separation distances ranging between 1 and 3 nm, as shown in b) and c). Usually the gap size can only be estimated by electrical characterisation.

When the nanowires break in two stages, the electromigration process can be stopped and further continued after electrical characterisation (as shown in Figure 4.8). This is especially advantageous for obtaining systems with Coulomb blockade, since it allows modifying the coupling between the active elements of the device until the desired conductance characteristics are achieved. We note that as a consequence of the non-linear charge transport, the low bias resistance of the obtained devices usually differs from the value of R_{LIMIT}, which is measured at higher voltages (typically, V >1V).

4.3.1.2. Strategy 2: Gradual electromigration

We carried out gradual electromigration experiments in palladium nanowires with the purpose of performing a mild breaking process of the nanowires and comparing the results to those of continuous electromigration (see 4.3.1.1).

The procedure consisted on applying several cycles of increasing voltage at a rate of 3 mV/s. Partial electromigration took place in each voltage ramp when J_C was reached (observed as a sudden drop of the measured current, as the nanowire cross-section decreased by a small amount). The applied voltage was reset to zero at the onset of electromigration in each cycle, in order to allow cooling and relaxation of the nanowire material. The process was controlled by activating the 2nd and 3rd conditions in the feedback algorithm (see 4.1.2). We could consider that the electromigration happened in three stages. In the first stage, the cross-section of the nanowires became smaller throughout several voltage ramps and V_C decreased accordingly. At a certain point the nanowires experienced a major break (second electromigration stage), after which the I(V) curves entered a different regime, similar to the one observed in some devices in section 4.3.1.1 (Figure 4.7a, curve 1). At this third stage we deactivated the 2nd stop condition of the controlling program and we kept increasing the voltage steadily, while the current (and the conductance) across the device decreased in jumps of random character. The voltage was reset to zero and the process was finished when a target resistance (R_{LIMIT}) was reached. We often observed quantization of the conductance at the last breaking stage of the nanowires (see Figure 4.12).

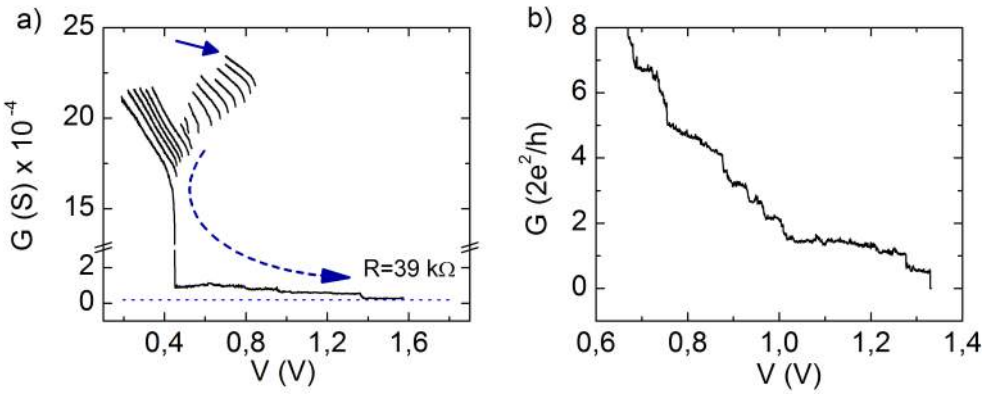

Figure 4.12, Evolution of the device conductance (G) during the electromigration process of a palladium nanowire. a) A series of increasing voltage (V) ramps are applied while the decrease of G in each V ramp is limited to a 1.5%. The solid arrow indicates the starting point of the first V ramp, while the dashed arrow shows the order of the successive V ramps throughout the process. A gradual decrease of G indicates that the cross-section of the nanowire is decreased after each V ramp. The nanowire suffers a major break (observed as a sharp jump in G) and it becomes unstable. Afterwards, G evolves in random jumps until a target G value

(corresponding to a device resistance of around 40 kΩ, indicated by a dotted line) is reached. b) Evolution of the conductance (G) in units of quantized conductance ($G_Q=2e^2/h$) in the last stage of the electromigration for a similar nanowire. The appearance of quantized conductance steps indicates the formation of a narrow constriction before the physical failure of the nanowire.

In general, the low bias resistance of the obtained devices (ranging from 100 kΩ to 10 - 100 MΩ) and the transport characteristics depended on the moment at which we stopped the process, same as it happened in the case of continuous electromigration of nanowires with R_0 >1kΩ (section 4.3.1.1). This similarity could indicate that in both cases the electromigration process is governed by the same mechanism. The transport features of the resulting devices consisted mainly on either I(V) curves with slightly non-linear shape or with pronounced plateaux of negligible conductance (as previously exemplified in Figure 4.10 b and c).

Breaking the nanowires gradually allows observing the evolution of the transport features throughout different electromigration cycles, as shown in Figure 4.13. In this example, a nanowire with ohmic behaviour is first transformed into a constriction (panel b) and the electromigration is continued until it enters a Coulomb blockade state (panel c and d).

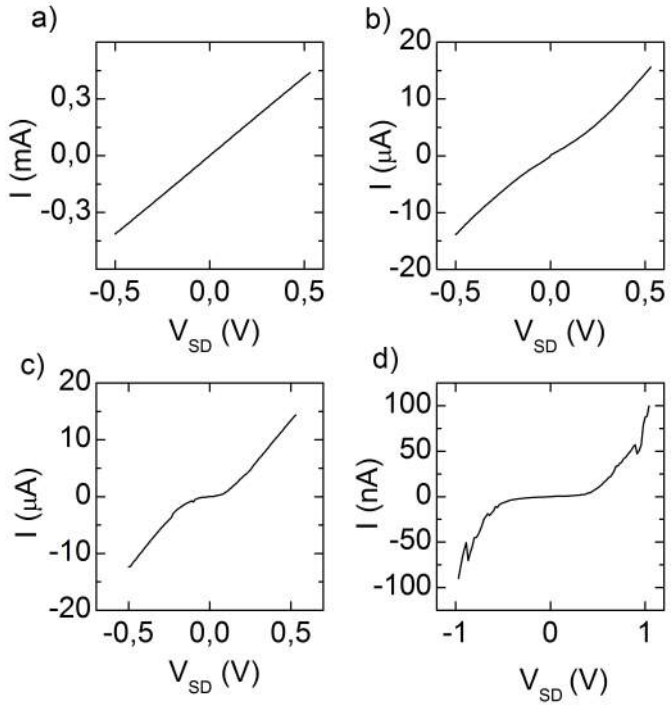

Figure 4.13. Evolution of the transport characteristics of a device throughout several electromigration cycles. a) The as-fabricated device has an ohmic behaviour. b) After the first electromigration cycle a low bias resistance

of 32 kΩ is achieved and the I(V) curve becomes slightly non-linear. c) After a second electromigration cycle the low bias resistance increases to 150 kΩ and a slight shoulder appears in the zero bias region, indicating a suppression of current. d) The device is further electromigrated until it develops a wide plateau of negligible current, indicative of the Coulomb blockade state. The low bias resistance is in the order of 100 MΩ.

We note the high yield (about a 90% of the tests) of devices with Coulomb blockade obtained in the gradual electromigration experiments, indicating the inclination of palladium to form quantum dots, probably in the shape of small clusters or nanoparticles trapped into nanogaps (further studied in Chapter 5).

Regarding the statistics of all our electromigration experiments in palladium (from a total amount of 75 tests), around 9% of the obtained devices contained nanogaps with a measurable tunnelling current, around 8% gave constrictions and 49% showed Coulomb blockade characteristics. This leaves a 33% of devices in which no measurable current was detected after the electromigration process.

4.3.2. Gold devices

Gold is the metal that has mostly been used in the fabrication of devices by electromigration [21-22, 26, 28, 34-35]. In fact, data regarding electromigration in palladium are scarce in literature, whereas we can find plenty of references to gold [12-13, 26, 32, 36-37, 38]. Thus, performing electromigration in gold nanowires allowed contrasting our results with literature and validating our experimental procedure.

Same as we did in the case of palladium devices, we explored the effect of changing the conditions at the onset of electromigration (mainly V_C) by varying the resistance in series with the nanowires (R_S). This was achieved both by means of lithography and by connecting a variable resistor to the circuit. We performed experiments setting different values of the final device resistance as a stop condition in the feedback algorithm (R_{LIMIT} between 13 kΩ and 15 kΩ). Apart from this, we tested both continuous electromigration and gradual electromigration strategies (following the same procedure as in 4.3.1.1 and 4.3.1.2).

As observed in the graph of Figure 4.14 most of the I_C values in our gold devices fall between 7 and 8.5 mA, which corresponds to an average critical current density (J_C) of around 4×10^{12} A/m^2 according to our nanowire dimensions. This values are in good agreement with literature [21-22, 26-28, 32], meaning that our experimental procedure is comparable to the one employed by other research groups. Therefore, we conclude that our findings in the electromigration of palladium nanowires are not related to any particularity of our experimental methods.

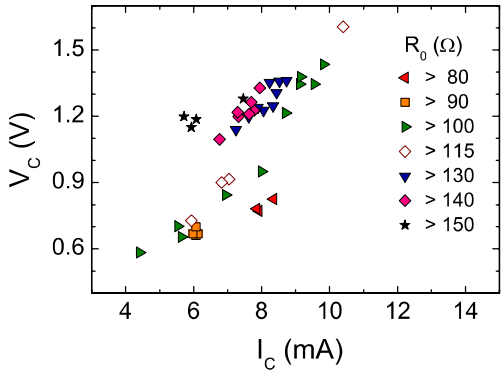

Figure 4.14. Experimental conditions at the onset of electromigration of gold nanowires. Critical voltage and current (V_C, I_C) measured at the onset of electromigration of the nanowires in 44 gold devices. The initial total resistance of the devices (R_0) in Ohm are represented with a different code.

We did not observe any segregation of data as a function of V_C or any other variable, neither any change in the evolution of the current during electromigration, as happened in the case of palladium devices. However, we cannot rule out the possibility of observing this behaviour in gold devices, since the range of different initial device resistance (R_0) explored in the experiments with gold is not comparable to the one explored in the case of palladium.

The characteristics of the resulting devices depended on the breaking conditions, as expected. In general, a higher V_C resulted in a higher resistance of the obtained devices, in agreement with literature. The number of experiments carried out with gold nanowires (44) might not be sufficient for a fully reliable statistics, although we could draw a few qualitative conclusions from them. We observed the following trend in the continuous electromigration experiments in gold devices:

- When V_C <1.1 V, the low bias resistance of the obtained devices ranged from 100 kΩ to 10 MΩ. Their charge transport was in general characterised by slightly non-linear I(V) curves (Figure 4.15-a). Occasionally, we also measured curves with a plateau of negligible conductance in the low bias region (mostly in devices with low bias resistance higher than about 1 MΩ), which is the characteristic signature of Coulomb blockade (Figure 4.15-b).
- When Vc >1.1 V, the low bias resistance increased beyond 10 MΩ after electromigration, often reaching values that were unmeasurable in practice. We ascribed this to the formation of larger (>3 nm) inter-electrode gaps. In some cases we also obtained devices with Coulomb blockade characteristics (Figure 4.15-b).

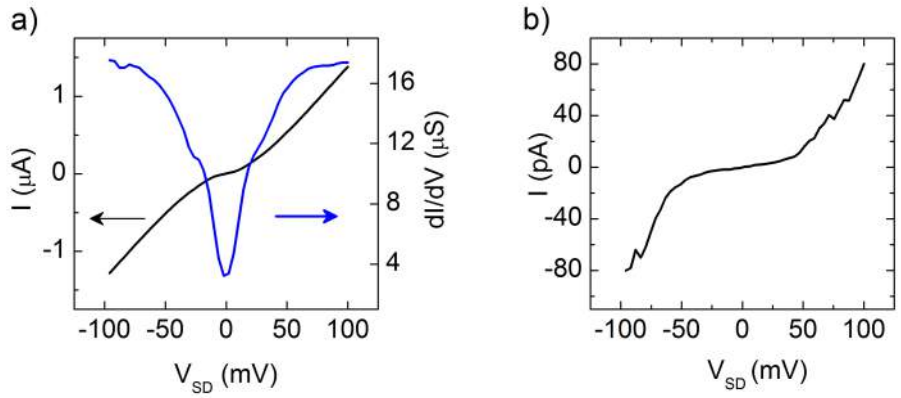

Figure 4.15. Electrical characterisation of electromigrated gold devices. a) Slightly non-linear I(V) curve and the corresponding derivative (dI/dV), possibly indicating the formation of a nanoconstriction. b) Coulomb blockade characteristics in a device with a low bias resistance of around 10 GΩ.

A few experiments were performed with the gradual electromigration strategy, for which we followed the same procedure utilised with palladium devices (Figure 4.16). Same as it happened in the case of palladium, we observed three distinct stages in the electromigration process. In the first stage, the cross-section of the nanowires became smaller throughout several voltage ramps and V_C decreased accordingly. At a certain point the nanowires experienced a major break (which we considered as a second electromigration stage) and finally, the measured I(V) curves entered a third stage, in which the current decreased in random jumps. We observed that once the constrictions were narrowed up to a certain point, gold nanowires could sometimes undergo grain rearrangements that led to a sudden decrease of resistance. Some nanowires experienced this "reconstruction" more than once during electromigration, and also during electrical characterisation.

Most of the electromigrated gold devices showed non-linear I(V) curves that were not stable during characterisation. Among all the obtained devices, only a few (around 20 %) contained nanogaps (Figure 4.16) and showed the signatures of a tunnel junction in their charge transport. However, the obtained nanostructures did not seem to be robust in general, since their properties were altered during electrical characterisation. The conductance measured in these devices either fell down to negligible values while recording I(V) curves or increased suddenly, as the conductive path was restored by a grain rearrangement (Figure 4.17). Some other devices (about 15 %) showed Coulomb blockade characteristics, although they were also quite unstable, same as it happened with the nanogaps.

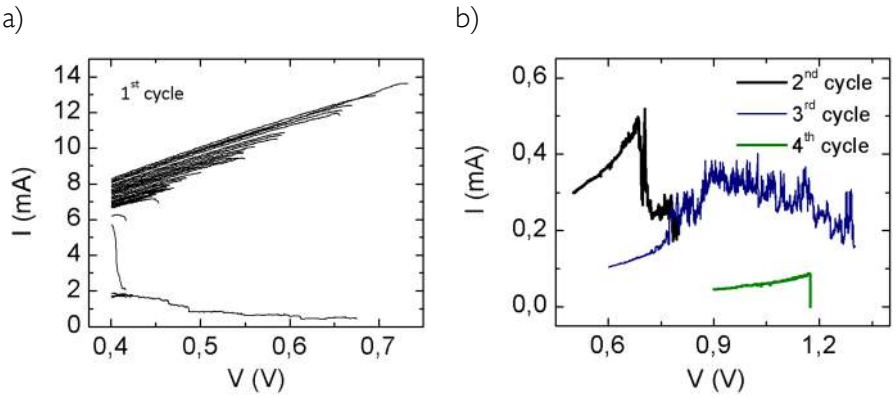

Figure 4.16. Gradual electromigration process of a gold nanowire. a) First cycle of the gradual electromigration process of a gold nanowire. The measured current decreases gradually throughout consecutive voltage ramps (corresponding to an increase of resistance from around 50 Ω to 65 Ω). At this point, there is a major break that gives way to a different behaviour, in which the current decreases in sudden jumps as the applied voltage is increased. b) 2nd to 4th cycles of electromigrtion of the same device, as an example of the random character of the I(V) curves in the last stage of electromigration.

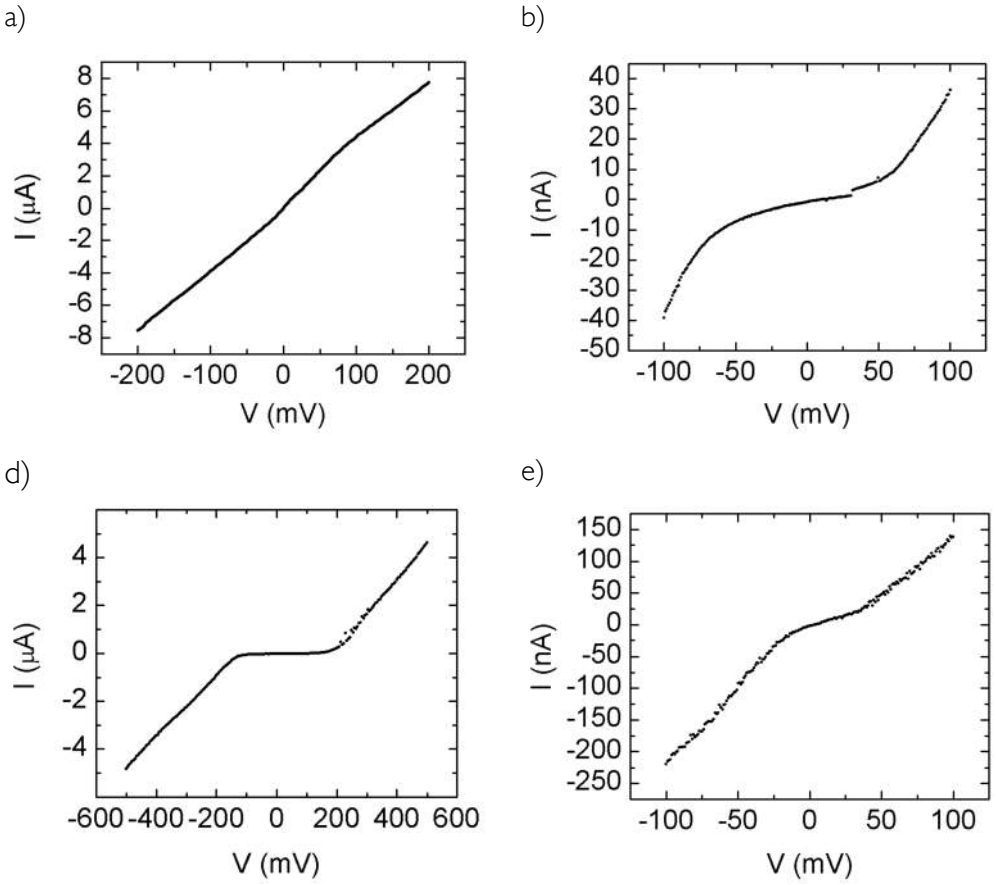

Figure 4.17. Electrical characterisation during gradual electromigration of gold devices. Panels a to e show the evolution of charge transport characteristics of gold devices at different stages in a gradual electromigration process (performed at T=2K). The measurement of I(V) curves at successive stages show that the gold nanowires develop constrictions (panel a) that can eventually end up as tunneling nanogaps or as systems in the Coulomb blockade state (panel d). However, these "broken" nanowires can eventually be restored back into nanoconstrictions. This reconstruction of the conductive path is observed as a decrease of the device resistance and the disappearance of the blockaded region in the I(V) curves, as seen when comparing panel d to e, which belong to successive electromigration stages.

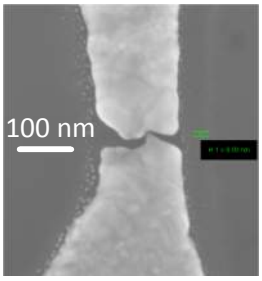

Figure 4.18. SEM image of a nanogap in an electromigrated gold nanowire. The size of the nanogap in the electromigrated gold nanowire in this image cannot be resolved by SEM.

For the sake of comparison between the results obtained for electromigration in gold and palladium nanowires, we briefly review the general trends observed in sections 4.3.1.1. and 4.3.1.2. in the next table.

Table 4.3. Comparison of palladium and gold devices. Summary of the observations on the electromigration experiments in palladium and gold devices. Note that the abbreviations *Cont. EM* and *Grad. EM* in the second column stand for continuous and gradual electromigration, respectively.

Material	Condition	Device R (low bias)	Observations
Pd	Cont. EM R_0 < 0.7 kΩ	100 MΩ to 10 GΩ	-Onset of electromigration at 0.5 V < V_C < 0.8 V. -Devices with quantum tunnelling transport characteristics (nanogaps).
	Cont. EM R_0 > 1 kΩ	100 kΩ to 100 MΩ	-Onset of electromigration at V_C > 1.5 kΩ. -Electromigration in two stages: 1) Abrupt drop of current. 2) Current decreasing in small random jumps. -Results depend on R_{LIMIT}: • R_{LIMIT} <13 kΩ ➔ devices with slightly non-linear I(V) curves (constrictions). • R_{LIMIT} >20kΩ ➔ devices with Coulomb blockade characteristics (metallic nanoclusters embedded into nanogaps).
	Grad. EM	100 kΩ to 100 MΩ	-Onset of electromigration at V_C ≈ 0.7 V when R_0 < 0.7 kΩ. -Onset of electromigration at V_C >1.5 V when R_0 > 1 kΩ. -Gradual decrease of V_C in several voltage ramps. -Electromigration in three stages: 1) Gradual decrease of V_C in several voltage ramps. 2) Abrupt drop of current. 3) Current decreasing in random jumps. -Results depend on R_{LIMIT}: • R_{LIMIT} < 13kΩ ➔ devices with slightly non-linear I(V) curves (constrictions). • R_{LIMIT} >20 kΩ ➔ devices with Coulomb blockade characteristics (metallic nanoclusters embedded into nanogaps).

Material	Condition	Device R (low bias)	Observations
Au	Cont. EM R_0 < 110 Ω	100 kΩ to 10 MΩ	-Onset of electromigration at V_C <1.1 V -R_{LIMIT}:13 to 15 kΩ ➔ Devices with slightly non-linear I(V) curves (constrictions) or Coulomb blockade characteristics (metallic nanoclusters embedded into nanogaps).
	Cont. EM R_0 >110 Ω	>10 MΩ	-Onset of electromigration at V_C >1.1 V - R_{LIMIT}:13 to 15 kΩ ➔ Devices with Coulomb blockade characteristics (metallic nanoclusters embedded into nanogaps).
	Grad. EM	>1MΩ	(Not representative due to the low number of experiments). - Devices with quantum tunnelling characteristics. -Devices with Coulomb blockade characteristics.

4.3.3. Palladium alloy devices

In previous sections (see 4.3.1) we found the adequate methods and conditions for favoring the formation of certain nanostructures by electromigration of palladium nanowires.

We then wanted to determine if our findings could be extended to palladium based alloys, which would open the possibilities of studying additional effects in the obtained devices. We were particularly interested in single electron transistors (SETs) because palladium showed a high yield in the formation of these devices (up to a 90%) by gradual electromigration.

Palladium forms magnetic alloys even when mixed with a very low percentage (0.1 to 0.2 atomic %) of a ferromagnetic impurity [39], offering the opportunity of inducing spin dependent effects in the created nanostructures. We prepared palladium alloys with a 50 atomic percent of nickel ($Pd_{0.5}Ni_{0.5}$) by co-sputtering of pure palladium and nickel targets (both of 99.99 % purity). We were aware that the proportion of palladium and nickel in the structures created by electromigration could vary from that in the deposited alloy, depending on the diffusivity of each element. However, gradually varying the initial composition of the alloy would result in a series of devices that could be interesting for a qualitative comparison.

A few tests of gradual electromigration in alloyed nanowires hinted that we could indeed obtain SETs with a yield, comparable to the case of pure palladium (see section 5.4 in Chapter 5). The yield was expected to decrease when further augmenting the nickel content, as deduced from a few experiments in pure nickel devices, in which we did not obtain any SETs. As regards the conditions at the onset of electromigration (J_C, V_C and I_C), they seemed similar to the ones for pure palladium (see Figure 4.9), although the low number of experiments only allowed for a qualitative comparison.

4.3.4. Electromigration tests in other metals

We performed a few experiments with several other materials that have been more extensively studied in literature [15, 25, 36], namely, nickel (Ni), copper (Cu), permalloy (Py or $Ni_{0.8}Fe_{0.2}$) and platinum (Pt). These tests not only served us for acquiring a better understanding of the electromigration process in general, but also for proposing specific applications in new experiments (see Chapter 5 and Chapter 6).

All the experiments were carried out by employing feedback-controlled gradual electromigration (explained in 4.3.1.2). The first test performed for each material consisted on increasing the applied voltage starting from V = 0, in order to determine the parameters at the onset of electromigration. Once the approximate I_C and J_C were known, the V_C of the first electromigration cycle of each device could be approximately predicted. This was done by measuring the initial resistance, since $V_C \approx I_C \times R_0$. We assumed that the nanowire dimensions and grain structure were similar (meaning that I_C and J_C would be practically constant) in devices belonging to the same fabrication batch.

The electromigration process was slightly different for each material, as expected for different diffusivity, grain structure and activation energies, among other possible factors. This could be noticed, for instance, in the different shape of the I(V) curves at the onset of electromigration. The resulting nanostructures depend on the nature of the metal and its grain structure. Therefore, the chances for obtaining certain combinations of metals and nanostructures may be very low. The charge transport characteristics observed in the obtained devices account for the types of nanostructures that are more likely to form in each metal.

The following figures (Figure 4.19 to Figure 4.24) show some examples of the experimental I (V) curves and Table 4.4 summarises our observations and results.

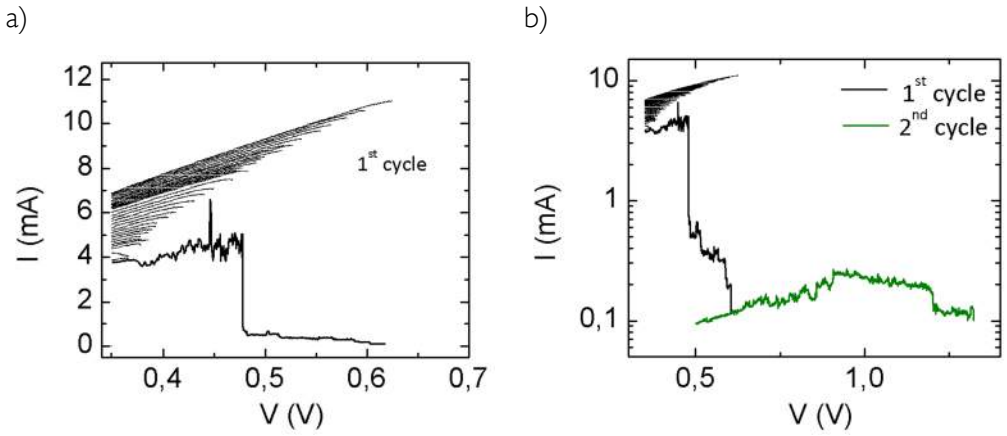

Figure 4.19. Electromigration of copper nanowires. a) First cycle of gradual electromigration, in which V_C and I_C decrease in each voltage ramp, while the measured resistance increases gradually from 50 Ω to about 80 Ω. At this point, there is a major break, after which the I(V) curves enter a regime in which they evolve in sudden and random jumps, instead of gradually. The current decreases in steps in the final stage of this 1st cycle. b) First two cycles of the electromigration process of the same device, where the changes in the measured current are more clearly observed in a logarithmic scale. Note that in the last stage (2nd cycle) the current increases around V=1V and later decreases abruptly (therefore, this nanowire is partially reconstructed and once more, rebroken during the electromigration process).

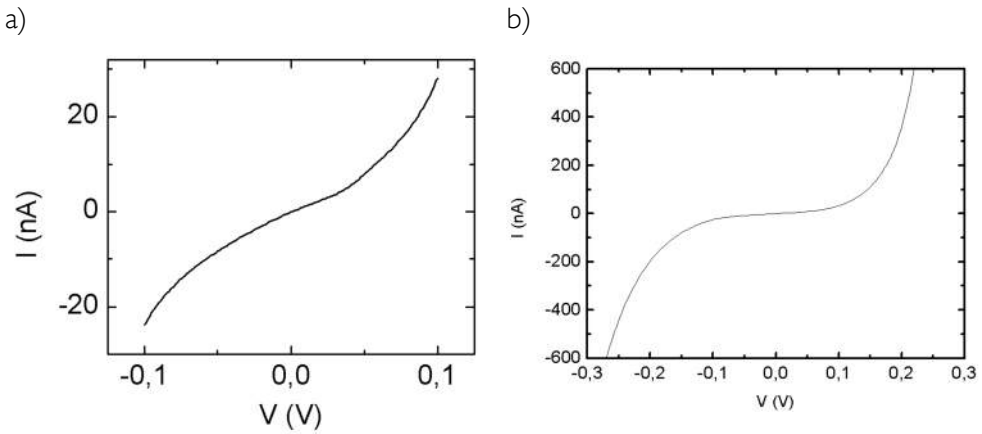

Figure 4.20. Characterisation of electromigrated copper nanowires. Non linear I(V) curves obtained at the last stage in the electromigration process shown in Figure 4.19. Both I(V) curves correspond to the same device, recorded at different bias range.

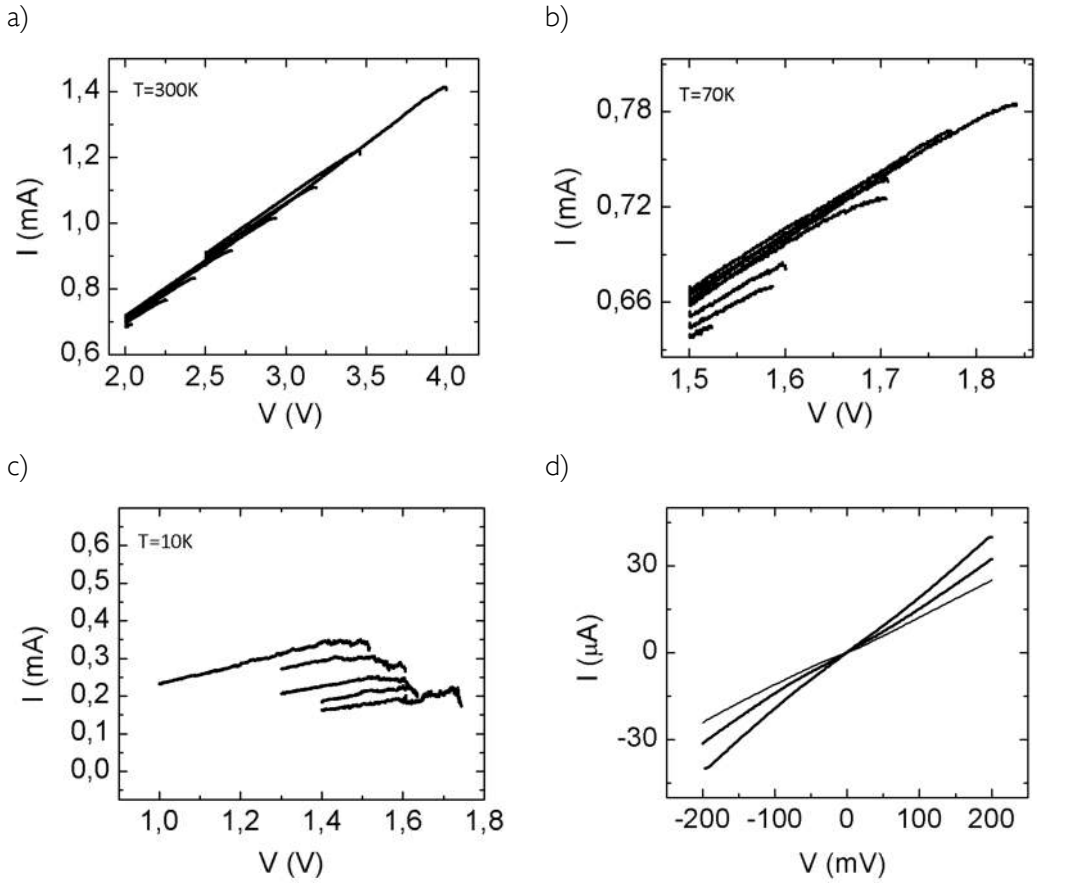

Figure 4.21. Electromigration of platinum nanowires. a) I(V) curves corresponding to a pre-breaking process of a platinum nanowire by electromigration at T=300K. Breaking the nanowire at this temperature was easier, due to an enhanced thermal activation. We lowered the critical voltage at the onset of electromigration in each ramp, approximately from V_C=4 to V_C=2V. b) Follow up of the electromigration process shown in a). The nanowire was further broken at T=70K. c) Performing the final breaking stage at lower temperatures (T=10K) was more controllable, due to a lower thermal activation. Thus, the cross-section of the nanowire was gradually narrowed until acquiring the desired transport characteristics in the device. d) Evolution of the I(V) curves measured during different breaking stages of the nanowire. We stopped the breaking process for measuring each of the I(V) curves. These three curves, which have a slightly non-linear shape, show the gradual decrease of the measured current while the constriction in the nanowire is narrowed.

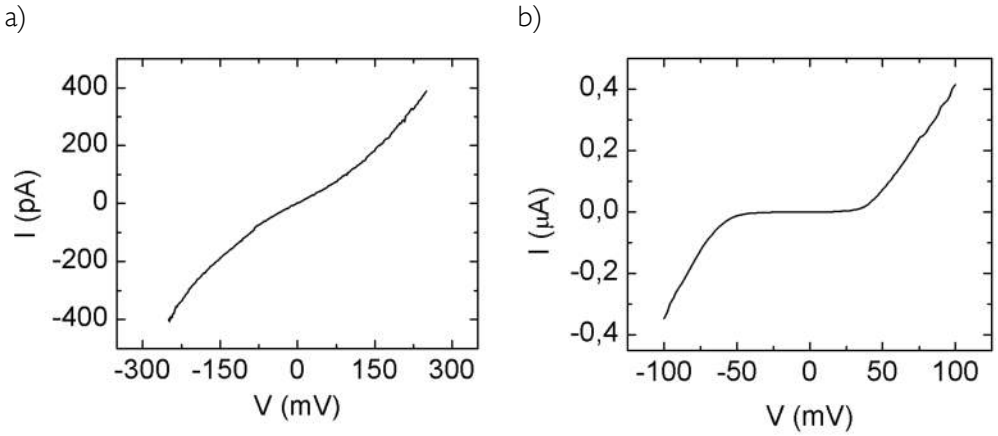

Figure 4.22. Charge transport characteristics of electromigrated platinum nanowires. a) Platinum nanowire electromigrated until obtaining a tunnelling transport regime. b) Coulomb blockade characteristics were also obtained in electromigrated platinum nanowires, although they were not stable enough for performing a full characterisation by applying a gate voltage. Their tendency was to undergo partial reconstructions of the conductive path, recovering a linear or a slightly non-linear shape in the I(V) curves.

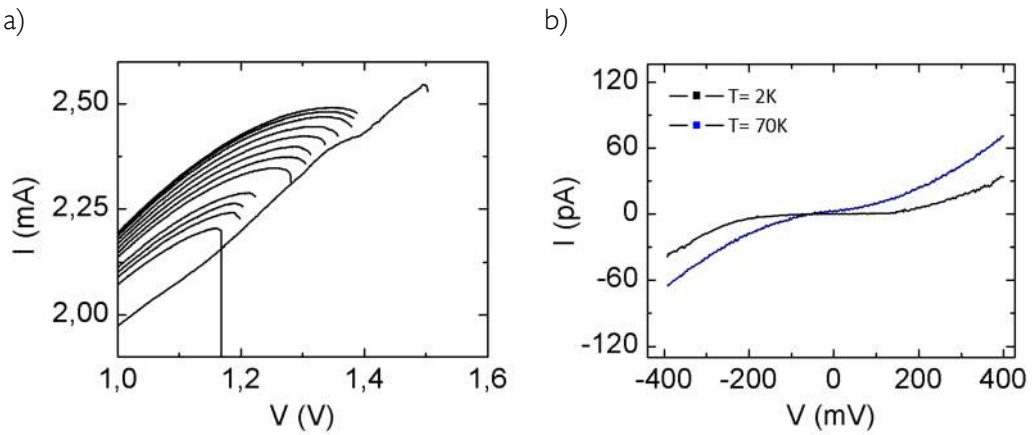

Figure 4.23. Electromigration and charge transport characteristics of permalloy nanowires

a) I(V) curves measured during the electromigration of permalloy nanowire at T= 2K. b) Coulomb blockade characteristics were observed in several devices at low temperatures (T= 2K), indicating the formation of quantum dots embedded between closely separated electrodes. When increasing the temperature (for instance, see the curve at T= 70K in the graph), the Coulomb blockade state disappeared due to thermal activation of the charge carriers.

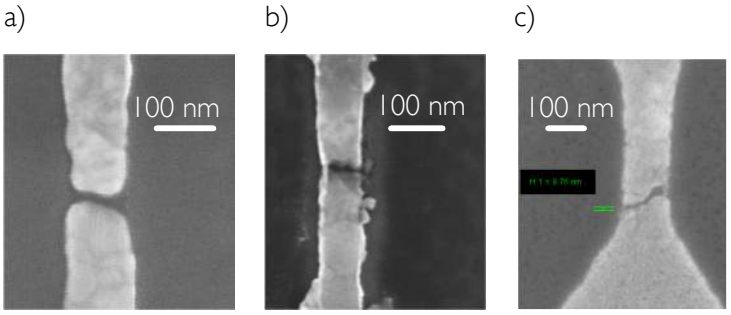

Figure 4.24. SEM images of electromigrated nanowires. a) Nanogap of around 13 nm and b) nanogap bridged (on the left side) by a constriction of width < 10 nm obtained by electromigration of permalloy nanowires. c) Nanogap of around10 nm in an electromigrated copper nanowire.

The estimated current densities agree fairly well with those reported in literature [13, 15, 25, 32], although our results are not supported by the necessary statistics and are therefore illustrative. In fact, the performed tests had the purpose of serving as a qualitative study for planning our future experiments. We briefly comment on the results of the experiments with different materials in Table 4.4.

Table 4.4. Summary of electromigration tests with different materials. Approximate value for the critical current density (J_C) and comments on the electromigration experiments for each of the studied materials.

Material	J_C (A/m^2)	Observations
Cu	2.6×10^{12} (T<10K)	-Highly controllable and gradual breaking process. -Rearrangements can lead to a reconstruction of the nanoconstrictions, decreasing the device resistance. -Stable nanoconstrictions with a wide range of resistances. -Devices with quantum tunnelling transport characteristics.
Pt	8.54×10^{11} (T=300K)	-Pre-breaking done at T=300K and electromigration continued at T=10K. -Highly controllable and gradual breaking process. -Rearrangements can lead to a "reconstruction" of the nanoconstrictions, decreasing the device resistance. -Stable nanoconstrictions with a wide range of resistances. -Devices with quantum tunnelling transport characteristics. -Devices with Coulomb blockade characteristics; not stable, tend to reform a constriction or break further into a gap.
Py	1.2×10^{12} (T<10K)	-Performing a gradual breaking process becomes difficult as the nanowire cross-section decreases; once the nanowires develop constrictions, they often break suddenly to give negligible conductance values in the devices. Obtaining stable

		constrictions seems difficult. -Devices with quantum tunnelling and Coulomb blockade transport characteristics (both types of structures are fairly stable, compared to platinum and copper devices).
Ni	1.4×10^{12} (T<10K)	-Devices with quantum tunnelling characteristics in the charge transport.

4.4. Conclusions

We explored the possibilities of electromigration for the fabrication of devices with nanostructures that would be difficult to obtain by conventional EBL. We obtained devices with different active elements, such as nanogaps, nanoconstrictions and metallic nanoclusters, which could be used in multiple nanoelectronics applications. Distinctive charge-transport properties allowed identifying the type of nanostructures contained in the devices.

Two different strategies were employed in the experiments: gradual and continuous electromigration. In addition, we used different working conditions for tailoring the charge-transport characteristics of the obtained devices. Regarding the materials utilised, our study focused mainly on palladium, although we also performed tests in other metals and alloys, namely, gold, copper, platinum, nickel, permalloy and palladium-nickel.

The following points summarise our main conclusions:

- As expected, the outcome of electromigration depended on the experimental conditions, the nature of the material and the grain structure of the nanowires. The difficulty to control the latter is mainly the reason for which the results obtained by this technique are practically statistic. However, we found that the strategy chosen for electromigration in combination with the material properties of the nanowires can lead to the formation of certain nanostructures in an almost deterministic manner. For instance, we obtained palladium devices with Coulomb blockade characteristics with a yield of around 90% by gradual electromigration. We then extended the procedure to ferromagnetic palladium alloys (further studied in Chapter 5).
- It is worth noting the clear correlation and homogeneity in the results obtained in devices of the same fabrication batch. This confirmed that slight variations in the metal deposition parameters could induce significant changes in the grain structure of the nanowires, directly affecting the results of the experiments. This made us aware of the importance of statistics and of our limitations for drawing quantitative conclusions from these experiments.

- We studied electromigration in palladium nanowires using different working conditions for tailoring the charge-transport characteristics of the obtained devices. We varied the critical current and voltage at the onset of electromigration by changing the cross-section of the nanowires and the total resistance of the devices, respectively. Interestingly, we found the existence of a threshold resistance value separating two different sets of results. Apart from that, we found that employing different electromigration strategies (gradual or continuous) could yield different types of devices. Taking advantage of these particular features of palladium, we could favour the transformation of the nanowires in our devices into nanoconstrictions, electrodes with tunnelling nanogaps or nanostructures with Coulomb blockade characteristics.
- Our results in the electromigration of gold nanowires agreed fairly well with literature, meaning that our experimental methods were comparable to the ones used by other groups. In general, we noticed that the nanostructures obtained by the gradual electromigration method were not very stable and tend to alter their transport properties during electrical characterisation, probably due to grain rearrangements.
- Performing a few tests in different metals such as nickel, copper, permalloy ($Ni_{0.8}Fe_{0.2}$) and platinum served us to acquire a better understanding about the electromigration process in general. In spite of being just qualitative results, the general trends observed in these tests were helpful for the proposal of new experiments. (The work presented in Chapter 6 is an example).
- Based on the occurrence of different nanostructures resulting from the electromigration experiments presented along this chapter, we proposed several possible applications for further studies (Table 4.5). Note that the formation of these nanostructures is closely related to the nature of the metal and its grain structure. Therefore, the chances of obtaining certain combinations of metals and nanostructures might be very low.

Table 4.5. Summary of studied materials and potential applications. Relation of the studied nanowire materials, the nanostructures predominantly obtained in the experiments and potential applications that could inspire further research projects.

Material	Potential applications	Obtained structures
Pd	Single electron transistors	Metallic nanoclusters embedded into nanogaps
PdNi		
Py		
Au	Tunnel junctions and electrodes for molecular electronics	Nanogaps
Pt		
Au	Spintronics	Nanoconstrictions and nanogaps
Cu		
Py	Magnetic tunnel junctions and electrodes for molecular electronics	Nanogaps
Ni		

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Chapter 5

We employ the previously explored nanofabrication methods for obtaining single electron transistors (SETs). We describe the fabrication of SETs based on metallic quantum dots by the combination of electron beam lithography and electromigration techniques. Our main goal is the fabrication and measurement of these devices in situ and the prospect of using the same strategy for exploring the properties of different materials.

We first introduce some basic concepts about single electron transport and Coulomb blockade theory in section 5.1, followed by the experimental sections 5.2 and 5.3, in which the fabrication and characterisation of palladium SETs is explained in detail. Section 5.4 extends the methods stablished in 5.2 and 5.3 to obtain SETs of palladium-based ferromagnetic alloys. Finally, the conclusions of the chapter are summarized in section 5.5.

5. Obtaining single electron transistors by electromigration

Single-Electron Transistors (SETs) are electronic devices that provide the means for controlling the circulation of individual electrons [1]. Roughly speaking, these devices consist of two parts; a zero-dimensional element or quantum dot and a set of electrodes that connect the dot to an electrical circuit.

Single electron transport has been studied in a great variety of nanostructures. SETs in which either metallic or semiconducting nanoparticles [2-5], single molecules [6-8], carbon nanotubes [9-11] or graphene nanoribbons [12] act as quantum dots have been reported in literature. The case of SETs constituted by small metallic grains is especially interesting. On one hand, it allows probing the influence of quantum confinement in electron-electron correlations and spin-orbit interactions in a given metal. On the other hand, the possibility of alloying different metals offers the opportunity of tuning the type of electronic interactions, for example, by the introduction of ferromagnetism or superconductivity [2, 13].

In this chapter we focus on the fabrication and characterisation of SETs that have metallic quantum dots as active elements. The fabrication of such devices requires electrically contacting individual elements of small dimensions, such as nanoparticles. As we discussed in chapter 4, we employ electromigration for this task, as it is a widely used strategy for obtaining electrodes in the nanometre size range.

We chose palladium (Pd) for constituting our devices for several reasons. First, the predictions of spontaneous magnetisation in Pd nanostructures make it an attractive choice

for single electron physics studies [1, 9, 14, 15]. Second, due to its material properties, Pd tends to form small metallic clusters during electromigration, which is ideal for the creation of quantum dots. Last but not least, being a noble metal, it is suitable for fabricating electrodes.

5.1. Single electron transport and Coulomb blockade

The theory of single electron transistors has been described in detail in several reviews [2]. In this section we give a simple description of the theory and we address the existing publications for further details.

The fundamental condition for observing single electron transport in an electronic device is having a low dimensional element capable of inducing the confinement of conduction electrons. This element can be simply pictured as a small island of a conductive material called quantum dot (QD). A QD contains a finite number of electrons (N) that confer a net electrical charge $Q = Ne$. If this small conducting body is placed into a dielectric environment, it will have the capacitance (C) and an electrostatic energy $E = Q^2/2C$ (or in this case, $E = (Ne)^2/2C$) associated to it.

Let us assume that the dot is contacted by a pair of electrodes and connected to an electrical circuit. If we add just one electron to the dot, its electrostatic energy increases roughly by the amount $E_C = e^2/2C$. This quantity is known as the single electron charging energy (E_C). In other words, E_C is the energy we must provide in order to overcome the Coulomb repulsion created by the electrons contained in the dot. As the dot decreases in size, the repulsion is stronger and the E_C is larger. We can also draw this conclusion by observing that the capacitance depends on the dimensions and shape of the conductor, as well as on the dielectric environment. Assuming that the QD has a spherical geometry and it is embedded in an environment with permittivity $\boldsymbol{\varepsilon}$, its capacitance is given by $C = 2\pi\varepsilon d$. Decreasing the diameter (d) also decreases the capacitance and therefore, E_C becomes larger.

At this point, we must mention that in the present model we are ignoring the quantum mechanical energy level-spacing (arising from spatial confinement). In the case of metallic grains of more than a few nanometres, the distance between quantum mechanical electronic energy levels (ΔE) is negligible compared to E_C. Thus, the origin of single electron transport in our devices is purely electrostatic and we have a so-called classical dot.

Figure 5.1 shows two sketches representing the structure and the energy landscape of the system composed of a QD contacted by a pair of electrodes, which we will call source (S) and drain (D). There is an energetic barrier (a tunnel barrier) that gives a contact resistance (R_S and R_D) between the QD and each of the electrodes. A bias voltage (V_{SD})

applied by an external source controls the difference between the electrochemical potentials of the electrodes, $\mu_S - \mu_D = eV_{SD}$. The different charge states of the QD are represented by discrete energy levels with a distance of $E_C = e^2/2C$ from each other. Again, we would like to highlight that these energy levels arise from electrostatic effects (Coulomb repulsion) and not from quantum mechanical effects. All the levels below μ_S and μ_D are occupied by a single electron, while the ones located above remain empty.

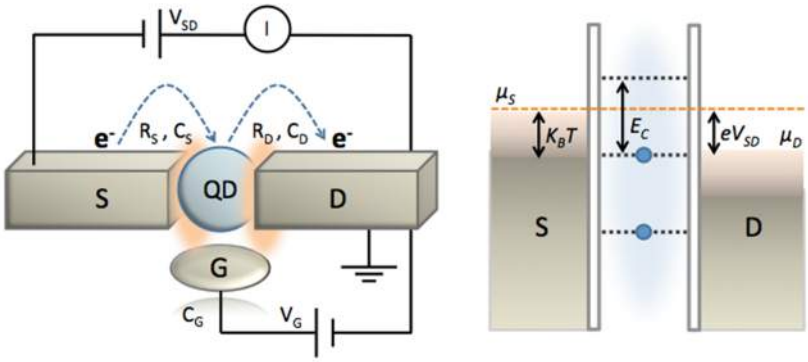

Figure 5.1. Sketch of the structure and the energy landscape of a single molecule transistor. Left: schematic diagram of a SET with a quantum dot (QD) between source and drain electrodes (S and D, respectively). There is a tunnel barrier between the QD and each of the electrodes, resulting in the resistances R_S and R_D, as well as in a capacitance C_S and C_D. A back gate electrode (G) supplies gate voltage V_G and has the corresponding capacitance C_G. Right: diagram showing the energetic landscape of the described SET. An applied source to drain voltage (V_{SD}) creates a difference (eV_{SD}) between the electrochemical potentials of the electrodes (μ_S and μ_D). The horizontal lines in the space between S and D represent the different charge states of the QD. The distance to the first available state corresponds to the energy amount E_C (charging energy). The contribution of thermal energy to the system has been represented as a smearing of magnitude (K_BT) in the energy distribution of the electrodes.

Single electron charging effects start to affect the charge transport through the dot when the thermal energy range of the system is below that of E_C. Thus, the comparison between E_C and the thermal energy (given by $E = K_BT$, where K_B is the Boltzmann constant and T is temperature), leads to the first condition for the observation of single electron transport: $E_C >> K_BT$. According to literature, the proportion should be roughly $E_C \sim 100 \times K_BT$, which corresponds to $E_C \sim 100 \times 26$ meV at room temperature and $E_C \sim 100 \times 0.16$ meV at T=1.8 K (the lowest temperature achieved with our current equipment). As a direct consequence of this condition, we note that studying QDs of bigger dimensions implies working at lower temperatures. The advances in microfabrication techniques have allowed reducing the dimensions of the QDs to around 2 nm and obtaining SETs that can operate at room temperature [4].Table 5.1 shows some examples of E_C values extracted from experiments with different types of QDs reported in literature.

Table 5.1. Examples of charging energy (E_C) and energy level-spacing (ΔE) values for different QDs. Taken from [17].

QD type	QD size	E_C	ΔE
Gold cluster	10 nm	Tens of meV	~0.2 meV
Carbon nanotube	500 nm	~10 meV	~3 meV
C_{60} molecule	1 nm	~3.3 eV	~100 meV

Observing the circulation of individual electrons also demands having a well-defined number of electrons in the dot. Therefore, the QD must be weakly coupled to the electrical contacts. This condition is fulfilled by placing a tunnel barrier between the QD and each of the contacts (source and drain electrodes). The contact resistance (R_C) must be high enough to suppress quantum fluctuations of the charge through the tunnel barriers at either side of the QD. This implies that the leak-out time for an electron through any of the contacts, or more exactly, the quantum mechanical energy uncertainty associated with it, should be small compared to E_C. We thus infer the lower limit for the contact resistance $R_C > e^2/2h$, which corresponds to the resistance of a single conductance channel (R_Q).

In devices that meet these two conditions ($E_C >> K_BT$ and $R_C >> R_Q$) the circulation of electrons is suppressed at low bias voltages. This situation in which the device is in the OFF state is known as Coulomb blockade. The corresponding energy diagram (Figure 5.1) shows that there are no energy levels available in the bias window between the source and drain electrochemical potentials, μ_S and μ_D ($\mu_S - \mu_D = eV_{DS}$). Therefore, no current can flow into or out of the dot.

There are two ways for lifting the blockade and allowing a sequential tunneling of electrons through the dot. An electron tunnels into the dot when the bias voltage (V_{SD}) is increased enough to access a new charge state. If the applied voltage (V_{SD}) is not further increased to access the next state, an electron must leave the dot before another one is able to enter. Thus, the QD acts as a bottleneck in the circuit, limiting the flow of charge carriers to one at a time (Figure 5.2-b). The Coulomb blockade can also be lifted by bringing an energy level into resonance with the Fermi level of the source and drain electrodes. Then, electrons are allowed to pass even at zero bias voltage ($V_{SD} = 0$) by resonant tunneling. This situation is achieved by applying a voltage at a third terminal (gate electrode), which is used for tuning the electrochemical potential in the QD by electrostatic field-effect. The gate electrode is capacitively coupled to the QD through an electrically opaque insulating barrier (gate dielectric or gate oxide), in order to avoid any leak of charge carriers (Figure 5.2-c).

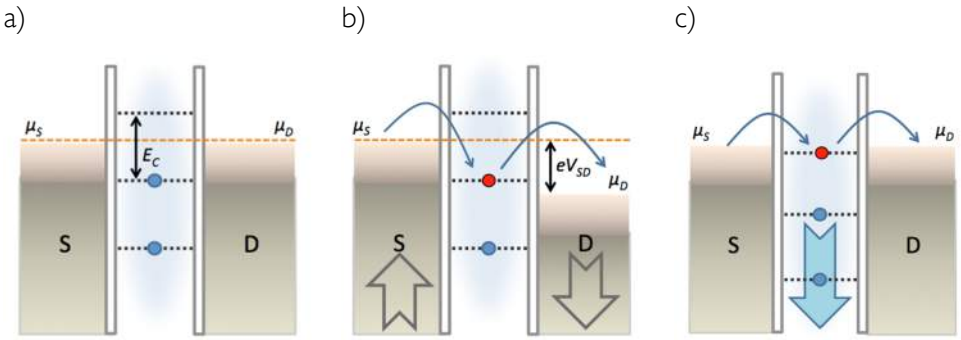

Figure 5.2. Schematic view of the charge transport mechanisms in the single electron transport regime. Sketches illustrating the relative position of the electrochemical potential of source (S) and drain (D) electrodes (μ_S and μ_D, respectively) with respect to the energy levels of the QD. a) Represents a device in the Coulomb blockade (CB) state. b) Applying a potential between S and D electrodes (V_{SD}) lifts the CB, allowing the circulation of electrons. c) The CB is lifted at $V_{SD} = 0$ by applying a gate potential V_G and shifting the electrostatic energy of the QD until an available charge state level is brought into resonance.

The charge transport in the Coulomb blockade regime is characterised by current (I) *versus* voltage (V_{SD}) curves with a plateau of negligible conductance around zero bias. As V_{SD} is increased, an abrupt onset indicates that E_C is overcome and the Coulomb blockade is lifted. In addition to this, the size of the plateau can be tuned by applying different values of gate potential (V_G). When an energy level is brought into resonance by applying the adequate V_G value, the plateau disappears and there is a circulation of current even at V_{SD}=0. Note that even if in the example in Figure 5.3 the I(V) curve is symmetric with respect to the bias voltage, it does not necessarily have to be like that. It is possible having different energy barriers for tunneling to the QD from the source or the drain electrodes (due to differences capacitive coupling of the QD with the respective electrodes). Therefore, the asymmetries in the I(V) curve reflect these different coupling regimes with source or drain electrodes.

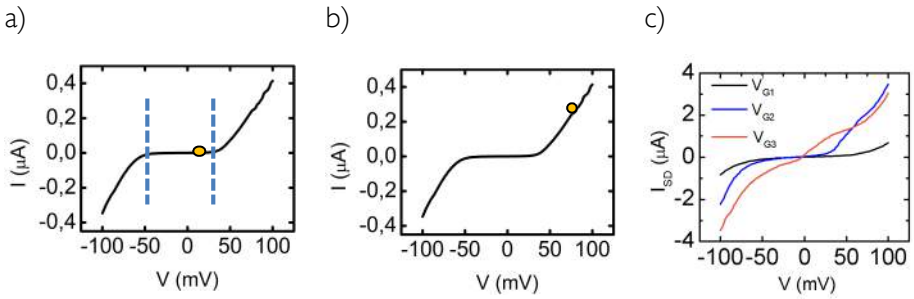

Figure 5.3. Characteristics of charge transport through a QD. The graphs in a, b and c corresponds to the situations described in panels a, b and c of Figure 5.2, respectively. a) When the system is in the Coulomb blockade state, the I(V) curve is characterised by a plateau in which the measured current is negligible (delimited

by blue dashed lines in the graph, corresponding to the onset of charge transport in the device, roughly at V=± 50 mV). b) When the applied bias exceeds the charging energy, there is a net charge current flowing through the QD (for instance, we would have this situation in the spot represented by a coloured dot in the graph, corresponding roughly to V_{SD}=75 mV). c) Applying different gate potentials leads to variations in the shape of the I(V) curves in general, as observed in 3 curves represented in this graph. There are situations in which the charge transport takes place even without an applied bias voltage, as observed in the red curve (corresponding to Figure 5.2-c).

5.2. Device fabrication

Our targeted devices have a planar geometry and a three-terminal configuration, with metallic source and drain nanoelectrodes and the doped silicon substrate as back-gate electrode. A quantum dot should bridge the space between source and drain electrodes, resulting in a single electron transport regime.

Nowadays there is no lack of methods for obtaining electrodes and metallic quantum dots of extremely small sizes. However, the assembly of these two elements into a nanometric transistor is still challenging. In addition, some metallic nanoparticles tend to be chemically reactive and prone to oxidation due to their high surface to volume ratio. This condition often requires working at inert atmospheres and using passivation layers, which may add difficulty to the task.

Typically, the fabrication of such SETs comprehends the following sequence: 1) a lithographic step for patterning macroscopic electrical contacts, 2) creating nanoelectrodes by lithography or alternative techniques and 3) the addition of nanoparticles by chemical or physical methods [18-20].

Following the procedure explained in the next sections, we have achieved the simultaneous formation of quantum dots and nanoelectrodes assembled into a SET configuration, skipping a step of the fabrication sequence. Thus, we have simplified the fabrication process of SETs and in addition, we have performed the characterisation of these devices in situ.

5.2.1. Electron beam lithography

We used electron-beam lithography for defining palladium devices on top of p-doped silicon chips coated with 150 nm of thermally grown silicon oxide (SiO_2). The lithography was carried out on a double layer polymethyl metacrylate (PMMA) resist system spun onto the thermal SiO_2 surface, followed by metal deposition and lift-off (see details in Chapter 4, section 4.2). We fabricated devices depositing 25nm of Pd (99.99%) by magnetron sputtering.

Each device consisted of a palladium nanowire attached to a pair of microscopic electrodes and terminated with a pair of macroscopic contact pads, where it was connected to the electrical measurement system (more details in Chapter 2, section 2.3.1). Each of the as-produced palladium nanowires was around 300 nm long, 25 nm thick and around 65 nm wide, which gave an approximate cross-section of 1600 nm^2. The devices were cleaned with acetone and isopropanol, followed by 10 seconds of oxygen plasma, before placing them in a liquid helium cryostat. The initial resistance of the devices (R_0) had ranged between 600 Ω and 900 Ω (measured in a 2 probe configuration at a temperature of 1.8 K). As expected, they showed linear current *versus* voltage characteristics, before the electromigration process.

5.2.2. Electromigration: obtaining SETs in one step

As explained in chapter 4, we can obtain electrodes separated by distances well below 10 nm by electromigration. This technique consists on applying a high electrical current density through a metallic wire of nanometric cross-section, until it breaks by electrical stress.

The combination of certain experimental conditions during the electromigration process and the intrinsic properties of the nanowire material can favor the simultaneous formation of metallic quantum dots (probably in the shape of small clusters or nanoparticles) at the breaking point. The newly formed QDs have the advantage of being already embedded in the gap between the two electrodes that can be used as source and drain terminals. No additional step is needed for adding the QDs onto the electrodes, simplifying the fabrication. A gate electrode can be readily added by electrically addressing the doped silicon substrate lying under the insulating gate oxide. The resulting device is a SET with its three terminals (source, drain and gate) capacitively coupled to a metallic QD. The device is thus created inside a cryostat chamber, which constitutes a fairly clean environment with a good control of the pressure and temperature. Most importantly, the as-fabricated device is ready for electrical characterisation without further manipulation.

The formation of SETs with metallic QDs as a consequence of electromigration has already been reported [7]. These devices have generally been regarded as undesired by-products when the aim was obtaining bare electrodes with clean inter-electrode gaps. Opposite to this, we have used the spontaneous formation of SETs to our advantage.

All the electromigration and electrical characterisation experiments were carried out at 1.8K inside a liquid He cryostat with 10 mTorr He atmosphere. A home-made LabVIEW program controlled the electromigration process with the aid of an appropriate feedback algorithm (see section 4.1.2 in chapter 4 for more details). The nanowires were gradually broken by electromigration. The strategy consisted on applying series of increasing voltage

ramps and limiting the extent to which the electromigration took place in each ramp. This was done by continuously monitoring the conductance (G) across the device and limiting the amount it changed in the last measured 40 data points. Figure 5.4 shows the conductance of a device as it evolved in a typical electromigration process. At the beginning of each voltage ramp the conductance of the device decreased slightly, due to the increase of electron scattering events as the circulating current got higher. The observation of a sudden decrease of conductance marked the starting point of electromigration. We refer to the values of voltage and current at the onset of electromigration as the critical voltage (V_C) and critical current (I_C), respectively. Typically, we limited the decrease of conductance to a 1.5% in the last measured 40 data points, after which the applied voltage was reset to zero and a relaxation time of 5 seconds was allowed. These conditions ensured that the electromigration in the nanowire occurred only partially in each voltage ramp. As the gradual breaking process of the nanowires was carried out, V_C decreased. When the onset of electromigration took place at V_C values lower than about 500 mV, we allowed the nanowire to electromigrate beyond the previously set limits. During the final voltage ramps the nanowires suffered a sudden and major break. Afterwards, the evolution of the conductance entered a different regime in which sudden jumps of random character were often observed. The applied voltage was steadily increased until a target conductance value was reached (typically, around 25 μS), after which the voltage was reset to zero and the process was finished. At this point, the low bias resistance of the devices was in the order of 1 to 100 MΩ (measured at V = 20 mV and T =1.8 K) and the measured I(V) curves became non-linear.

During the electromigration process the nanowires develop constrictions that grow gradually throughout several voltage ramps until they finally break [21]. This is consistent with the steady decrease of G measured during the first few voltage ramps of the process (Figure 5.4-a). As regards the more random evolution and the sudden jumps of G observed in the last stage of the process, they are generally attributed to rearrangements of the metal grains. We could occasionally observe the conductance decreasing in quantized steps in this last stage. This quantization indicated the formation of a constriction with a few conductance channels just before the complete breakdown of the nanowire.

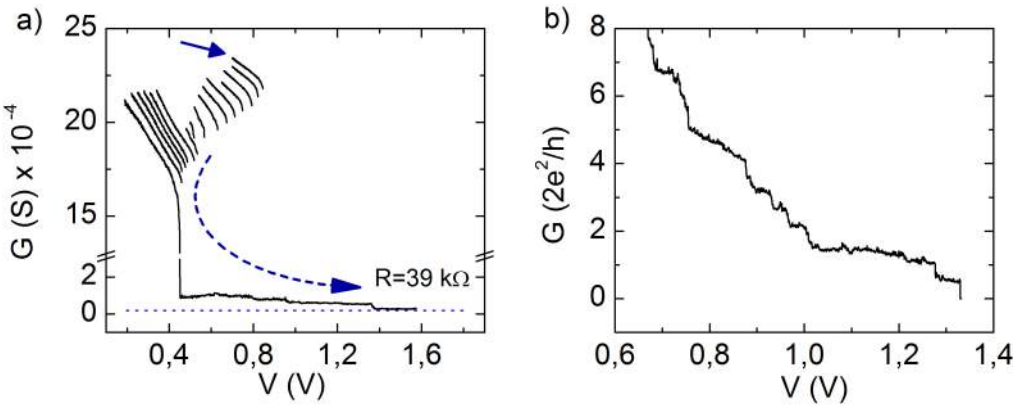

Figure 5.4. Evolution of the device conductance (G) during the electromigration process of a palladium nanowire. a) A series of increasing voltage (V) ramps are applied while the decrease of G in each V ramp is limited to a 1.5%. The solid arrow indicates the starting point of the first V ramp, while the dashed arrow shows the order of the successive V ramps throughout the process. A gradual decrease of G indicates that the cross-section of the nanowire is decreased after each V ramp. The V required for triggering the electromigration decreases accordingly with the cross-section. When the required V is below 0.5 V we let G to decrease beyond the 1.5% limitation. The nanowire suffers a major break (observed as a sharp jump in G) and it becomes unstable. Afterwards, G evolves in random jumps until a target G value of 25 μS (indicated by a dotted line) is reached. b) Evolution of the conductance (G) in units of quantized conductance ($G_Q=2e^2/h$) in the last stage of the electromigration for a similar nanowire. The appearance of quantized conductance steps indicates the formation of a narrow constriction before the physical failure of the nanowire.

5.3. Electrical characterisation

As explained in the previous section, we obtained SETs by electromigration inside a He cryostat chamber at T=1.8K. The electrical characterisation was done in situ, since the as-produced devices were already connected to an electrical measurement system.

The characterisation consisted on DC measurements realized with a Keithley sub-femtoamp remote source-meter SMU instrument (model 6430) or a Keithley dual-channel source-meter instrument (model 2636A). We mostly worked in a 2 probe configuration and set the electrical measurement system in voltage-source and current-meter mode. We realized the measurements following the next sequence:

1) Record the source-drain current (I_{SD}) while sweeping the bias voltage (V_{SD}) at a constant gate voltage (V_G).
2) Step the gate voltage.
3) Iterate steps 1 and 2 for the whole range of gate voltages we wanted to explore.

4) Obtain the differential conductance (dI/dV) by calculating the derivative of the measured current with respect to the bias voltage.

In general, we did not vary much the temperature during the electrical characterisation, since it caused the loss or irreversible distortion of the Coulomb blockade features. This suggests that the obtained nanostructures undergo physical rearrangements when changing the temperature. However, we did explore the variation of other type of conductance features with temperatures ranging from 1.8 K to 15 K (explained in section 5.3.4).

5.3.1. Measurement of gated source-drain current

In about 90 % from a total amount of 35 experiments, the source-drain I(V) curves of the electromigrated devices were non-linear. Around 71% presented a plateau of almost negligible current near the zero bias region of the I (V) curves (Figure 5.5, curves a and b). The observed charge transport features were a characteristic of the Coulomb blockade regime. This was an indication of the possible transformation of the metallic nanowire into a QD coupled to a pair of electrodes. On the other hand, most of the obtained devices showed a periodic modulation of the described transport features as a function of the applied gate potential. This last observation confirmed that after the electromigration of the nanowires, the devices had indeed transformed into SETs in which the current went through a QD. As explained in section 5.1, the modulation with V_G occurs because the electrostatic energy of the QD is shifted with respect to the electrochemical potential of the source and drain electrodes by field effect. Depending on the applied V_G electrons need a different amount of energy for tunneling into the quantum dot. Hence, the onset of the circulating current (I_{SD}) shifts accordingly to higher or lower V_{SD} values (Figure 5.5, curve b). For certain V_G values, an energy level of the QD may align with the μ_S and μ_D in the source and drain electrodes, allowing the circulation of electrons by resonant tunneling even near V_{SD}=0 (Figure 5.5, curve c).

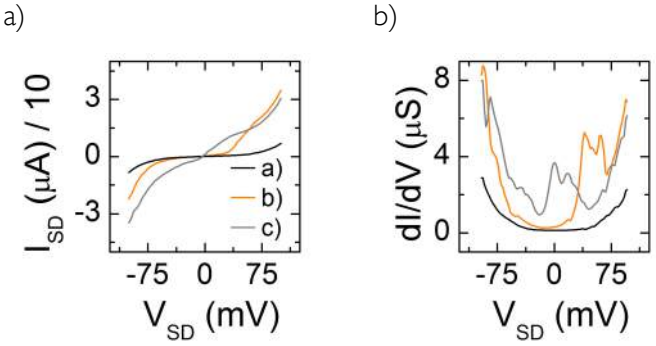

Figure 5.5. Transport features of the obtained SETs. Top left graph: Drain Current (I_{SD}) *versus* bias voltage (V_{SD}) curves for a palladium SET obtained by electromigration, measured at 3 different values of gate voltage (V_G). Top right graph: Differential conductance (dI/dV) *versus* V_{SD} curves, obtained by calculating the derivative of the I_{SD} *versus* V_{SD} curves. As V_G was varied, the devices changed from the Coulomb blockade (CB) state, with its characteristic plateau of almost negligible current near the zero bias region (curves a and b), to more conductive states (curve c).

5.3.2. Stability diagrams

The effect of V_G is more easily analysed in the differential conductance curves (dI/dV), which are obtained by calculating the derivative of the recorded I_{SD} vs V_{SD} traces. The circulation of single electrons into or out of the QD is marked by peaks in the dI/dV. These peaks appear at different V_{SD} values depending on the applied V_G. We calculated the dI/dV curves for a range of gate voltages and we plotted them as a function of V_{SD} and V_G. The resultant graphs, commonly known as stability diagrams, constituted a conductance-map of the devices. Some of our devices showed stability diagrams with the characteristic pattern of a SET, in which we observed periodic diamond-shaped regions of almost negligible conductance (Figure 5.6).

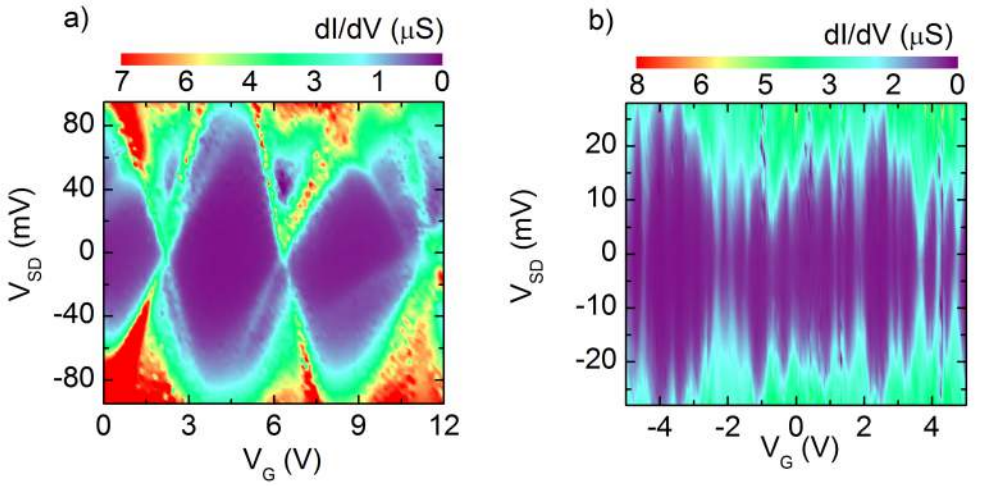

Figure 5.6. Stability diagrams of palladium SETs obtained by electromigration. Plotting the derivative of the drain current (dI/dV) as a function of bias voltage (V_{SD}) and gate voltage (V_G) results in a pattern of diamond-shaped regions of almost negligible conductance. These conductance features are characteristic of the Coulomb blockade regime and they indicate the transformation of the palladium nanowires into QDs. Differences in the dimensions of the diamonds in a) and b) indicate that the QDs formed in each case have a different size and a different coupling with the electrodes.

Each of the so-called Coulomb diamonds represents the range of V_{SD} and V_G at which the circulation of electrons through the QD is blocked. At V_G values between contiguous diamonds the electrostatic energy of the QD is shifted enough to admit a new electron at V_{SD}=0. Therefore, the average number of electrons inside the QD is fixed in each blockaded region and contiguous regions differ by just one electron. The dimensions and shape of the diamonds can be used to extract information about the studied systems (such as the charging energy, size of the quantum dot, energy level-spacing, coupling with the electrodes, etc) [2, 3, 5, 7] (Figure 5.7). The longest dimension of the Coulomb diamonds in the V_{SD} axis is related to the charging energy ($\Delta V_{SD} = 2E_C/e$). The charging energy can be written as $E_C = e^2/2C$, where C is the total capacitance of the quantum dot. The capacitance is related to the size of the QD and therefore, we can extract information about its approximate dimensions using a simple model, such as that of a conducting sphere into a dielectric environment. In this case we can use the expression for the self-capacitance of a sphere $C = 2\pi\varepsilon d$, where ε is the absolute permittivity of the dielectric media and d is the diameter of the conducting QD. According to these expressions, we extracted the following values from diagrams in Figure 5.6-a and Figure 5.6-b respectively: E_C (a) = 6.47 × 10^{-21} J and E_C (b) = 1.85 × 10^{-21} J for the charging energy; C (a) = 1.98 × 10^{-18} F and C (b) =6.95 × 10^{-18} F for the total capacitance; d (a) = 12.5 nm and d (b) = 32 nm for the approximate diameter of the QD (assuming a spherical shape and ε = 3.45 × 10^{-11} F/m for the silicon dioxide gate dielectric, on top of which the QD was located). It is not unusual to observe differences in the size of the Coulomb diamonds, as in the present case. They are a consequence of the background charge in the silicon oxide surrounding the QD, which may vary when applying the gate potential, as the charge traps in the oxide get or release electrons. The biggest dimension of the Coulomb diamond in the V_G axis is related to the gate capacitance ($\Delta V_G = e/C_G$), whereas the capacitance between the quantum dot and the drain (source) electrodes can be extracted from the positive (negative) slope of the diamonds $(dV_{SD}/dV_G)^+ = C_G/(C_G+C_D)$ and $(dV_{SD}/dV_G)^- = -(C_G/C_S)$. Based on these expressions, we extracted the following values from the slopes of the diamonds in Figure 5.6-a: C_G = 3.72 × 10^{-20} F, C_S = 6.48 × 10^{-19} F and C_D = 1.29 × 10^{-18} F, which agree fairly well with literature. As expected, the capacitance with the gate electrode was one or two orders of magnitude smaller than with the source and drain electrodes. This was consistent with the approximate distances from the QD to the gate (150 nm, the thickness of gate oxide), source (a tunnel barrier of a few nm) and drain (similar to the source) [2-3, 5]. Similarly, the periodicity of the diamonds in the V_G axis is related to the gate coupling, that is to say, the efficiency with which the electrostatic energy of the QD is shifted by the gate. The coupling improves when the distance between the gate and the QD is minimized and the electrostatic field is more intensely felt by the latter. Using the expression $\Delta V_G = E_C/e\beta$ we can extract an approximate value of 0.019 for the gate coupling (β) in diagram a). This number is close to the value expected for a SiO_2 gate dielectric of 150 nm thickness [5].

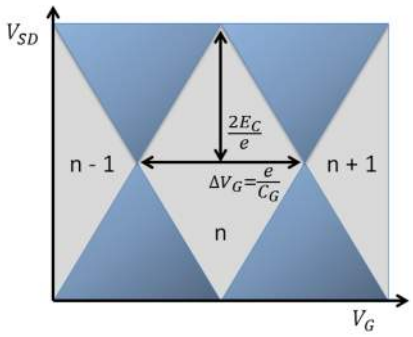

Figure 5.7. Schematic view of a stability diagram. This sketch shows how to extract and calculate the approximate values of the charging energy and the gate total capacitance from the dimensions of the Coulomb diamonds.

We must note that although approximately a 71 % of our devices showed Coulomb blockade, only around a 16 % of them displayed clearly distinguishable Coulomb diamonds, consistent with the charge transport through a single quantum dot. The formation of several QDs conducting in parallel was often observed, giving as a result a pattern of superposed diamonds in the stability diagram that was not appropriate for extracting useful information about the QDs (see Figure 5.8). In some devices the conductance features did not respond to the variation of the gate voltage. This was probably due to the formation of unsuitable geometries during electromigration, which lead to poor coupling of the QD with the gate electrode [5].

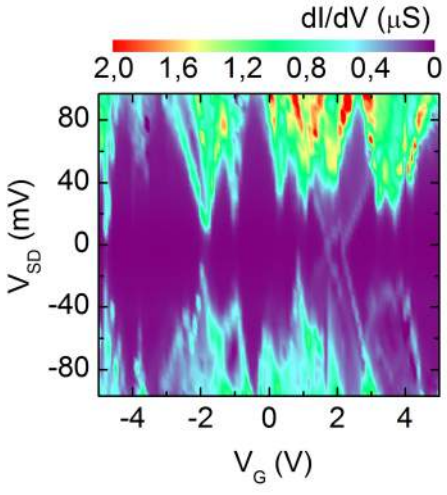

Figure 5.8. Stability diagram with superposed Coulomb diamonds. Stability diagram showing a conductance pattern of a SET with several QDs conducting in parallel. Extracting useful information becomes practically impossible.

5.3.3. Higher order tunneling processes and Kondo effect

The obtained SETs showed a non-zero current inside the Coulomb diamonds, even if in these regions the V_{SD} was not sufficient for overcoming the Coulomb blockade state. This is directly related to the coupling regime, which depends with the resistance of the tunnel barriers between the QD and the source-drain electrodes (R_S, R_D). When R_S or R_D is close to R_0 (where $R_0=h/2e^2$ is the resistance of a single conductance channel) the device is in the strong coupling regime, where the QD is not sufficiently isolated to avoid charge fluctuations. The number of electrons of the QD is not fixed in this state and therefore, the Coulomb diamonds cannot be properly defined. When R_S, $R_D >> R_0$ the device is in the weak coupling regime, in which by definition the conditions for Coulomb blockade are fulfilled. It is generally considered that there is an intermediate coupling regime, in which electrons are able to access the quantum dot through higher order tunneling processes even when the path for resonant tunneling is closed. This occasionally results in the observation of conductance features in the blockaded regions, such as the peak at zero bias shown in Figure 5.9, which could correspond to a Kondo resonance. The Kondo effect is a particular case of elastic co-tunneling process involving spin-flip events [2, 7] .

As explained before, the number of electrons in the QD is fixed inside the Coulomb diamonds. When the QD is blockaded with an odd number of electrons, it has a net spin and we can observe magnetic effects arising from the presence of this isolated unpaired spin, as it is the case of the Kondo resonance. This enhancement of the conductance arises from the attempt of the conduction electrons in the source and drain electrodes for screening the unpaired spin. The conduction electrons in the leads couple antiferromagnetically with the unpaired spin in the QD by means of co-tunneling processes, resulting in a singlet state. The resonance peak at zero bias in the differential conductance curve resulting from these co-tunneling events has two specific characteristics: its intensity increases when lowering the temperature and it splits by Zeeman effect in the presence of a magnetic field. The Kondo effect has been observed in quantum dots of different nature, such as carbon nanotubes, semiconducting QDs, metallic QDs or molecules.

We observed features that could most likely be due to the Kondo effect in around a 16 % of our devices with Coulomb blockade characteristics. Unfortunately, the observed feature was lost when trying to explore the transport at different temperatures or higher V_{SD} regions, probably due to a rearrangement of atoms in the vicinity of the QD and the subsequent weakening of the coupling with the electrodes. Therefore, no further characterisation could be done to verify the nature of the observed peak. We note that in general, the properties of our devices were easily altered when changing the temperature or applying higher V_{SD} and hence, their SET characteristics (Coulomb diamond pattern) were easily degraded or lost.

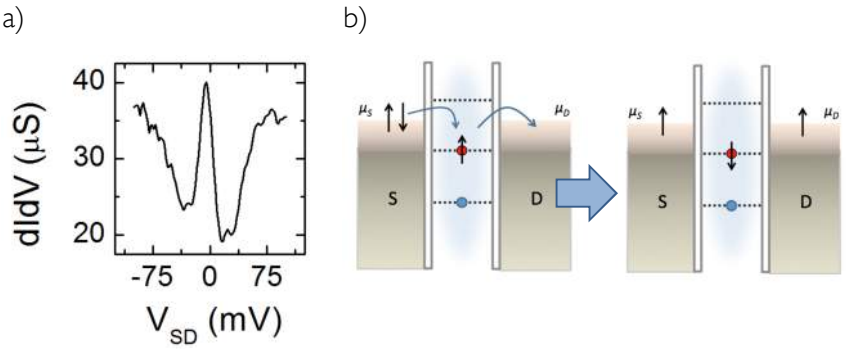

Figure 5.9. Evidences of higher order tunneling processes. Enhancement of the zero bias conductance observed for a device in the OFF state at T=1.8K. a)The peak at V_{SD} = 0 is a consequence of the zero-bias enhancement of the charge transport that could correspond to a Kondo resonance. b) The sketches depict the underlying elastic co-tunneling process, which involves the simultaneous movement of two electrons and a spin-flip event. As a result, an electron is effectively transported from source (S) to drain (D) leading to an antiferromagnetic configuration between S, D and the unpaired spin in the QD.

5.3.4. Unusual conductance features

We observed unusual conductance features in some devices (around 20 %). Their I(V) curves were non-linear, although with features different from the ones corresponding to Coulomb blockade. The corresponding differential conductance curves showed a series of sharp resonance peaks, which were previously observed by Scott *et al.* [14] in electromigrated Pd nanowires. These features appeared in two different sets, which were symmetrically located with respect to zero bias. The first set appeared at V_{SD}<0.2 V and comprised a cluster of small peaks of different sizes. The other one consisted of two bigger peaks (with several μS intensity) located around V_{SD}=0.4 V. Same as reported in literature, both the intensity and position of the observed peaks depended on temperature. They shifted to lower V_{SD} values and decreased in size when increasing the temperature. The low-bias features became imperceptible at a temperature of about 4 K, while the high-bias peaks were visible up to 10 K. However, neither of these features seemed to be affected by an applied magnetic field or gate voltage. The origin of these features remains still unclear, although the authors of the cited work [14] ruled out several physical mechanisms after exhaustive experimental and theoretical studies. Inelastic tunneling processes involving spontaneous magnetization were finally proposed as a possible explanation. This hypothesis seems to be consistent with the onset of ferromagnetism predicted for palladium nanoparticles and atomic-sized contacts [22-23]. The origin of the observed features remains unsolved for the moment and further experiments would be needed for a full understanding.

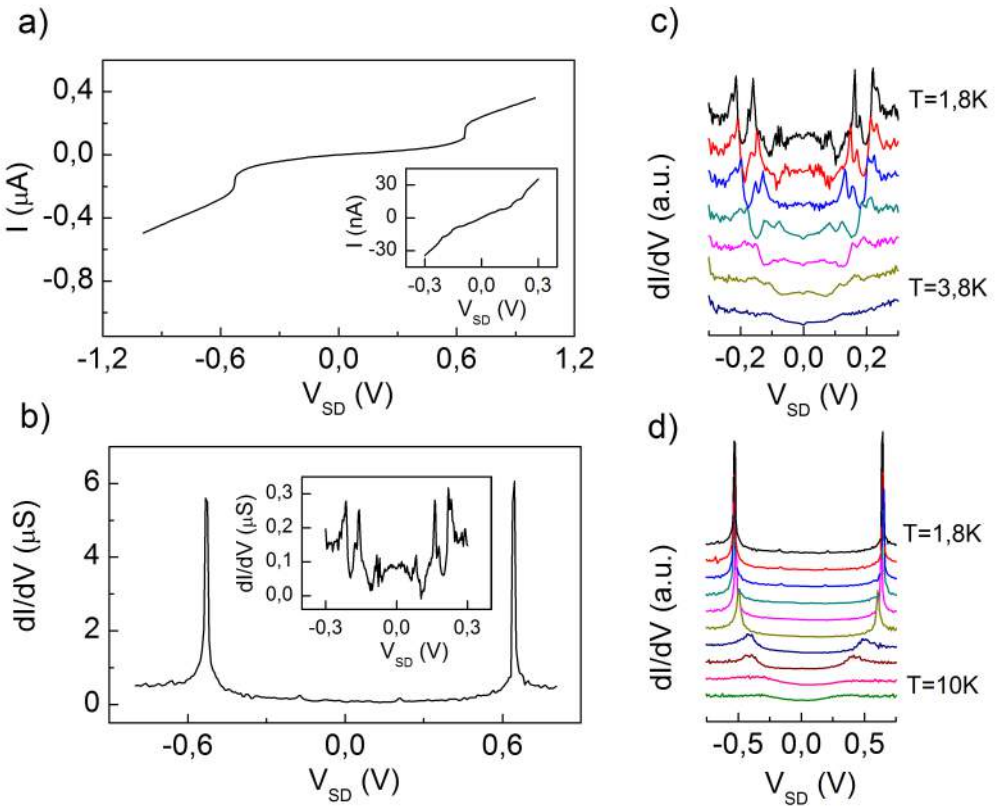

Figure 5.10. Unusual conductance features in palladium devices. Unusual features in the form of symmetric and sharp resonance peaks appeared in a number of palladium devices. a) I vs VSD curve measured for a device with unusual features. The low bias region of the same curve is shown as an inset. b) Differential conductance vs VSD curves calculated from the curve in a). Again, a detail from the low bias region is shown as an inset. c) and d) Evolution of the position and intensity of the differential conductance peaks as a function of temperature in arbitrary units (a.u.); c) shows the peak cluster at low bias while d) shows the single pair of peaks at high bias.

These sharp resonances had only been observed in electromigrated palladium devices, according to literature. Consequently, they had been attributed to an intrinsic phenomenon, particular only to this metal. Interestingly, we also observed similar features in a nickel device (Figure 5.11), which pointed toward the fact that such peculiarities in the conductance could perhaps be attributed to the formation of specific nanostructures, instead of to the inherent properties of palladium itself. We note the resemblance of the observed differential conductance peaks with the ones arising from the Van Hove Singularities (VHS) in the DOS of a one dimensional system, such as a carbon nanotube. The VHS would account for the sharp peaks presented in the differential conductance curves of Figure 5.10.

In the case of the nickel device of Figure 5.11, the peaks at low bias are not so well defined and intense as those observed in the palladium device in Figure 5.10. Their shape and intensity are closer to the traces recorded at higher temperatures in the palladium devices (see the graph on the right in Figure 5.10-c). Regarding the peaks at high bias, we observe that they are sharper and fairly asymmetric, compared to the ones observed in palladium. They show a very abrupt drop when decreasing bias, while the decay is more gradual for increasing bias. Qualitatively speaking, this detail resembles again the typical profile of the VHS, as can be seen in Figure 5.11 (panels b and c). For the sake of comparison, we include in the same figure two graphs taken from literature, which show the features corresponding to the density of states (DOS) of single walled carbon nanotubes measured by STM. We note that the size of the gaps between the peaks reported in the cited work (0.4 to 1.9 eV) are of the same order of magnitude as the ones measured in our structures (0.2 to 1.2 eV, depending if we refer to the set of peaks at lower of higher bias) [24].

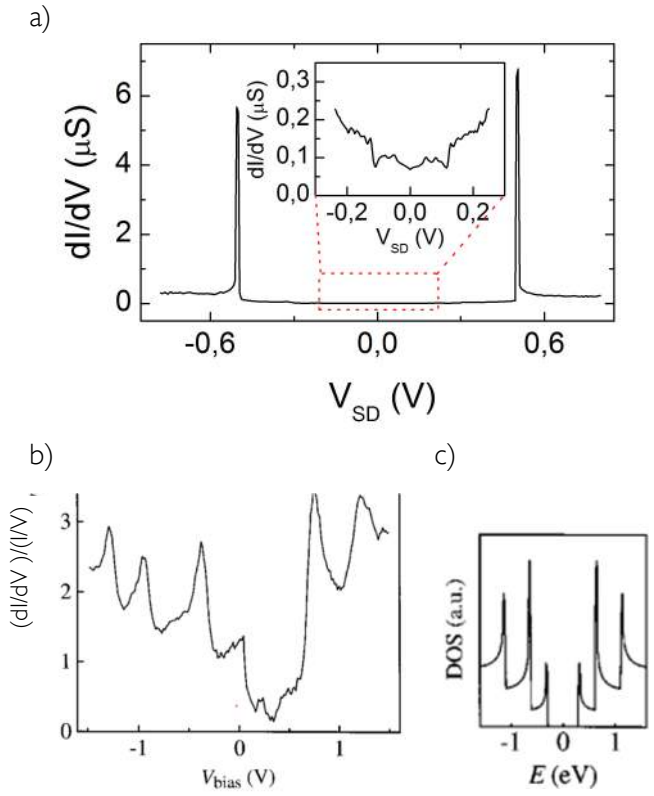

Figure 5.11. Unusual conductance features measured in nickel devices. a) Sharp resonance peaks in the differential conductance curve of an electromigrated nickel device at T=1.8K. The resemblance of these features to the peaks observed in several palladium devices (such as the one in Figure 5.10) seems to indicate that they belong to the same type of resonance or excitation. b) Density of states (DOS) of single-walled carbon nanotubes (SWCNT), measured by STM. The observed peaks correspond to van Hove singulatities at the

onset of one-dimensional energy bands, confirming the one-dimensional nature of the charge transport within the nanotubes. c) Theoretical calculation of the DOS for a semiconducting SWCNT, showing a good agreement with the experimental results in panel b. (Graphs in b and c are taken from [24]).

5.4. Ferromagnetic alloy SETs

Preliminary tests of electromigration with palladium alloys were also carried out following the same strategy as explained for palladium devices.

The fabrication was done following the same procedure as in the case of palladium devices (explained in section 5.2), except for the metal deposition. We deposited 25 nm of a palladium alloy with a 50 atomic percent content of nickel ($Pd_{0.5}Ni_{0.5}$) by co-sputtering of a Pd and Ni targets. The co-sputtering procedure was carried out following the instructions of the Nanomagnetism Group of CIC nanoGUNE. A calibration curve of the deposition rate *versus* the applied power was first done for each metal independently. Afterwards, we selected the power needed for depositing a total thickness of 25 nm with the required composition.

After electromigration we observed Coulomb diamonds in several devices (Figure 5.12), confirming that the procedure stablished for palladium (section 5.2) was also valid for alloyed nanowires. This opened up the possibility of fabricating and studying a series of alloyed SETs covering the whole range from pure Pd to 50 atomic percent of Ni content. We also performed a few electromigration experiments in pure Ni nanowires, in which we formed tunnel junctions, but no traces of Coulomb blockade were observed. Therefore, we expect the yield of SET fabrication by our method to drop as the amount of Ni is increased, although we have not stablished a limit. Our results hint that Pd could be used as a medium for driving the formation of SETs containing small amounts of magnetic elements.

Apart from assisting in the formation of SET structures Pd is expected to play a role in the magnetic properties, due to a possible onset of magnetism in the nanoscale. However, studying electronic correlations at this level requires resolving individual electronic energy levels of the metallic grains [2]. This last condition implies working at temperatures below 1 Kelvin, which for the time being is beyond our experimental capabilities.

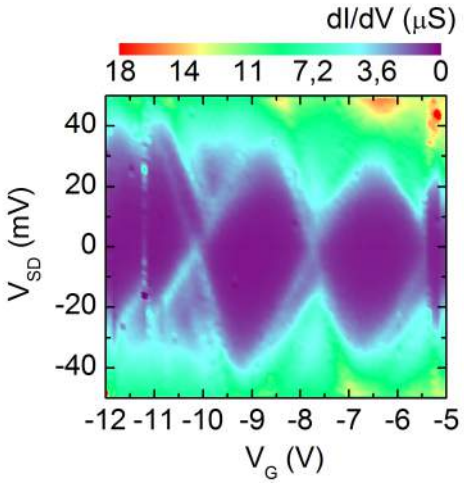

Figure 5.12. Stability diagram of an alloyed Pd SET. Electromigrating alloyed Pd nanowires ($Pd_{0.5}Ni_{0.5}$) also resulted in the formation of SETs. The sudden jumps in the conductance features observed around VG=11 V and VG=6.6 V are probably due to fluctuations in the background charge. These fluctuations are typically produced by charge-traps in the surrounding silicon dioxide insulator.

5.5. Conclusions

We have obtained devices working in the single electron transport regime by performing feedback-controlled electromigration of palladium and palladium-nickel alloy nanowires.

Breaking palladium nanowires at low temperature by a gradual electromigration process resulted in the simultaneous formation of closely separated nanoelectrode pairs (source and drain) and quantum dots, probably in the shape of metallic nanoclusters. These QDs formed into the inter-electrode channel and constituted the active element of each device and ruled the electron flow between source and drain electrodes. The amount of current that was able to flow through the QD was limited to one electron at a time by electrostatic effects. The charge transport of the fabricated devices showed Coulomb blockade characteristics and their source-drain current could be modulated by electrostatic gating, thus forming SETs. On the other hand, following the same experimental procedure, we obtained devices with unusual conductance features, which we hypothesised to be due to the formation of one-dimensional structures as a consequence of electromigration. SETs were obtained with a 71% yield, while 20 % of the devices presented unusual conductance features. Around a 8 % of the electromigration experiments resulted in devices with no measurable current.

The formation and subsequent measurement of these nanostructures inside a cryostat had the advantage of reducing the number of fabrication steps. Additionally, we showed that the fabrication method could be extended to palladium-based alloys, such as $Pd_{0.5}Ni_{0.5}$, which offer the opportunity of combining magnetic effects with single electron physics. Precisely, this method could help circumventing the main difficulty for obtaining SETs based on magnetic nanostructures, namely, that they tend to oxidize due to their enhanced reactivity in comparison to bulk metals. Hence, the proposed approach, in which the samples are fabricated and measured in situ, would be most convenient for studying single electron physics in non - noble metals.

It must be noted that the formation of SETs by electromigration depends on the experimental conditions, but most importantly, it strongly depends on the nature of the metal itself, as well as on its grain structure. Thus, the use of the proposed fabrication method is limited to the study of those metals (or alloys) that are apt to form small clusters or nanoparticles due to their material properties. Our results suggest that it would be possible to prepare SETs of Pd alloyed with small quantities of different elements (for instance Fe, Co or Al), which is an attractive prospect.

Last, we must note that the performance of the obtained devices can differ greatly from one another, as it generally happens with nanoparticle-based SETs, regardless their fabrication method. This fact limits their use mostly to research applications.

5.6. References

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Chapter 6

We utilised the combination of EBL and electromigration for obtaining devices for spintronic research. The work presented in this chapter has been developed thanks to the experience on electromigration that we acquired in previous stages of this thesis (see Chapter 4). Apart from this, the dedicated effort of several members of our group in the research of the injection, transport and manipulation of pure spin currents in metals was essential for realising the experiments described in the following sections.

We must say that the work concerning this project has still not been concluded, due to time constraints. The partly random nature of electromigration experiments typically demands large statistics in order to achieve conclusive results. In this case, it was not possible to attain a sufficient number of successful experiments within the timeframe of this thesis. Therefore, part of this chapter is devoted to the proposal of further work.

After an introduction to spintronics and lateral spin valves (Section 6.1), we describe the experiments originally proposed for this project (Sections 6.2 and 6.3). Afterwards, we report the issues we encountered during their development and we propose further experiments for pursuing the initially intended goals (Section 6.4). These experiments, as well as several others that stemmed from the initial proposal are currently under development.

6. Fabrication of lateral spin valves with nanoconstrictions

In previous chapters we described strategies for the fabrication of nanodevices with applications in different branches of nanoscience research, such as electronics and photonics. After that, we decided to merge our new fabrication skills with the previous experience of our group in the study of spin transport in metals.

We thus proposed a new project aimed at fabricating devices for spintronic research, more precisely, lateral spin valves, by the combination of EBL and electromigration.

6.1 Brief introduction to spintronics

It has been predicted that the constant downscaling of the current silicon-based transistor technology (CMOS), which has been going on for almost six decades [1], will soon encounter its limit. Therefore, there is an active search for alternatives to conventional

electronics, *among which spintronics (or spin electronics) is one of the most popular examples.*

*Spintronics propose using both the charge and the spin of electrons for information processing. Magnetic random access memories and hard-disc read-heads constitute two very successful technological applications of spintronics, which are based on spin-polarised charge currents. However, the main potential of spintronics resides in the possibility of building charge-less devices and circuits, uniquely based on spin currents. The advantages of using pure spin currents would be a dramatic decrease in power consumption and an enhanced data processing spee*d [2,3].

The basis of spintronics: spin polarisation

The spin is a quantum mechanical property of elementary particles, which is understood as an intrinsic angular momentum of the electron $\vec{S}$. It is quantized along a preferential direction, since $S_z = m_s\hbar$, where $\hbar$ is the reduced Plank's constant ($\hbar = h/2\pi$) and m_s is the *spin projection quantum number*, which can only have the values $m_s = +\frac{1}{2}$ or $m_s = -\frac{1}{2}$ (associated to the "spin-up" and "spin-down" states, respectively) [4]. The spin angular momentum of electrons has a magnetic moment associated to it. Ferromagnetic (FM) materials present a net macroscopic magnetization ($\vec{M}$), which arises from the sum of the magnetic moments of all electrons that align in a preferentially parallel orientation via the exchange interaction [5]. Thus, FM elements (Ni, Co and Fe) have different spin-up or spin-down electron populations, the highest of which is typically called "majority spin electrons". This occurs due to a shift between the spin sub-bands of the inner shell electrons (*3d* electrons) [6], which are the ones that effectively account for the exchange interaction.

An important consequence of the sub-band shift occurring in FM elements is that the electronic density of states (DOS) at the Fermi energy is different for spin-up and spin-down electrons. Therefore, the Fermi velocities and conductivities are also different in each case, which allows treating the conduction of spin-up and spin-down electrons in a FM metal as if occurring through two parallel and independent channels. This is the basis of the so-called *two-channel model* [7]. This characteristic of FM materials results in their ability to induce a net spin polarisation (α_F) in the electrical current that circulates through them [8]. In other words, the current comprises a net spin flow, as well as a charge flow.

6.1.1. Lateral spin valves

We could say that spin valves are the archetypal spintronic devices. The most simple spin valve is a trilayered structure consisting of two FM metals spaced by a non-magnetic conductor (NM). The electrical resistance across this trilayer can change dramatically

depending on the relative orientation of the magnetisations ($\overrightarrow{M_1}$, $\overrightarrow{M_2}$) of the two FM metal layers. This effect, known as giant magnetoresistance (GMR), can be observed when circulating a current through the spin valve and varying the orientation of $\overrightarrow{M_1}$ and $\overrightarrow{M_2}$ with respect to each other by an applied magnetic field [9, 10].

The GMR effect is based on spin polarised currents circulating through spin valves, as described above. In other words, the electron spin and charge information are simultaneously transferred. However, spin and charge currents can be decoupled, creating devices that work with pure spin currents. For instance, lateral spin valves (LSV) are devices that allow generating pure spin currents by electrical spin injection [11, 12], based on the same principle as conventional spin valves. These devices consist of two FM electrodes bridged by a NM channel of a given length, (as shown in Figure 6.1).

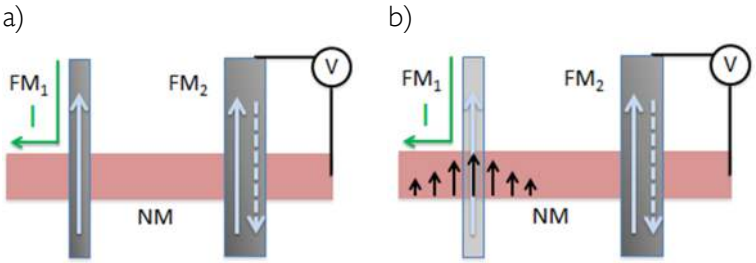

Figure 6.1. Working principle of a lateral spin valve. Schematic view of a LSV showing the configuration for measuring the non-local resistance. The current (I) is injected into an end of the NM channel through a FM electrode (FM1) and a voltage (V) is detected at the opposite end of the same NM channel (towards which there is no net charge flow) by means of another FM electrode (FM2). a) The magnetisation of FM2 can be in a parallel (solid arrow) or antiparallel (dashed arrow) orientation with respect to FM1, depending on the magnitude and direction of the applied magnetic field. b) Sketch showing the diffusion of the spin accumulation inside the LSV (represented by small black arrows). The spin current diffuses from the FM/NM interface towards both ends of the channel and decays due to spin relaxation in the NM material.

The working principle of LSVs relies on the possibility of injecting an electric current and measuring a voltage in a non-local configuration, thus decoupling the spin from the charge. Applying an electrical current between the first FM electrode (injector, FM_I) and one end of the NM channel injects a spin polarised current into the latter. In a NM both spin sub-bands and consequently, the conductivities for both spin orientations are equal. This situation leads to an imbalance of spin-up and spin-down electron populations (*i.e.*, a spin accumulation) in the NM channel, near the interface with FM1 (Figure 6.2). This spin imbalance is likewise reflected as a difference between the spin-up and spin-down electrochemical potentials ($\mu_s = \mu_\uparrow - \mu_\downarrow$). The pure spin current diffuses isotropically inside the NM, driven by the gradient of the spin-up and spin-down electrochemical potentials. In the present case, the spin current diffuses towards the two ends of the NM channel [Figure 6.1 b]. A new spin accumulation is then created in the area of the NM

channel that is close to the interface with the second FM electrode (detector, FM_2). This accumulation, also seen as a difference between the electrochemical potentials of both spin orientations ($\Delta\mu_s$), creates a proportional voltage at the FM_2/NM interface. The voltage ($V_s = \Delta\mu_s/e$) can then be measured between the FM_2 and the other end of the NM channel (see Figure 6.1 b) [13]. We note that the detected non-local voltage is exclusively due to the pure spin current diffusing along the NM, since there is no net charge current circulating through the channel between the two FM electrodes.

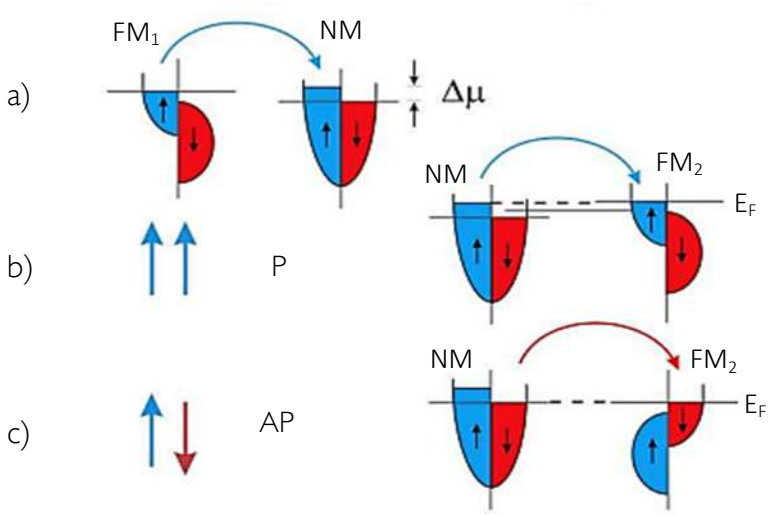

Figure 6.2. Schematic representation of spin injection and detection in a LSV. a) Spin injection from FM1 to the NM. The sketches show the DOS of 3d spin sub-bands in the injector FM1 (shifted with respect to each other due to the exchange interaction) and the s spin sub-bands in the NM. The spin accumulation induced in the NM is observed as a difference between the electrochemical potentials of both spin orientations ($\Delta\mu_s$), which should otherwise be equal. b) and c) show how the spin accumulation induced in the NM is detected by the FM2 (also represented by the 3d spin sub-bands), in the case of a parallel (P) and antiparallel (AP) orientation of the magnetisations of FM1 and FM2. The Fermi level (EF) in FM2 equilibrates with the spin-up Fermi level of the NM for the P magnetisation orientation and with the spin-down Fermi level for the AP magnetisation orientation. The difference $\Delta\mu_s$ in the NM sub-bands is thus detected as a voltage at the FM2/NM interface ($V_s = \Delta\mu_s/e$). Figure taken from [14].

Acquiring a spin signal

We then define a non-local resistance by normalising the measured non-local voltage with respect to the injected current ($R_{NL} = V_s/I$). Its magnitude is proportional to the spin accumulation at the FM2/NL interface and therefore, it directly depends on the amount of spin current that is diffusing along the NL channel. Same as it happens with the electrical resistance in a conventional spin valve, R_{NL} in a LSV depends on the relative orientation of the magnetisation of the FM electrodes. Thus, we can control R_{NL} by changing the

magnetisations from parallel (P) to antiparallel (AP) state. This is achieved by applying the adequate value of a magnetic field in the direction of their longest dimension (easy axis). Designing elongated electrodes with slightly different widths results in a sharp switching of the magnetisation (since the electrode comprises a single magnetic domain), as well as different coercive fields (H_C) for FM1 and FM2. This last characteristic allows switching the magnetisation of each FM electrode independently, achieving stable P and AP states. R_{NL} keeps the same magnitude, although its sign changes from positive (in P state) to negative (in AP state) as we sweep an external magnetic field (H). This change of sign occurs at the same values of the applied magnetic field either when sweeping in the positive or in the negative direction.

The curve resulting from representing R_{NL} *vs* H shows the characteristic response (also known as non-local spin valve effect) of a LSV (see Figure 6.3). This response is typically quantified by calculating the difference between the R_{NL} values at the P and AP state, which is known as the spin signal (ΔR_{NL}).

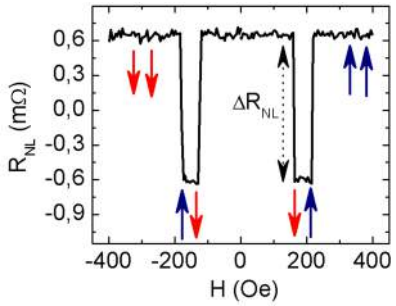

Figure 6.3. Measurement of the spin signal in a LSV. Evolution of the non-local resistance (R_{NL}) as a function of an external magnetic field (H) in a LSV. The solid (dashed) trace correspond to sweeping the applied field from positive to negative (negative to positive) direction. The relative orientations (P or AP) of the FM electrodes corresponding to each segment are represented by short arrows. The characteristic quantity known as spin signal (ΔR_{NL}) that is usually extracted from these curves is also shown in the graph.

Estimating the efficiency of spin transport

The efficiency of spin transport in a given material is quantified by the spin-diffusion length (λ_N) and the spin-relaxation time (τ_{sf}), (related by $\lambda_N = \sqrt{D\tau_{sf}}$, where D is the diffusion constant). They refer to the distance and time through which a spin current can circulate without losing its polarisation. In metals, the mechanism that accounts for spin relaxation (Elliot Yaffet mechanism [15, 16]) is based on the interaction of electron spin with the local magnetic field created by the metal ions in the crystal lattice. This interaction happens by means of the spin orbit coupling (SOC) during the momentum scattering events. Thus, the materials with low atomic number (Z), high crystallinity and high purity

(especially, as refers to the absence of magnetic impurities) are desirable for an efficient spin transport.

Values of λ_N and τ_{sf} for a given material can be obtained by fitting the measured spin signal to its corresponding mathematical expression. An expression for the non-local voltage (V_s) was derived from solving the one-dimensional spin-dependent diffusion equation proposed by Valet and Fert [17]. Considering spin diffusion in only one dimension is reasonable in the spin valves fabricated in this project, given the typical dimensions of the NM channel (from 200 nm to microns in length, around 100 nm in width and around 40 nm in thickness, respectively).

Different approximations are applied to the solution of the diffusion equation, depending on the resistance regime of the FM/NM interface [18]. The following two situations are usually considered in experiments:

- Transparent interfaces: $R_I \ll R_F,\ R_N$.

This situation occurs when there is an ohmic contact between the FM and the NM and thus, the interface resistance (R_I) is negligible. Usually, the spin resistance of the FM (R_F) is also much lower than that of the NM channel (R_N). The following expression is thus obtained for the spin signal:

$$\Delta R_{NL} = \frac{4\, R_N\, \alpha_F^2}{\left[2 + \frac{R_N\,(1-\alpha_F^2)}{R_F}\right]^2 e^{L/\lambda_N} - \left[\frac{R_N\,(1-\alpha_F^2)}{R_F}\right]^2 e^{-L/\lambda_N}} \qquad (6.1)$$

L refers to the distance between both FM electrodes. The spin resistance $R = \lambda\, \rho / w\, t$ (where ρ is the electrical resistivity and $w\, t = V$ is the volume through which the spins can diffuse) can be understood as the tendency of each material (FM or NM) for absorbing spins.

We note that in this expression the spin signal depends on the ratio R_N/R_F and therefore, it becomes clear that the spin injection is not efficient when $R_N \gg R_F$. According to the equation, the spin signal decays exponentially as L is increased. This is in perfect agreement with experimental observations.

- Tunneling interfaces: when $R_I \gg R_N \gg R_F$

This situation enhances the spin injection in the NM, since the spins are prevented from returning back to the FM through the interface and relaxing there. The following expression is obtained for the spin signal:

$$\Delta R_{NL} = P_I^2 R_N \, e^{-L/\lambda_N} \tag{6.2}$$

In this equation $P_I = P_{I1} = P_{I2}$ corresponds to the polarisation of the FM/NM interfaces (considering they are equal for the injector and detector FM). This quantity accounts for the spin injection efficiency of the interface.

We note that unlike in the case of transparent interfaces, the spin signal now only depends on R_N, instead of on the ratio R_N/R_F.

6.1.2. Spin transport in confined systems

The interest of building low dimensional systems for spin transport relies in the enhancement of the spin signal due to the reduction of the effective volume in which the created spin accumulation diffuses. This occurs because restricting the dimensions (for instance, the cross section) of the NM channel below the spin diffusion length (λ_N) helps directing the spin accumulation towards the detector, reducing spin relaxation in other areas [19]. Pure spin transport has been widely studied in one dimensional (1D) structures of different nature, such as metallic nanowires [12,20], carbon nanotubes [21] or graphene nanoribbons [22]. Interesting results have also been obtained from studying spin polarised charge transport in zero dimensional (0D) systems or quantum dots (QD) [23, 24]. For instance, introducing spin dependence effects in systems with single electron transport regime results in the so-called magneto-Coulomb effects [25, 26].

The measurement of tunnelling magnetoresistance (TMR) between closely distanced nanoelectrodes [27, 28], constitute other example of spintronic studies in low dimensional systems. The TMR effect works in a similar manner as GMR, although it corresponds to the case when the two FM layers or electrodes are spaced by an insulator, instead of by a NM conductor. The resulting structures are known as magnetic tunnel junctions (MTJ) [29] and they have demonstrated that the spin polarisation is conserved when electrons tunnel through a thin insulator spacer.

We note that most of the reported experiments, especially those regarding 0D systems and TMR measurements, are based on spin polarised charge currents, instead of pure spin currents.

6.2 Fabrication of lateral spin valves for studying pure spin currents in confined systems

Inspired by the remarkable results on spin polarised charge transport in low dimensional systems reported by several groups [23-29], we proposed fabricating devices for realising similar experiments with pure spin transport.

We thus combined EBL and electromigration in order to obtain metallic LSVs with nanoconstrictions, nanogaps and other nanostructures. The fabrication process is briefly described in this section and we refer to previous chapters (Chapter 3, to 5) for further details.

We identified the following main requirements for achieving our objectives:

- The metal employed for constituting the NM channel had to be adequate for yielding the desired structures by electromigration.
- At the same time, the intrinsic spin diffusion length of the NM metal had to be high.
- The electromigration process had to be localised between both FM electrodes (ideally, exactly in the middle of the NM channel).

Among the metals we studied in our experiments (Chapter 4), copper ($\boldsymbol{\lambda}$N~ 1 µm) and gold ($\boldsymbol{\lambda}$N~100 nm) are the ones that best suited to these conditions. On the other hand, we patterned a constriction by EBL in the middle of the NM channel, in order to localise the electromigration process at this spot. In principle, the electromigration triggers in the place where the critical current density is first achieved, for instance, in the place where the cross section is smaller.

6.2.1 Electron beam lithography

The first fabrication stage involved two steps of standard EBL on highly doped silicon substrates coated with 150 nm of thermal silicon oxide. The optimisation of the EBL process for the fabrication of metallic LSVs was carried out by other members of our group, who work in a parallel research line devoted to spin transport in metals [30, 31].

Both EBL steps were carried out on a double layer polymethyl metacrylate (PMMA) resist system spun onto the thermal SiO2 surface, followed by metal deposition and lift-off (for further details see Chapter 4, section 4.2). Permalloy (an alloy with about 80% nickel and 20% iron) was chosen for constituting the FM electrodes and the NM channel was fabricated with copper. The former was chosen due to its spin injection efficiency [32], whereas the latter is one of the metals with longest measured spin diffusion lengths ($\boldsymbol{\lambda}$N ~

1 µm). Apart from that, we chose copper based on our results and observations in previous electromigration experiments (Chapter 4). Macroscopic contact pads, consisting of 25 nm thick gold on top of a 2 nm titanium adhesion layer, were defined prior to EBL by a standard photolithography process (we are going to skip the explanation of this step).

The general design of our devices is shown in Figure 6.4.

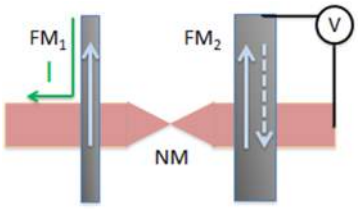

Figure 6.4. LSV with a constricted NM channel. The designed LSVs are based in the same working principle explained in Figure 6.1. The NM channel has a constriction in the middle of the segment between the two FM electrodes, with the purpose of localising the electromigration process that is carried out in a second fabrication stage.

We first patterned two elongated permalloy electrodes at a distance of 300 nm and parallel to each other. They had a thickness of 25 nm, a similar in length (around 4 µm) and slightly different in width (130 nm and 90 nm, respectively), which resulted in different coercive fields. This allowed controlling the relative orientation of their respective magnetisations by applying an external magnetic field in the direction of the easy axis (parallel to their longest dimension). We then overlayed a 120 nm wide and 40 nm thick copper stripe on top of the permalloy electrodes in a second lithography step. The narrow copper stripe helps channelling the diffusion of spins and results adequate for the approach utilised in the 1D diffusion equation (Section 6.1.1).

We fabricated devices with and without constriction, in order to determine if there was any difference between the spin signal measured in either of them before subjecting the devices to electromigration.

The size of the patterned constrictions varied approximately from 30 to 55 nm in width and around 40 nm in thickness. We could in principle obtain smaller constrictions by performing the EBL with a higher beam voltage (for instance, 20 kV). However, overlaying the second lithography layer on top of the first one (composed of 25 nm thick permalloy structures) turned out to be rather difficult and time consuming. This happened because the images obtained at 20 kV with the employed metal and thickness did not have enough contrast for performing the fine alignment properly. The cross section of the patterned nanoconstrictions was very sensitive to any change in the effective dose, developing conditions, evaporation angle during metal deposition and the size of the grown metallic

grains. Sometimes open gaps (instead of constrictions) were formed due to undesired shadow masking effects during metal deposition (see Chapter 3, section 3.5).

Optimising the quality of the interfaces and the deposited metallic films required special attention, since the performance of LSVs depends critically on these characteristics [33] (see Section 6.1.1). For this reason, the metal deposition was entirely done in ultra-high vacuum conditions, which have shown devices with optimum performance, according to previous experience in our group [34]. The samples were subjected to argon ion milling at a grazing incidence angle after the first lithography step. This process was necessary to remove the sharp edges remaining around the permalloy electrodes after metal deposition and lift off. If these edges were not removed they led to open circuits or discontinuities when overlapped with the second lithography layer. On the other hand, the FM/NM interface was cleaned by performing a mild argon ion milling immediately before depositing the metal for the second lithography layer. This allowed removing the materials (resist, solvents, *etc.*) that could remain after the previous lithography step. The optimisation of this step was crucial for achieving transparent interfaces and an efficient spin injection [30]. Table 6.1 summarises the steps of the whole EBL process.

Table 6.1. Summary of the EBL process for the fabrication of LSVs in two steps. The following protocol was optimised by other members of our group in a parallel research line, putting special attention in the metal evaporation and interfacial treatments steps (steps 5, 7, 10, 11).

STEP	PROCEDURE
1) Substrate preparation	10 X 10 mm Si chips (with 150 nm SiO_2 coating) were cleaned with the application of ultrasounds in acetone and IPA (5 minutes in each solvent). Drying with nitrogen gun.
2) Resist processing	Application of a 495 PMMA A2 /950 PMMA A2 bilayer. Spin coating at 4000 rpm during 1 minute, followed by 1 minute baking in a hot plate at 190°C (for each layer).
3) e-beam exposure	1st step: Exposure of FM electrodes and alignment marks with a current of ~20 pA (corresponding to an aperture of 10 μm and an acceleration voltage of 10 kV). Utilised dose: 150 $\mu C/cm^2$. This layer was aligned by 3 point adjustment to a set of macroscopic contact pads pre-patterned by photolithography (consisting on 25 nm of gold, with a titanium adhesion layer of 3 nm).
4) Developing	Immersion in MIBK/IPA 1:3 for 1 minute, followed by an IPA rinse for 10 seconds and drying with a nitrogen gun.
5) Metal deposition	E-beam evaporation of 25 nm of Py in an UHV chamber. Conditions: P_0 ~5×10^{-9} mbar (base pressure), r ~ 0.69 Å/s (deposition rate), P ~2×10^{-8} mbar (evaporation pressure).
6) Lift off	Immersion in acetone (1 to 2 hours). Gently squirt with acetone (while still immersed) for removing the attached metal, periodicallly inspecting with optical microscope. Immersion in IPA for rinsing. Drying with a nitrogen gun.
7) Ar ion milling	The Sample was subjected to 180 seconds or Ar ion milling at a grazing angle (at 10 degrees with respect to the substrate surface and rotation of 15 rpm). The

	purpose was removing the sharp metallic edges or "fringes" protruding around the structures.
8) Resist processing	Repeat step 2
9) e-beam exposure	2nd step: Exposure of NM channel with a current of ~20 pA (corresponding to an aperture of 10 μm and an acceleration voltage of 10 kV). Utilised dose: 150 μC/cm^2. 3 point adjustment and fine alignment procedures were used for aligning this layer with the pre-patterned structures.
9) Developing	Repeat step 4
10) Interface cleaning	The Sample was subjected to 30 seconds or Ar ion milling (at 80 degrees with respect to the surface and rotation of 15 rpm). The purpose was cleaning the surface that would be in direct contact with the second metallic layer. This process was done immediately before putting the sample into the UHV evaporation chamber and yielded transparent FM/NM interfaces in the final devices.
11) Metal deposition	Thermal evaporation of 40 nm Cu in a UHV chamber. Conditions: P_0 ~5 x 10^{-9} mbar (base pressure), r ~ 2 Å/s (deposition rate), P ~3.5 x 10^{-8} mbar (evaporation pressure). .
12) Lift off	Repeat step 6

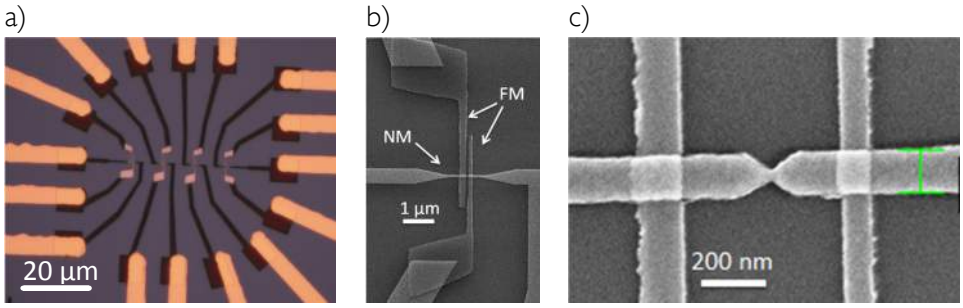

Figure 6.5. Lateral spin valves obtained by EBL a) Optical microscopy image of 4 devices contained in the same chip, where 3 lithography layers can be observed (each has a different colour). b) SEM image of a device with two permalloy electrodes (FM) bridged by a NM copper channel with a pre-defined nanoconstriction. c) Detail of constriction patterned in a copper channel between the two FM electrodes of a LSV.

6.2.2 Electromigration

We further modified the fabricated devices by feedback-controlled electromigration, which basically consisted on applying increasing voltage ramps across the copper channel in a two-probe configuration (Figure 6.6-a). The phenomenological description of electromigration and the experimental details of the process were reported in previous chapters (Chapter 4).

In the following set of experiments, we made use of electromigration for narrowing a lithographically pre-defined nanoconstriction in the NM channel of each LSV. We carried out the process gradually, applying series of increasing voltage ramps. In general, the resistance of the copper channel increased very slowly, as the cross section decreased during the electromigration process, allowing to stop after inducing very small resistance changes (for instance, ΔR ~1Ω). We stopped the electromigration process periodically for characterisation, usually, when the resistance of the copper channel changed by a given amount (typically around 1 Ω) (see Figure 6.6-c). On occasions, especially at the point in which a constriction became unstable, sudden rearrangements of metallic grains led to a reconstruction of the nanoconstrictions (observed as a sudden decrease in the measured resistance). The electromigration process was carried out until the spin signal decreased below our detection limit and it was further continued until the constrictions were converted into nanogaps, still stopping periodically for characterisation (Figure 6.6-c).

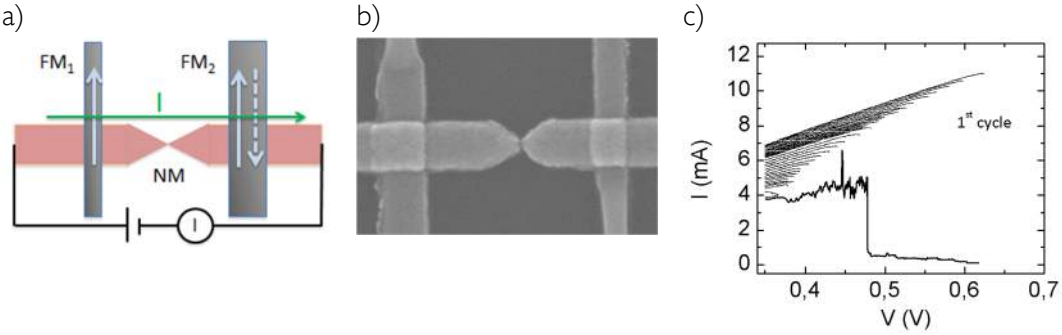

Figure 6.6. Electromigration of the nanoconstrictions in LSVs. a) Schematic view of a two-probe configuration used for electromigration of the nanoconstrictions in the NM copper channel. b) SEM image of a LSV in which the constriction has been narrowed and finally broken to form a nanogap. c) I(V) curves recorded during the electromigration process of the copper channel

6.3 Characterisation

Electromigration processes and characterisation were performed in alternate steps, modifying the LSV by short electromigration cycles and measuring the spin signal immediately afterwards.

All the studied devices were inspected by scanning electron microscopy in order to measure the dimensions of the NM channel and FM electrodes after the experiments where completed. On one hand, the LSVs were electrically characterised by measuring the non-local resistance (R_{NL}) as a function of the applied magnetic field (H) and the electrical resistance of the NM channel at a four-probe configuration (R_{4P}). On the other hand, the charge current (I) as a function of the applied voltage (V) of the NM channel and its low

bias electrical resistance were measured at two-probe configuration (R_{2P}) before and after each electromigration cycle. We aimed at detecting any possible variation in the charge transport through the constricted NM channel in order to correlate it with the evolution of R_{NL} or the measured spin signal (ΔR_{NL}). The configurations utilised for the mentioned measurements are shown in Figure 6.7.

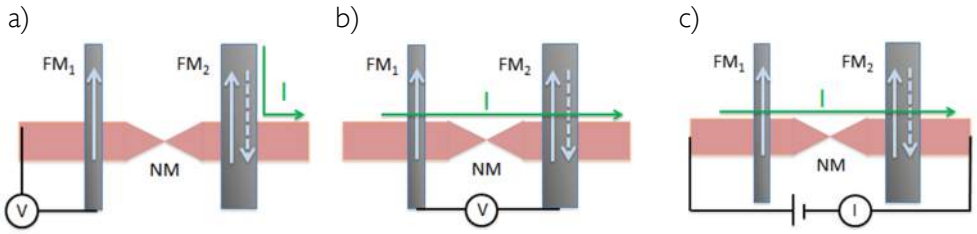

Figure 6.7. Configurations for the electromigration and characterisation of LSVs. a) The measurement of the non-local resistance utilising four probes was carried out as shown in the scheme. b) Measurement of the electrical resistance of the NM channel at a four-probe configuration. c) The electromigration and charge transport characterisation of the NM channel were done at a two probe configuration, as shown in the sketch. The arrows in all 3 panels represent the magnetization of FM electrodes, which can be parallel or antiparallel to each other, depending on the applied magnetic field.

The measurements were performed inside a liquid He cryostat at T=10 K, since the spin relaxation time scales with the electrical conductivity [16] and therefore, it was convenient measuring at low temperatures in order to obtain intense signals. On the other hand, performing electromigration at low temperatures allowed having a better control of the process due to a lower thermal activation. Setting a four probe configuration for the measurements allowed injecting the current (I ~ 100 μA) with two electrodes and measuring the non-local voltage with the other two, as shown in Figure 6.7 a. We employed the DC reversal or "delta mode" technique in the measurements, in order to eliminate the thermal noise (for more details see Chapter 2).

Regarding the spin signal measured in the as-fabricated LSVs before electromigration, we noticed that R_{4P}, as well as the spin signal, were slightly higher in devices with a patterned constriction (Figure 6.8). Apart from that, they did not show any other remarkable characteristic when compared to the LSVs without constrictions.

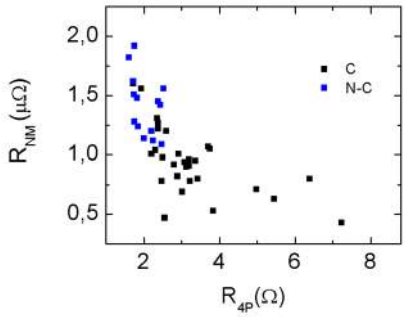

Figure 6.8. Spin signal measured in as fabricated LSVs. We observe that the resistance of the LSVs with patterned nanoconstrictions in the copper channel had in general a higher resistance and a lower spin signal before electromigration, when compared to the LSVs without constrictions. Note that C and N-C in the legend stand for constricted and non-constricted.

The spin signal in the LSVs with constrictions (ranging from 0.4 to 1.6 m Ω) and the electrical resistance of the copper channel measured before electromigration (approximately from 2 to 6 Ω) changed from device to device. We attributed this dispersion to small variations in the fabricated constrictions and also to differences in the resistivity (ρ) of the copper channel. The resistivity of a metal has a temperature independent term (residual resistivity) that is related to scattering events with defects. As it was demonstrated in previous experiments in our group, in the case of copper nanowires without constrictions this term is mostly dominated by grain-boundary scattering [35]. In the cited work, it was assumed that the average grain size was given by the smallest dimension of the nanowires, which in that case corresponded to the thickness. The values obtained for the spin diffusion length of copper by fitting the measured spin signal to equation 6.1 were higher for thicker copper nanowires, ($\boldsymbol{\lambda}_{Cu}$ ~1 μm for 145 nm thickness and $\boldsymbol{\lambda}_{Cu}$ ~500 nm for 40 nm thickness), since $\boldsymbol{\lambda}_{Cu}$ scales with $1/\rho$ [35]. Hence, in the case of copper nanowires with patterned constrictions of similar or smaller dimensions than the nanowire thickness (40 nm), we expected to have values of $\boldsymbol{\lambda}_{Cu}$ < 500 nm. Similarly, we also expected to have a lower spin signal in devices with smaller constrictions.

We obtained around 100 devices by EBL that were suitable for the proposed experiments (in other words, they had constrictions that were robust enough for standing at least one measurement of the spin signal before being eletromigrated). In general, the spin signal decreased dramatically after electromigration, often disappearing completely after the channel resistance had changed very little (ΔR ~1Ω). This decrease of the signal happened gradually in a few devices (Figure 6.9). Just a 2% of devices conserved the spin signal for more than 6 electromigration cycles and around a 10% lasted more than 2 cycles. We note that these numbers are only illustrative, since it was not easy to extract statistics from the performed experiments. In fact, each electromigration cycle could have a different effect (meaning that it could induce a different amount of change in the constriction), as a

consequence of the inherently random nature of the process, even when applied to the same device and in the same experimental conditions. Therefore, we note the difficulty to support or contradict our hypothesis and conclusions based on the obtained statistics.

In all the studied cases, the spin signal was lost when the conduction through the copper wire was still ohmic. The constrictions were then further electromigrated and the spin signal was measured repeatedly, although we did not detect any spin current through the constriction. SEM imaging of the devices after the finishing the experiments showed the creation of nanogaps in the pre-patterned constrictions (Figure 6.6 b).

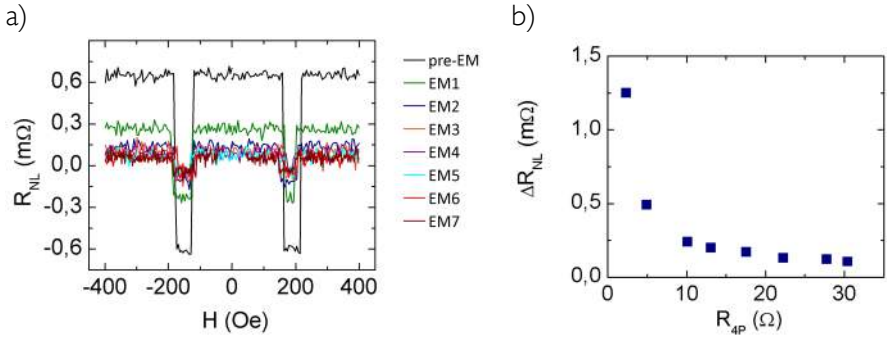

Figure 6.9. Evolution of the spin signal in a LSV along several electromigration cycles. a)The spin signal decreased after each electromigration cycle. b) Dependence of the spin signal with the electrical resistance of the copper channel (R_{4P}), corresponding to the measurements in panel a.

After comparing the results in several devices, we observed that they all showed a dramatic decay of the spin signal as R_{4P} increased (Figure 6.9 b and Figure 6.10). In principle, this seemed reasonable based in equation 6.1 (Section 6.1.1), since an increase in the spin resistance of the NM channel (R_N, where $R_N = R_{4P}\,\lambda/L$) would led to a less efficient spin injection. However, we suspected that R_{4P} might change as a consequence of variations in not only the cross section, but also the resistivity of the copper channel induced by electromigration, which would complicate the analysis of results. A decrease of the constriction cross section might lead to an increase of grain boundary scattering and a larger resistivity, as we discussed earlier in this section, based on references [35]. This change in the resistivity would at the same time decrease the spin diffusion length (since $\lambda \propto 1/\rho$) and therefore, the spin signal itself.

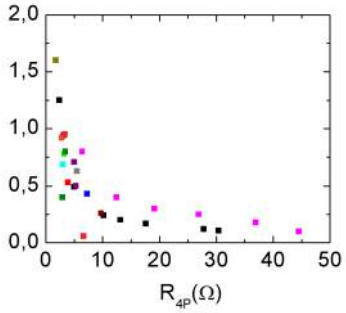

Figure 6.10. Dependence of the spin signal with electrical resistance. Magnitude of spin signal as a function of the electrical resistance (R_{4P}) of the copper channel measured in several devices at different electromigration stages. Each device is represented with a different colour, showing the evolution along different electromigration processes, in which the resistance increases.

Hence, we calculated the resistivity after each electromigration cycle by estimating the dimensions of the copper channel and applying the formula $R_{4P} = \rho L/A$ (where ρ is the resistivity, L and A are the length and cross section of the NM channel). The length of the copper channel was extracted from SEM imaging after the experiments. The cross section of the constriction varied during the experiments, since we were gradually breaking the copper channel by electromigration. The cross section could be estimated by means of electrical measurements and knowing that $J = I/A$, where I and J are the current and current density measured through the copper channel, respectively. In this case, we extracted the critical current (I_C) from the first curve of each electromigration cycle (Figure 6.11 b) and we calculated A, assuming that J_C (the critical current density) was constant throughout the successive electromigration cycles (See Chapter 4 for more details). J_C was initially calculated by estimating the cross section of the constriction in 7 devices (based on SEM imaging and X-ray reflectivity measurements) and extracting their respective I_C values from electromigration data. The resistivity value obtained for each device would correspond to a copper rectangle with the same length as the respective NM channel and a cross section equivalent to the narrowest part of it.

Regarding the obtained data, we first observed that indeed, the resistivity of the channel changed with each electromigration cycle (Figure 6.11 a). Thus, we must be aware that the variation of the spin signal with electromigration could be the sum of (at least) two effects: the increase of the resistivity and the resistance of the copper channel. We suggest that the variation of resistivity may be related to modifications in the grain structure as a consequence of the material accumulation and depletion areas resulting from electromigration. The variation of resistance would be directly affected by the reduction of the cross section and at the same time, by the change in the resistivity, since $R_{4P} = \rho L/A$.

When studying the dependence of the spin signal with resistivity, we observed that the values measured for different samples followed a similar trend. From this graph we could deduce that the non-local signal scaled with the resistivity.

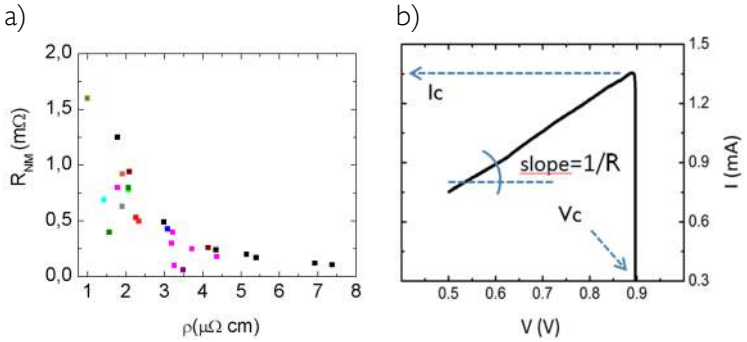

Figure 6.11. Dependence of the non-local resistance with resistivity. a) Dependence of the magnitude of the non-local resistance with respect to the electrical resistivity of the copper channel at different electromigration stages. Each device is represented with a different colour (using the same colour code as in Figure 6.10), Observing the evolution of a certain device along different electromigration processes shows that the resistivity of the copper channel increases. b) Example of a current (I) *versus* voltage (V) curve measured during electromigration, from which we extracted the critical current (Ic) in order to estimate the cross section of the constriction. This data were afterwards used for the calculation of the resistivity shown in panel a.

After further analysis, we suspected that electromigration did not just have an effect in the resistivity and the electrical resistance of the channel, but probably also in the quality of the FM/NM interface. We observed several devices in which the spin signal was lost after a short electromigration process, even if the resistance of the copper channel (and therefore, also the resistivity) remained unchanged. Additionally, we noticed that in the cases that further electromigration of the constrictions led to a drop in the measured resistance (probably due to grain rearrangements, as mentioned in Section 6.2.2), the spin signal did not necessarily return back to its previous state. In fact, the signal usually dropped to unmeasurable values after such sudden changes, showing that the effect of electromigration in the spin signal was not reversible. We hypothesised that this could be due to changes in the grain structure of the copper channel as a consequence of the material flow, even if the resistance returned to the initially measured values.

A possible explanation for this might be found in the modifications of the FM/NM interface, the quality of which affects exceedingly the spin injection efficiency [18, 33]. After SEM imaging of electromigrated devices, we observed that the migration of metal atoms did not occur exclusively in the constricted area. In fact, although the central part of the channel was possibly more susceptible to electromigration, we also noticed the appearance of morphological changes (mostly observed as a material accumulation spot) in areas at roughly 100 nm distance from the constriction. Therefore, there might be a material flow in

the channel areas situated below each FM/NM interface. Unfortunately, our conclusions on this point are quite speculative, since we do not have other means for quantifying the changes in the grain structure (or material flow) induced after each electromigration cycle.

6.4 Further work

This section is devoted to the proposal of further experiments targeted to achieve or, at least, to attempt approaching the objectives initially intended for this project.

The project itself was motivated by the research reported in literature regarding TMR in nanostructured devices and magnetoresistance in quantised conductance regimes, which are exclusively based on spin polarised currents. We intended to contribute with similar experiments but based on pure spin currents. We had in mind the following objectives:

- Studying the evolution of pure spin currents while the NM channel enters the ballistic transport regime.

We intended to carry out this objective by narrowing the cross section of the nanoconstrictions in the LSVs. So far, we have been able to observe the evolution of the spin signal when the constriction gets narrower, although the signal was lost before reaching a non ohmic behaviour. We proposed measuring the magnetoresistance in a local configuration in order to increase the intensity of the measured signal (see Figure 6.12). We expect that this would in allow going a bit further in the electromigration of the copper channel, ideally until a quantisation of the conductance is reached, and still measuring a magnetoresistance. We must note that the measured magnetoresistance would involve spin polarised currents and not pure spin currents, as it was initially intended. However, these experiments might help determining the moment at which the effects of spin polarisation is lost in our system and thus, asses the possibility of success in measuring pure spin currents in the nanostructured devices.

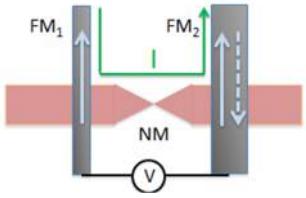

Figure 6.12. Proposed experiments. a) Schematic representation of the configuration for local magnetoresistance measurement in a LSV. The arrows represent the magnetization of FM electrodes, which can be parallel or antiparallel to each other, depending on the applied magnetic field.

- Observing the tunnelling of a pure spin current through a nanogap created by electromigration.

The local magnetoresistance measurements proposed in the previous point would also be valid for pursuing this objective. It might thus be possible to perform magnetotransport measurements when entering the tunnelling transport regime (after the constriction had been transformed into a nanogap). Depending on the obtained results we should be closer to knowing if a pure spin current could be transported by tunnelling, once there is no net charge flow associated to it.

- Measuring the spin signal in a system in the single electron transport regime.

We observed in previous electromigration experiments (see Chapter 4 and 5) that it is possible to create single electron transistors (SETs) by electromigration. We aimed at reaching this regime in the NM channel of our LSVs and studying the differences in the measured spin signal in the ON and OFF states of the formed SETs by simultaneously applying a gate potential at the silicon substrate. Similar studies have already been reported, although they are based on the measurement of the magnetoresistance with spin polarised currents [26].

In general, enhancing the spin signal measured in our devices would help pursuing the mentioned objectives. Another method proposed for this, apart from employing a local measurement configuration in the LSVs as suggested above, consists on using tunnel barriers in the FM/NM interfaces [36].

We attributed the observed decrease in the spin signal to a reduction in the diffusion of the spin current across the copper channel. We speculated that on decreasing the cross section of the constriction and therefore, increasing the spin resistance of the NM channel, the injected spins would be retained near the injector electrode, FM_1. This would lead to a spin accumulation in the NM channel section between the injector and the constriction. We anticipate that if the FM/NM interface resistance is in the transparent regime, as it is our case (see fabrication in Section 6.2.1), there is a higher probability for having a backflow of the spin current and subsequent spin relaxation inside FM1. This would indeed lead to a decrease of the non-local and local magnetoresistance in the devices, which agrees with the results observed our experiments. We proposed a complementary experiment that could help proving our hypothesis. It consists on placing the constriction outside the segment that connects the two FM electrodes (see Figure 6.13 b). We expected the spin signal to increase in this case, since the confinement effect induced by the constriction should enhance the spin accumulation in the copper channel between the two FM electrodes, leading to a more intense signal. An enhancement of roughly 100% has been demonstrated in LSVs with confined channels [37]. Our case would be similar, although with a gradually increasing confinement, as the constriction gets narrower by electromigration. Additionally,

monitoring the interface resistance in the devices after each electromigration cycle might shed some light on the obtained results.

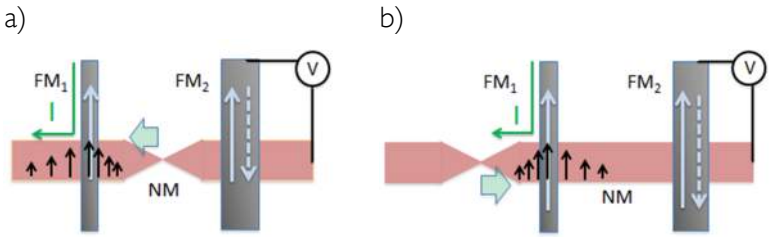

Figure 6.13. Proposed experiments. a) Sketch representing the decrease in the diffusion of the spin current across the constriction, due to an increased spin resistance. The spin accumulation gets confined and it does not diffuse so much as in the absence of a constriction. Thus, the probability for having a backflow and relaxation of the spin current into FM_1 increases. b) Representation of a non-local measurement in a LSV with a constriction outside the segment that connects the two FM electrodes. Decreasing the cross section of the constriction by electromigration is expected to lead to a confinement of the spin accumulation in the NM channel. This accumulation would result in an enhancement of the spin signal. Both in a) and b) panels the arrows represent the magnetization of FM electrodes, which can be parallel or antiparallel to each other, depending on the applied magnetic field.

Finally, we note that the equations that are usually employed for fitting the experimental data (see Section 6.1.1) and extracting the spin diffusion length and the spin polarisation might not be adequate for our experiments. These equations assume that the resistivity of the copper channel, as well as its spin resistance is uniform and constant, which is not our case.

6.5 Conclusions

We utilised EBL and electromigration in order to obtain metallic LSVs with nanoconstrictions, in which we intended to perform pure spin transport experiments while gradually decreasing the cross section of the constrictions.

Our main objective was studying how the transport of pure spin currents might be affected when reaching a conductance quantisation regime in the NM copper channel. We also proposed longer term objectives, aimed at studying pure spin transport in the tunneling regime (both in the case of direct tunneling through bare nanogaps and in systems involving quantum dots and showing Coulomb blockade characteristics.

So far, we obtained metallic LSVs with nanoconstrictions and we measured the spin signal and charge transport properties at different stages during the process or narrowing the constrictions. We observed a gradual decrease of the magnetoresistance when narrowing the nanowires by electromigration. We found that the spin signal was extremely

sensitive to electromigration, which we ascribe to (at least) three simultaneous effects, 1) the increase of the spin resistance of the NM channel, 2) the increase of the resistivity of the NM channel (which directly influences the spin diffusion length) and 3) variations in the FM/NM interface resistance. All three effects led to a dramatic decrease of the spin signal. We suggest that the responsible mechanism, especially as refers to the variation of resistivity and FM/NM interface resistance, was the change of the grain structure of the copper channel. This occurred as a consequence of the material flow (creation of voids and accumulation of metal) during electromigration.

All in all, we are aware that decoupling the different factors that affect the spin signal is not trivial. Being able to fabricate extremely small constrictions with EBL and comparing the results to electromigrated constrictions would be a starting point. In previous chapters (Chapter 3) we estimated that the narrowest constriction we can obtain with EBL is around 20 nm wide. Reducing the width by etching with focused ion beams (FIB) was discarded, due to the possibility of doping and introducing additional contamination of the NM channel that would complicate the analysis of results. Apart from the difficulty of obtaining these delicate nanostructures, it is extremely difficult to avoid their modification during electrical characterisation.

Finally, we must mention that electromigration experiments have an inherent random component that demands large statistics in order to achieve conclusive results. Unfortunately, we could not attain a sufficient number of successful experiments within the timeframe of this thesis. Therefore, we do not have the necessary statistics to strongly support our hypothesis and conclusions. However, we believe that we have achieved interesting results that could be further studied following the suggested experiments (see Section 6.4.

6.6 References

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List of publications

The work carried out in this thesis gave way to the following publications:

In situ electrical characterisation of palladium-based single electron transistors made by electromigration technique
L. Arzubiaga, F. Golmar, R. Llopis, F. Casanova and L. E. Hueso
AIP Advances 4, 117126 (2014)

Tailoring palladium nanocontacts by electromigration
L. Arzubiaga, F. Golmar, R. Llopis, F. Casanova and L. E. Hueso
Applied Physics Letters 102, 193103 (2013)

Visualizing the Near-Field Coupling and Interference of Bonding and Anti-bonding Modes in Dimer Nanoantennas
P.Alonso-González, P. Albella, F. Golmar, L. Arzubiaga, F. Casanova, L. E. Hueso, J. Aizpurua, and R. Hillenbrand
Optics Express 21, 1270 (2013)

Resolving the electromagnetic mechanism of surface-enhanced light scattering at single hot spots
P. Alonso-González, , P. Albella, M. Schnell, J. Chen, F. Huth, A. Garcia-Etxarri, F. Casanova, F. Golmar, L. Arzubiaga, L. E. Hueso, J. Aizpurua and R. Hillenbrand
Nature Communications 3, 684 (2012)

Propagation and nanofocusing of infrared surface plasmons on tapered transmission lines: Influence of the substrate,
P. Sarriugarte, M. Schnell, P. Alonso-González, L. Arzubiaga, F. Golmar, F. Casanova, L. E. Hueso and R. Hillenbrand
Optics Communications 285, 3378 (2012)

Nanofocusing of mid-infrared energy with tapered transmission lines,
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Real-*Space Mapping of Fano Interference in Plasmonic Metamolecules*
P. Alonso-González, M. Schnell, P. Sarriugarte, H. Sobhani, C. Wu, N. Arju, A. Khanikaev, F. Golmar, P. Albella, L. Arzubiaga, F. Casanova, L. E. Hueso, P. Nordlander, G. Shvets and R. Hillenbrand
Nanoletters 11, 3922 (2011)

In preparation:

Constricting the path of pure spin currents in Py/Cu lateral spin valves
M. Masourakis, L. Arzubiaga, R. Llopis, F. Casanova and L. E. Hueso.

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