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## Reliable determination of the Cu/n-Si Schottky barrier height by using in-device hot-electron spectroscopy

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We show the operation of a Cu/Al<sub>2</sub>O<sub>3</sub>/Cu/n-Si hot-electron transistor for the straightforward determination of a metal/semiconductor energy barrier height even at temperatures below carrier-freeze out in the semiconductor. The hot-electron spectroscopy measurements return a fairly temperature independent value for the Cu/n-Si barrier of  $0.66 \pm 0.04$  eV at temperatures below 180 K, in substantial accordance with mainstream methods based on complex fittings of either current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements. The Cu/n-Si hot-electron transistors exhibit an OFF current of  $\sim 2 \times 10^{-13}$  A, an ON/OFF ratio of  $\sim 10^5$ , and an equivalent subthreshold swing of  $\sim 96$  mV/dec at low temperatures, which are suitable values for potential high frequency devices.

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The Schottky energy barrier naturally appearing at a metal/semiconductor (MS) interface is a critical parameter for the performance of many modern electronic devices, from mainstream metal-oxide-semiconductor field effect transistors (MOSFETs) to novel organic-based light-emitting diodes or photovoltaics.<sup>1–5</sup> Hot electron in-device spectroscopy is a powerful technique for determining such energy barrier between a metal and a semiconductor.<sup>6–9</sup> This technique is based on the hot-electron transistor (HET), a classical metal-A/insulator/metal-B/semiconductor (MIMS) device in which a hot electron current coming from a metal-A emitter crosses ballistically a metal-B base before entering into the semiconductor conduction band. The HET is particularly interesting since hot electrons can be collected in the semiconductor without biasing the MS interface, and hence, they generate a collector current that can be used to probe the Schottky barrier without the effects of an external electric field at the interface. Moreover, the energy barrier height can be obtained directly from the experimental data with a simple theoretical model.<sup>10</sup> However, despite its power and simplicity, the hot-electron spectroscopy has been sparsely used for the study of metal/inorganic-semiconductor<sup>6,7,10–14</sup> and, more recently, metal/organic-semiconductor interfaces.<sup>8,9</sup>

In this manuscript, we explore the prototypical Cu/n-Si interface and extract its energy barrier by the hot-electron spectroscopy. Additionally, our HETs exhibit appealing electronic characteristics such as an OFF current of  $\sim 2 \times 10^{-13}$  A, an ON/OFF ratio of  $\sim 10^5$ , and an equivalent subthreshold swing of  $\sim 96$  mV/dec. The Cu/n-Si combination is particularly interesting since copper grows highly textured on Si<sup>14,15</sup> and has a high electrical conductivity and strong electromigration resistance—properties which make it a model system for the investigation compared to other polycrystalline interfaces.

Previously, the hot electron spectroscopy have been used for exploring the attenuation length of hot electrons in

Cu,<sup>16,17</sup> identifying the band structure of the underlying n-Si substrate<sup>14</sup> and the crystallographic orientation of n-Si,<sup>16</sup> detecting *chemicurrent*,<sup>18</sup> as well as for spintronic applications.<sup>14,19,20</sup> However, in our HET device, we capture useful information such as the reduction of thermal-leakage current with decreasing temperature<sup>21</sup> in addition to the reduction of quasi-elastic phonon scattering of hot electrons in the metal base and in the semiconductor collector.<sup>22</sup> Most importantly, we provide reliable determination of the Schottky barrier of Cu/n-Si interface at low temperatures even below carrier freeze-out temperature of Si, a regime that can be hardly accessed by other conventional electrical characterization methods. For putting this technique into the right perspective, we compare the results obtained by the hot-electron spectroscopy with those arising from standard current–voltage (*I-V*) and capacitance–voltage (*C-V*) measurements taken on the same device. Our work underlines the in-device hot-electron spectroscopy as a method of choice to map out the Schottky barrier physics below carrier freeze-out temperatures in a wide range of semiconducting materials.

Figure 1(a) shows the schematics of the Cu/Al<sub>2</sub>O<sub>3</sub>/Cu/n-Si HET device. The collector used is a n-type Si(100) substrate, having a resistivity of 5–10 Ω cm (donor concentration,  $N_D \approx 10^{15}$  cm<sup>-3</sup> at room temperature), with 300-nm-thick thermally grown SiO<sub>2</sub> on top. A  $1 \times 1$  mm<sup>2</sup> window was opened on the oxide layer by means of photolithography and buffered hydrofluoric acid etching. The etched area was then hydrogen terminated using 1% hydrofluoric acid, onto which a 20-nm-thick Cu base layer was deposited by e-beam evaporation in ultrahigh vacuum (UHV) through a shadow mask. For the hot-electron injection by quantum tunneling, a 3-nm-thick Al layer was then evaporated all over the device without breaking the vacuum and *in situ* plasma oxidized, followed by another 20-nm-thick Cu emitter layer deposition through a different shadow mask. Prior to the evaporation of the second Cu layer, and to avoid voltage breakdown up to an emitter voltage  $|V_E| \approx 1.4$  V of the thin tunnel barrier at the edges of 300-nm-thick SiO<sub>2</sub>, an additional 10-nm-thick

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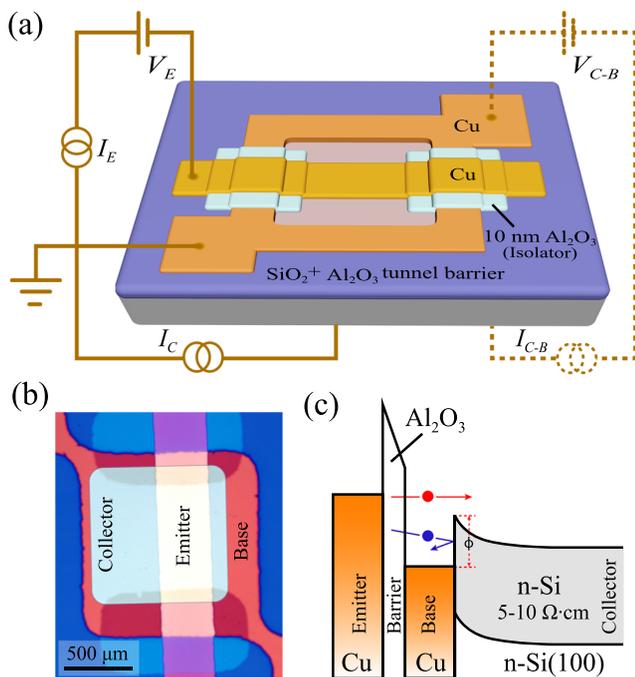


FIG. 1. (a) Schematic diagram of the hot-electron transistor. The dotted line represents the  $I$ - $V$  measurement setup to measure the base/collector diode. (b) Optical microscopy image of the real device. (c) Schematic energy diagram of the hot electron transistor, representing the negatively biased Cu emitter, the  $\text{Al}_2\text{O}_3$  tunnel barrier, and the grounded Cu base in direct contact with n-Si(100) collector. The base/collector junction is unbiased.

$\text{Al}_2\text{O}_3$  layer was evaporated in the area and surroundings of the Cu layers with the use of another shadow mask [see Fig. 1(a)]. Figure 1(b) pictures the top view of an actual device, with the emitter, base, and collector indicated. The active area for hot-electron injection and collection is considered to be confined to the overlapping area between the emitter and base electrodes ( $400 \times 800 \mu\text{m}^2$ ). Once fabricated, the device was then transferred into a variable-temperature probe station (Lakeshore) for electrical measurements with a Keithley-4200 semiconductor analyzer. Figure 1(c) represents the energy diagram of the HET device. The arrows represent the hot-electron transport above the Cu/n-Si barrier (red) and the electron reflection at the barrier interface below the barrier (blue), respectively. At a sufficiently high negative emitter bias ( $-V_E$ ), the electrons tunnel through the barrier and cross the metal base ballistically with enough energy to surpass the base/collector Schottky barrier and get collected into the semiconductor, providing the collector current. The onset of the output characteristic of the device accurately represents the height of the Schottky energy barrier in a first approximation. Those electrons that do not have enough energy to surpass the Cu/n-Si energy barrier are scattered/reflected at the base/collector interface and contribute to the base current directed to ground.

In order to investigate the collector current originated from the ballistic transport of hot electrons through the Cu-base, we measure the temperature dependence of the collector current ( $I_C$ ) versus emitter voltage ( $V_E$ ) from 300 K down to 10 K (see Figure 2). As noted above, the onset of the collector current represents an adequate measurement for the energy barrier at the Cu/n-Si interface. At 300 K, a slowly varying collector current of  $\sim 10^{-5}$  A is observed without

any well-defined onset above  $V_E = -0.3$  V, as it can be seen in Figure 2(a). The magnitude of this collector current decreases as temperature does, confirming that its origin is the regular thermal leakage current at the Cu/n-Si Schottky interface.<sup>21</sup> For temperatures below 180 K, the hot-electron current (ON) arises for  $V_E$  is higher than  $-0.5$  V, reaching values as high as  $\sim 10^{-8}$  A, while the OFF current (for  $V_E$  lower than  $-0.5$  V) is as low as  $\sim 2 \times 10^{-13}$  A. The OFF current measured is around two orders of magnitude lower than that reported in the recent literature,<sup>20</sup> and accordingly, our HET devices exhibit a large ON/OFF ratio of  $\sim 10^5$ . The equivalent subthreshold swing (defined as the required  $V_E$  for a ten-fold change in  $I_C$ ) is  $\sim 96$  mV/dec at  $\sim 80$  K and below, a very suitable value for applications in high-speed and frequency integrated-circuits.<sup>24,25</sup> Figure 2(b) shows in detail (in 5 K steps) the evolution of the hot electron current for temperatures below 190 K, while Figure 2(c) displays an exponential decrease with decreasing temperature for the thermal leakage down to  $160 \pm 20$  K. However, at temperatures below 160 K, the hot-electron current increases linearly for  $V_E$  voltages larger than the metal/semiconductor barrier height. Finally, for temperatures below  $\sim 20$  K, the hot electron current decreases due to the carrier freeze out in n-Si where the semiconductor becomes highly resistive (see Figure 2(c), inset).<sup>26</sup> Figure 2(d) represents the tunnel current vs emitter bias at several temperatures. Observation of a large amount of emitter current and also the linearity at high emitter bias suggests the possibilities of unavoidable current through the pinholes in the barrier that might be originated from the island growth of Al on top of Cu. However, the thin amorphous  $\text{Al}_2\text{O}_3$  barrier in our devices is good enough for the injection of energetic electron from the Cu-emitter into the Cu-base across the MIM structure. The emitter current slowly decreases with the decreasing temperatures, whereas the hot-electron current increases, possibly due to the reduction of quasi-elastic acoustic-phonon scattering in the base as well as in the collector at low temperatures.<sup>22</sup> As seen from this set of results, we describe the evolution of the collector current from 300 K to 10 K to interpret the origin of hot electron current and thermal-leakage current, while some previous experiments on hot electron transport across Cu/n-Si interface are reported at temperatures below 150 K.<sup>14,16,17,19,20,27</sup>

For the reliable determination of the Schottky barrier at the Cu/n-Si interface, we compare the values extracted from the hot-electron spectroscopy at several temperatures with the ones inferred from  $I$ - $V$  and  $C$ - $V$  methods of the same base/collector junction (see Figure 3). In the hot-electron spectroscopy, the barrier height is extracted as the intercept with the voltage axis for zero collector current. Due to the parabolic conduction band minimum in n-Si, the theoretical dependence (Bell and Kaiser model) of  $I_C$  with  $V_E$ <sup>10</sup> is  $I_C \propto I_E (V_E - \phi)^2$ , where  $\phi$  is the barrier height of the metal base/semiconductor collector interface. Figure 3(a) shows the hot-electron spectroscopy data, where  $(I_C/I_E)^{1/2}$  is plotted with respect to  $V_E$  and fitted linearly to the experimental curve. According to Schottky-Mott relationship, the value of  $\phi$  is typically the difference between the base-metal work function and the conduction band edge of n-Si(100) collector in the ideal case. However, in general, the energy-level

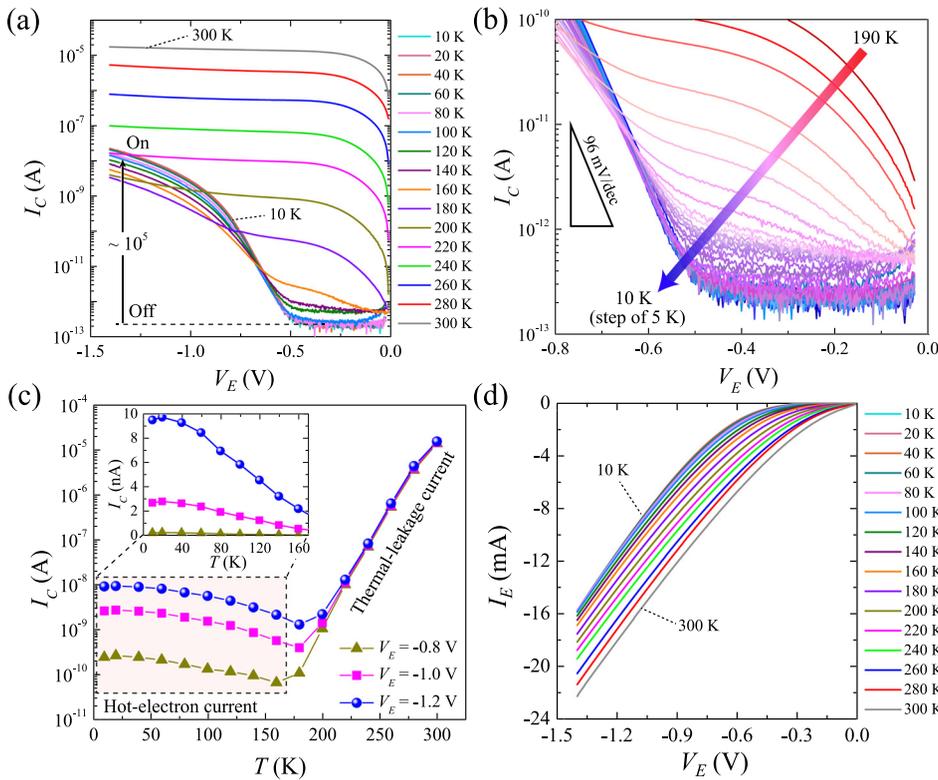


FIG. 2. (a) Plots of the collector current ( $I_C$ ) versus emitter bias ( $V_E$ ) at different temperatures for grounded base and at zero collector bias. (b)  $I_C$ - $V_E$  plots at different temperatures with 5 K step. (c)  $I_C$ - $T$  plots at different  $V_E$ , which describe the reduction of thermal leakage current and collection of hot-electron current. Inset shows the collector current only due to hot-electrons. (d) Plots of the emitter current ( $I_E$ ) versus emitter bias ( $V_E$ ) at different temperatures.

alignment is influenced by additional effects such as Fermi-level pinning, so that the rigid-band approximation is no longer suitable for capturing the actual barrier height.<sup>1,2,23</sup> Figure 3(d) displays experimentally extracted barrier heights by hot-electron spectroscopy and we can observe that its value below 180 K is constant around  $\sim 0.66 \pm 0.04$  eV.

We can now compare the hot-electron spectroscopy data with other mainstream techniques for obtaining the energy barrier height. In the first place, we show two-probe  $I$ - $V$  measurements of the base/collector (metal/semiconductor) junction [see Figure 1(a) for the setup and Figure 3(b) for the results]. The data show clearly the rectifying characteristics

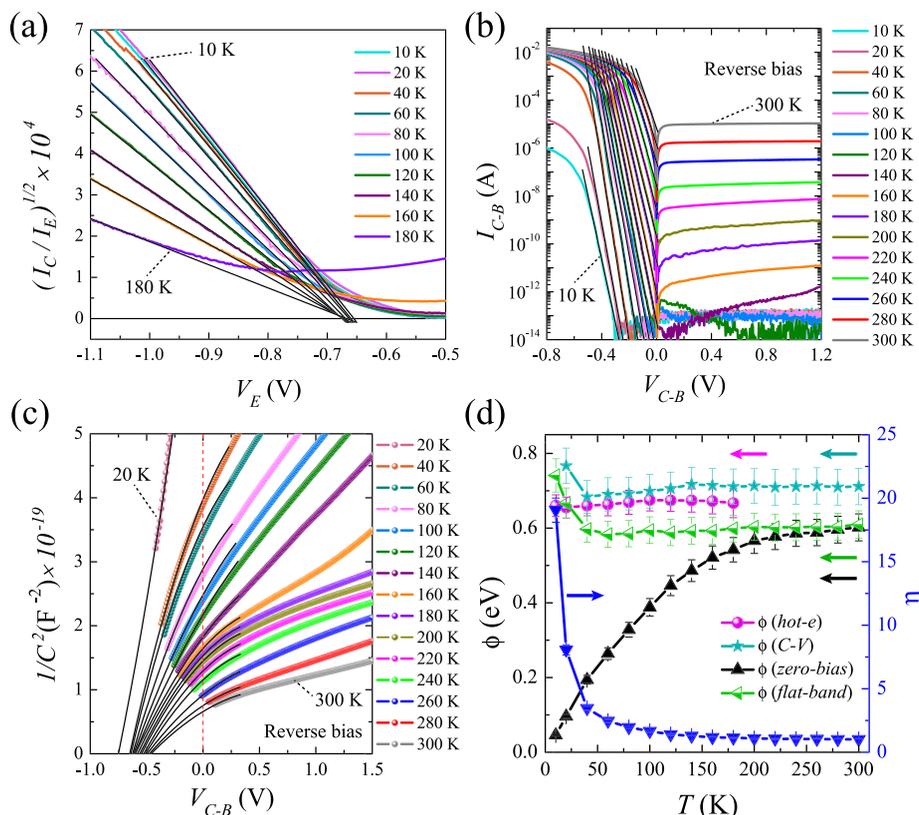


FIG. 3. (a) Hot-electron current plotted as  $(I_C/I_E)^{1/2}$  versus  $V_E$  superimposed to the linear fit (solid line) at several temperatures. Linear fits are used to extract the barrier heights. (b) Temperature dependent base-collector  $I$ - $V$  diode characteristics in semi-logarithmic scale. (c) Base-collector  $C^{-2}$ - $V$  characteristics of the diode at a frequency of 1 MHz and in the temperature range from 300 K to 20 K. Solid lines represent the extrapolation of the curvature of the experimental data. (d) Temperature dependence of the barrier heights extracted by different experimental methods, i.e., hot-electron, C-V, and I-V (zero-bias and flat-band); measurements are plotted in the left vertical axis. Right vertical axis represents the change in ideality factor of the diode.

of a MS diode. The rectification factor reaches several orders of magnitude and it increases with decreasing temperature due to the sharp decrease of the reverse-bias saturation current ( $I_{sat}$ ). However, below 40 K, the forward saturation current starts to decrease due to the fact that the Si-collector becomes resistive because of carrier freeze-out in Si. The amplitude and temperature dependence of the reverse saturation current varies in a similar way as the hot-electron leakage current, which confirms that the reverse saturation current of the base/collector diode contributes to the leakage current. Using the linear part of the forward bias regime, we extract the barrier height after a fitting with the thermionic emission (TE) equation<sup>1,2</sup> according to which  $I_{C-B} = I_{sat} \left[ \exp\left(\frac{qV_{C-B}}{\eta k_B T}\right) \right]$  for  $V_{C-B} > 3k_B T/q$ , where  $k_B$  is the Boltzmann constant,  $T$  is the temperature, and  $\eta$  is the ideality factor. Furthermore,  $I_{sat} = AA^* T^2 \exp\left(-\frac{q\phi_{b0}}{k_B T}\right)$ , where  $A$  is the base/collector junction area and  $A^*$  is the effective Richardson constant ( $\sim 110 \text{ A cm}^{-2} \text{ K}^{-2}$  for n-Si).<sup>1</sup> In principle,  $\phi_{b0}$  is meant to be the same Cu/n-Si Schottky barrier as determined by the hot electron spectroscopy; however, due to the different measurement methods, we denote this as zero-bias barrier height<sup>1</sup> and plot the extracted barrier height in Figure 3(d) along with the ideality factor  $\eta$ , a quantity which should be close to 1 for a well-defined Schottky interface. The zero-bias barrier height obtained from the  $I_{C-B}-V_{C-B}$  measurement decreases monotonically from  $0.60 \pm 0.04 \text{ eV}$  at 300 K to  $0.046 \pm 0.003 \text{ eV}$  at 10 K, whereas the ideality factor sharply increases from  $1.02 \pm 0.04$  at 300 K to  $19.06 \pm 0.95$  at 10 K. These phenomena are commonly observed in Schottky diodes,<sup>28-30</sup> and can be explained by considering an inhomogeneous distribution of barrier heights at the MS interface<sup>31,32</sup> only in a temperature regime without the carrier freeze-out in the semiconductor. Here, such a strong disagreement between these two measurement methods suggests that the zero-bias barrier height decreases artificially at low temperatures below 60 K, where the diode becomes extremely non-ideal and the thermionic emission model fails to explain the experimental data. Furthermore, taking into account the zero-bias barrier height and the ideality factor, the  $\phi_{bf}$  (flat-band barrier height)<sup>33</sup> can be expressed as  $\phi_{bf} = \eta\phi_{b0} + (\eta - 1)(k_B T/q)[\ln(N_C/N_D)]$ . The extracted  $\phi_{bf}$  is plotted in Figure 3(d) representing the correction of the non-ideal  $\phi_{b0}$  to achieve a more realistic Schottky barrier height. In addition, it is also possible to obtain a Schottky barrier height from the Richardson plots using the reverse bias diode characteristics.<sup>2,4,34</sup> We find the Cu/n-Si Schottky barrier height to be  $0.52 \pm 0.02 \text{ eV}$ , fitting the  $I_{sat}$

current only in the high temperature regime (300K–200K). However, this method of extracting the Schottky barrier height underestimates the influence of the diode ideality factor.

In the second place, we show the capacitance (C)-voltage (V) measurements and how we can extract in this case again the metal/semiconductor energy barrier, which we will denote as  $\phi$  (C-V) [see Figure 3(c)]. The applied voltages in this particular case range from the reverse-bias condition to a small regime of forward-bias until the diode starts conduction, i.e., maximum up to  $-0.36 \text{ V}$ . In the simplest case of a linear relation between  $C^{-2}$  and  $V$ , we can write,<sup>2</sup>  $1/C^2 = (2/qN_D\epsilon_s A^2) \cdot [V_I + V_{C-B}]$ , where  $V_I = (\phi - k_B T/q - \xi)$  represents the linear intercept on the voltage axis and  $\epsilon_s$  is the permittivity of Si. In case of linear dependence, the barrier height can be extracted as  $\phi = V_I + k_B T/q + \xi$ , where  $\xi = (k_B T/q)[\ln(N_C/N_D)]$  is the energy difference between the Fermi level and the conduction band edge in Si. The effective density of states in the conduction band edge is given by  $N_C \approx 2.8 \times 10^{19} \text{ cm}^{-3}$ .<sup>1</sup> However, we notice a strong nonlinear dependence of the  $C^{-2}-V_{C-B}$  characteristics. In case of nonlinearity, the  $C^{-2}$  can be expressed as a quadratic function, i.e.,  $1/C^2 = M_1[V_I + V_{C-B}] + M_2[V_I + V_{C-B}]^2$ , where  $M_1$  and  $M_2$  are the fitting parameters.<sup>35</sup> Such a nonlinear dependence could be due to a contribution of the interface charge capacitance that goes in adverted by other experimental techniques. By using a quadratic dependence around a zero-bias voltage, we extract the intercept on the voltage axis, which is then used to determine the barrier, as shown in Figure 3(d). It is worth noting that, in our measurement, the  $C^{-2}-V_{C-B}$  characteristics strongly deviate at 20K, which could be possibly due to carrier freezing in n-Si at  $\sim 20 \text{ K}$  and below.

Figure 3(d) shows the different values of the barrier height extracted by the hot electron spectroscopy,  $I-V$  and  $C-V$  measurements, i.e.,  $\phi$  (hot-electron),  $\phi$  (zero-bias),  $\phi$  (flat-band), and  $\phi$  ( $C-V$ ), respectively. They all show a similar weak temperature dependence; however,  $\phi$  (flat-band) and  $\phi$  ( $C-V$ ) diverge at very low temperatures, while  $\phi$  (hot-electron) remains stable for all the temperatures obtained. Consequently, the hot-electron spectroscopy provides a reliable and straightforward method for the barrier height extraction in the absence of an applied electric field at the Cu/n-Si interface and at temperatures below the carrier freeze-out. Being an in-device method, as opposed to photo-emission spectroscopic techniques, it provides a realistic approach to the metal/semiconductor barrier height determination for its application in electronic device design. Finally, we summarize the measured Schottky barrier heights by different methods in Table I, where we find a relatively good

TABLE I. Measured Schottky barrier heights by different methods and its comparison with the literature.

T (K)	$\phi$ (hot-e)	$\phi$ (C-V)	$\phi_{b0}$ (I-V) (eV)	$\phi_{bf}$ (eV)	$\phi$ (hot-e) from Ref. 16	$\phi$ (hot-e) from Ref. 17	$\phi_{b0}$ (I-V) from Ref. 36
300	...	0.71 eV	0.60	0.61	...	...	0.59 eV
200	...	0.71 eV	0.56	0.60	...	...	0.61 eV
100	0.67 eV	0.70 eV	0.39	0.59	0.62 eV	...	0.63 eV
80	0.67 eV	0.69 eV	0.33	0.58	...	0.64 eV	...
40	0.66 eV	0.68 eV	0.19	0.60	...	...	...
10	0.66 eV	...	0.05	0.74	...	...	...

agreement with the existing literature<sup>16,17,36</sup> only in some certain temperatures.

In conclusion, we have demonstrated the operation of a Cu/n-Si-based hot-electron transistor and determined the height of its base/collector (metal/semiconductor) Schottky energy barrier. In this experiment, we are able to fully describe the collector current that originates from the hot-electron transport and to extract the Schottky barrier height over a wide temperature range. For completeness, we have compared the extracted barrier height with the other measurements methods such as the *I-V* and the *C-V* techniques, concluding that the hot-electron spectroscopy is the most reliable method to map out Schottky barrier heights at very low temperatures. In addition, our results highlight the in-device hot-electron spectroscopy as a straightforward method to determine the metal (base)/semiconductor (collector) energy barrier in real device operation conditions. Our optimized hot-electron transistor, with a current ON/OFF ratio of up to five orders of magnitude, low OFF state current, and an equivalent subthreshold swing of  $\sim 96$  mV/dec at low temperatures, could be suitable for high-frequency device applications in cryogenic environments.

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