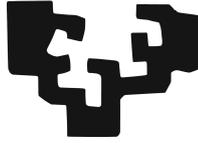


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Electronic and spintronic devices using two-dimensional materials

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PhD Thesis

2017



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Resumen

Durante las últimas décadas, la electrónica se ha intentado redefinir con nuevos conceptos de transporte de electrones. La búsqueda por un mayor rendimiento, menor consumo de energía, dispositivos de menores dimensiones y todo esto a menor costo, ha impulsado la industria de los semiconductores.

Desde que en 2004 la microexfoliación manual pusiera al alcance de la comunidad científica los materiales bidimensionales (2D) de van der Waals (vdW) atómicamente finos, su implementación en dispositivos con estructuras y conceptos nuevos ha prometido aplicaciones disruptivas, motivando la investigación en diversos campos. Confinados hasta el espesor mínimo posible, los electrones en estos materiales exhiben una plétora de propiedades electrónicas, desde el semiconductor MoS₂, hasta el superconductor NbSe₂, pasando por el dieléctrico BN, y el más versátil material, el grafeno (Gr).

En esta tesis se han explorado aspectos fundamentales y aplicados de grafeno obtenido por deposición química de vapor (CVD), MoS₂ y WSe₂. Se han utilizado como canal de transporte en dispositivos electrónicos, como en transistores de efecto de campo (FET), barras de Hall y diodos.

En los dos primeros capítulos iniciales motivamos la línea de investigación en electrónica y espintrónica basada en materiales de dos dimensiones, en concreto en grafeno y dicalcogenuros de metales de transición (TMDs), e introducimos brevemente los conceptos necesarios para comprender el transporte de electrones en uniones de metal/semiconductor, metal/aislante/semiconductor (MIS), metal/aislante/metal (MIM) así como efectos magnetoresistivos en materiales 2D y estrategias no locales de transporte de espín. En el capítulo 3 describimos las técnicas de caracterización y fabricación de los dispositivos estudiados en la tesis, con un fuerte enfoque en las técnicas de exfoliación y transferencia de los materiales 2D.

En la primera parte del capítulo 4, empezamos con los resultados experimentales de la tesis, y exploramos efectos magnetoresistivos en transistores de MoS₂. Éste es uno de los materiales bidimensionales de van der Waals más estudiados después del grafeno, con sus propiedades eléctricas muy bien caracterizadas. Es un semiconductor de tipo n que complementa uno de los aspectos más débiles de los transistores basados

en el grafeno, es decir, la pequeña diferencia entre la corriente máxima y la corriente mínima de los dispositivos. En el contexto de transporte de espín, las técnicas magnetoresistivas de localización débil emergen como una herramienta que, aunque no esté directamente relacionada con espintrónica, posibilita la determinación de las contribuciones relativas de los mecanismos de dispersión (*scattering*) de espines para el transporte difusivo de electrones. Esto provee una evidencia indirecta de las propiedades de transporte de espín del material. En nuestro trabajo identificamos una restricción de $8 \times 10^{12} \text{ cm}^{-2}$ en el dopaje electrónico para la realización de medidas de magnetotransporte estables, derivado de las fuertes fluctuaciones de corriente de los FET para niveles más bajos.

En el nivel de espesor mínimo, los electrones en los FET 2D vdW son particularmente vulnerables a las interacciones del medio ambiente. Los estados de trampa inducidos en la banda de energía del material semiconductor y las impurezas ionizadas provocan fluctuaciones en la corriente. Estas oscilaciones aparentemente aleatorias pueden descomponerse en un espectro de frecuencias usando procedimientos de transformada rápida de Fourier (FFT). Estudiar la dependencia de la densidad espectral de potencia (PSD) con la frecuencia puede proporcionar información adicional sobre mecanismos microscópicos que impulsan las oscilaciones.

Isso mismo lo hacemos entonces en la segunda parte del capítulo 4, donde estudiamos el ruido de baja frecuencia (LFN) de la corriente de dispositivos fabricados con diferentes espesores, y utilizando las interacciones luz-materia fuertes de MoS_2 para obtener técnicas de dopaje por fotones junto con el dopaje electrostático que permita dopar el canal. La convergencia de todas estas condiciones permite discernir el mecanismo detrás de los diferentes tipos de ruido LFN reportados en la literatura para MoS_2 , mientras que se identifica un crossover LFN impulsado por el dopaje por fotones. LFN en MoS_2 es el resultado de una compleja interacción entre las diversas fuentes de dopaje de electrones (el dopaje intrínseco del canal, el fotodopado y el dopaje electrostático), la fuerte disminución de las escalas de tiempo de recombinación con el número de capas decreciente, y la percolación desde una red discontinua de resistencia aleatoria hasta un mar de electrones continuo en el nivel de Fermi.

En el capítulo 5 exploramos transistores de WSe_2 , que dentro de la familia de los TMD semiconductores de vdW es otro material prometedor para aplicaciones

electrónicas y optoelectrónicas. La menor banda de energías y el dopaje tipo p hace que los transistores basados en WSe_2 sean una alternativa fuerte a la electrónica basada en MoS_2 . La menor banda de energía permite la realización de transistores ambipolares, donde tanto electrones como huecos son accesibles por medio de dopaje electroestático utilizando óxidos estándares como dieléctricos. Con una selección apropiada de los metales de contacto es posible producir transistores ambipolares. En nuestro trabajo con WSe_2 , optimizamos las propiedades de transporte de electrones considerando BN como un sustrato de interfaz superior e inferior y una capa de encapsulación, respectivamente. Al hacerlo, podemos abordar en cierta medida los fuertes efectos histéricos que afectan negativamente al funcionamiento de los FETs WSe_2 sobre sustratos de óxido. Mediante el uso de BN como sustrato, la movilidad de efecto de campo máxima de los huecos aumentó a $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, la movilidad de electrones a $14 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, y la relación ON/OFF a 10^8 .

La versatilidad del grafeno CVD nos permite realizar tanto estudios aplicados como fundamentales, tanto en espintrónica como en electrónica.

Las propiedades únicas del grafeno lo convierten en un material esencial en la búsqueda de modos completamente eléctricos para generar, transportar y detectar corrientes de espín sin el uso de elementos magnéticos. Utilizando una muestra en forma de barra Hall, se ha demostrado que las señales no locales en grafeno están asociadas con el transporte de espín.

En nuestro caso, en capítulo 6, utilizamos la gran disponibilidad de área de grafeno CVD para estudiar efectos no locales en un escenario improbable para el transporte de spines. Demostramos la persistencia de grandes señales no locales en dispositivos de grafeno CVD a escala milimétrica y micrométrica y que siguen de cerca la misma dependencia con la relación de aspecto del dispositivo para geometrías que difieren en dos órdenes de magnitud. Excluimos posibles fuentes de espín o transporte de valle debido a las escalas de longitud consideradas, y sugerimos que los mismos mecanismos presentes en los dispositivos de macroescala están impulsando la señal en las muestras de microescala. Teniendo en cuenta la fuerte asimetría de la magnetoresistencia no local y los detalles microscópicos de las muestras fabricadas, sugerimos que las grandes señales no locales son impulsadas por estados de borde contrapropagantes disipativos, mediados por los límites de los granos. Estos resultados

implican que se debe tener especial cuidado al atribuir señales no locales en dispositivos de estado sólido al transporte de corrientes de espín o de valle.

De una forma más aplicada, utilizamos grafeno de CVD para otros dos tipos de dispositivos.

En primer lugar (en el capítulo 7), estudiamos el uso de grafeno como material de electrodo para transistores de efecto de campo lateral y vertical que operan utilizando canales orgánicos (OFETs), y determinamos que la baja densidad de estados de grafeno permite que los campos eléctricos alcancen la capa orgánica y permitan la operación en modo de transistor para la geometría vertical. Como electrodo de contacto, ya se ha demostrado que el grafeno es un candidato adecuado para dispositivos semiconductores de alto rendimiento. Su gran disponibilidad en forma de grafeno monocapa de deposición química de vapor hace que sea un contendiente fuerte para superar los obstáculos que enfrentan los metales nobles. Se puede buscar grafeno monocapa para la función de electrodo de contacto en transistores orgánicos debido a tres propiedades: la función de trabajo sintonizable, la proyección electrostática débil y su estabilidad química. Mediante dopaje electrostático de grafeno, la función de trabajo puede ser modulada de 4.4 a 4.8 eV, en línea con la función de trabajo de muchos materiales metálicos. Debido a la baja densidad de estados de grafeno y ultra-delgadez (en contraste con los metales), el grafeno muestra proyección electrostática débil. Ésta permite que los campos eléctricos alcancen el semiconductor orgánico sobre el grafeno y modulen sus niveles de energía. En nuestro trabajo, proponemos una estrategia para reemplazar los electrodos de metal noble utilizados comúnmente en OFETs, integrando electrodos de grafeno CVD con polímeros procesados en solución tipo n para dispositivos laterales y verticales de alto rendimiento. Proponemos un diseño específico tanto para transistores laterales como verticales que nos permite monitorizar las propiedades eléctricas de los electrodos de grafeno en cada etapa de la fabricación, en particular la modulación del nivel de Fermi del grafeno y la proyección electrostática de la puerta.

El segundo estudio con grafeno CVD es la fabricación a gran escala de diodos (capítulo 8). Beneficiándose de la sección ultrafina del grafeno, y utilizando una geometría lateral, se demuestra la confiable fabricación de diodos laterales de

metal/aislante/grafeno. En paralelo con transistores de efecto de campo, los diodos son bloques de construcción fundamentales para circuitos electrónicos. La aplicabilidad de los diodos se basa en las características de salida no lineal y fuertemente asimétrica, que permite la rectificación de las excitaciones variables en el tiempo a las señales de corriente directa.

En este contexto, el grafeno ha surgido como un fuerte contendiente para las aplicaciones terahertz debido a su alta movilidad, dinámica ultrarrápida, capacitancia cuántica intrínsecamente baja cerca del punto Dirac y fuerte absorción interbanda en un amplio rango de frecuencias.

En nuestro trabajo demostramos la fabricación confiable a gran escala de diodos laterales de Ti/TiO₂ (5.7 nm)/Gr usando técnicas de fotolitografía de contacto y grafeno monocapa de deposición química de vapor. La construcción lateral de los dispositivos se beneficia de la capacitancia cuántica intrínsecamente baja del grafeno y, en última instancia, de la sección transversal delgada, al tiempo que se beneficia de la inyección y extracción completamente en plano de electrones a través de la capa de grafeno, que se sabe exhibir conductividades altamente anisotrópicas en función de la dirección de transporte. Basándonos en esta estrategia lateral, abordamos una de las fuertes limitaciones de los diodos MIM y MIS de materiales de vdW, que es la baja corriente de salida, mientras que exhiben fuertes valores de mérito (FOM) para aplicaciones de alta frecuencia. En nuestros dispositivos, determinamos una constante de tiempo que coloca nuestra arquitectura propuesta en una posición adecuada para la operación THz.

Abstract

Ever since in 2004 atomically-thin two-dimensional van der Waals materials became available to the scientific community, at the reach of manual microexfoliation techniques, their implementation in novel device structures and concepts promised disruptive new applications and motivated research in a vast range of fields.

Confined to the thinnest possible thickness, electrons in these materials exhibit a plethora of electronic properties, from semiconducting MoS₂, to superconductor NbSe₂, dielectric BN, and, jack-of-all-trades, graphene.

In this thesis, we explore fundamental and applied aspects of chemical vapor deposition (CVD) graphene, MoS₂, and WSe₂ using electronic device structures that use them as transporting channel, namely field-effect transistors (FETs), Hall bars, and diodes.

MoS₂ is a *n*-type semiconducting 2D vdW that complements one of the weak aspects of graphene-based transistors, which is the small ratio between the maximum current output and of the minimum current output of the transistors (ON/OFF ratio). Using MoS₂ we identify an electron doping constraint for performing stable magnetotransport measurements, and we investigate the origins of the strong current fluctuations of the FETs. We study the low-frequency noise (LFN) of the current output of devices made with different layer thicknesses, and use the strong light-matter interactions of MoS₂ to employ photodoping techniques together with the electrostatic gating to dope the channel. By converging all these conditions, we are able to discern a mechanism behind the different types of LFN noise reported in literature for MoS₂, while at the same time identifying a LFN crossover driven by photodoping from carrier-number fluctuations to Hooge-mobility fluctuations.

With *p*-type semiconducting WSe₂ we optimize the electron and hole transport properties of ambipolar FETs by considering BN as a top and bottom interface substrate and encapsulation layer, respectively. By doing so, we are able to address to some extent the strong hysteretic effects that adversely affect the operation of WSe₂ FETs on oxide substrates, and improve the overall device performance.

The versatility of CVD graphene allows us to do both applied and fundamental studies, both related to spintronics and electronics.

The unique properties of graphene make it a core material in the search of full-electrical approaches to generate, transport, and detect spin currents without the use of magnetic elements. Using a Hall bar shaped sample, non-local signals in graphene have been demonstrated to be associated with spin transport. In our case, we use the large area availability of CVD graphene to study non-local effects in an unlikely scenario for the transport of spins. We study the non-local signals of millimeter-sized Hall bars of CVD graphene, and by doing a systematic study as a function of device scale, from macro-to-microscale we identify a mechanism that cannot be connected with spin diffusion that also leads to large signals. By evaluating the microscopic details of the samples, and the different effects observed, we propose the counterpropagating edge states shunted by grain boundaries to drive such effects.

In a more applied manner, we use CVD graphene for two other types of devices. First, we study the use of graphene as an electrode material for lateral and vertical field-effect transistors that operate using organic channels, and determine that the low density of states of graphene allows for unscreened electric fields to reach the organic layer and enable the transistor operation in the vertical geometry.

The second applied study is the large-scale fabrication of diodes using CVD graphene. Benefiting from the ultra-thin cross-section of graphene, and using a lateral geometry, we demonstrate the reliable fabrication of lateral metal/insulator/graphene diodes using Ti and TiO₂ as metal and insulating layers, respectively. The time constants determined from the direct-current analysis place the operation of the fabricated devices in the THz range. Additionally, the material combination considered enabled large current densities based on field emission processes.

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Chapter 1

Introduction

For the last decades, electronics has been trying to redefine itself, exploring the various degrees of freedom of electrons other than the electrical charge [1]–[4]. The quest for higher-performance, lower-power consumption, lower foot-print devices, all at lower costs, has been driving the semiconductor industry [5]. Silicon (Si) has been the material of excellence for electronics due to its versatility in core device building blocks such as *p-n* junctions, metal/semiconductor contacts and metal/insulator/semiconductor capacitors [6]. The well-established fabrication processes, together with some unique features, as the thermal growth of SiO₂ and large conductivity range achieved via ion implantation and re-crystallization, makes Si widely convenient for semiconductor-based electronics. Complementary metal-oxide-semiconductor (CMOS) technologies remain, for all practical purposes, the strongest contender for electronic applications.

The driving concept with CMOS technologies has been integrating more devices with smaller foot-print to enable additional computational power and new applications. Achieving this integration density requires the use of expensive fabrication techniques to deposit homogenous high purity thin films on large scale, to print millions of nanometer sized features using lithographic techniques in ultraclean environments, requiring process-flows with dozens of steps where reliability, repeatability, and reproducibility are all main concerns. The miniaturization trend leads to technological problems, namely in transistors, where there is the need to reduce short-channel effects, decrease leakage currents, increase ON/OFF ratios, lower subthreshold swings, and use performance boosters as high mobility channels and high-*k* dielectrics. All of these are connected to the figures of merit (FOMs) used to assess the performance of transistors. In the pursuit of overcoming these and other technological issues, several fields emerged with solutions based on new materials and architectures exploring charge transport and non-trivial properties of the electrons, namely the spin degree of freedom,

also referred to as spintronics [2], [4], [7]–[10]. In the last decade, two-dimensional (2D) van der Waals (vdW) materials emerged as a strong platform for exploring these alternative routes.

1.1 Two-dimensional materials in the context of electronics

The first question that arises when dealing with 2D systems is under which context something becomes 2D. The layman understanding of dimensionality sees 2D materials as a system where a third dimension is much smaller than its two other dimensions. In the context of electron transport, this concept must be further refined with additional considerations.

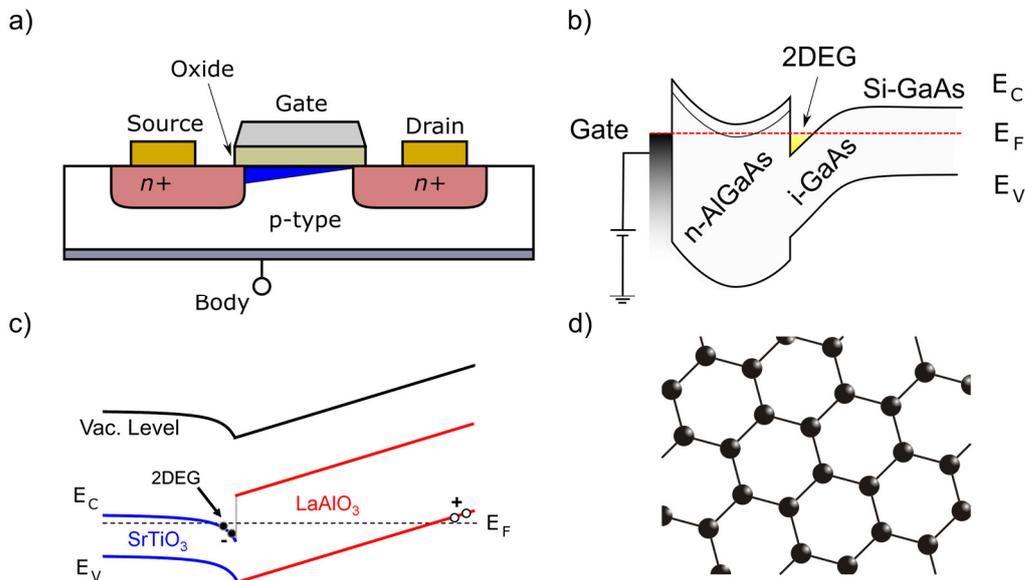


Figure 1.1 a) Two-dimensional electron gas (2DEG) generated by electrostatic confinement of mobile electrons in a field-effect transistor. b) Type I heterojunction between electron doped AlGaAs and intrinsic GaAs, resulting in a 2DEG at the interface. c) 2DEG formed between STO/LAO due to polarity discontinuity. d) One atom-thick layer of carbon atoms in an hexagonal lattice (graphene).

An electronic system becomes 2D whenever the reduction of the third dimension affects the translational symmetry, changing the energy vs crystal momentum dispersion of the electrons, or whenever the system's third dimension has magnitude equivalent or lower to the mean free path of electrons in that material. In this regard, there are two demonstrated classes of 2D systems: one that uses dissimilar materials to confine a 2D electron system at their interface, and one other where the 2D

system is realized by physically constraining a material to a few atomic layers. Figure 1.1 shows different approaches that can be undertaken to generate a 2D system.

The most common 2D system used in electronics is the two-dimensional electron or hole gas (2DEGs or 2DHGs, respectively). They can be found in metal-oxide-semiconductor field-effect transistors (MOSFETs) [6]. By means of a voltage applied to the oxide dielectric one can generate a layer of mobile unbound charge carriers limited to the interface between the semiconductor and the dielectric. Applying an electric field transverse to the generated 2DEG/2DHG allows for the flow of the accumulated mobile charge carriers (Figure 1.1 a)). Other ways of developing 2DEGs involves heterostructures of semiconductors where the Fermi level of the *n*-type semiconductor is lower than the carrier affinity of the *p*-type semiconductor. In such junctions, the band bending due to the uncompensated ionized dopants allows for the formation of a 2DEG at the interface, as is the case of a heterojunction of electron doped AlGaAs and intrinsic GaAs (Figure 1.1 b)). 2DEGs based on ultra-pure semiconductor heterojunctions have been demonstrated to possess electron mobility as high as $3 \times 10^7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [11]. Besides the two already refereed mechanisms to generate 2DEGs, it has also been demonstrated to emerge at the interface between oxides [12], [13] (Figure 1.1 c)). These realizations of 2DEGs rely on CMOS fabrication techniques to bring together bulk-like materials. In a broad sense, CMOS technologies encompass a wide set of applications exploring electron transport in bulk semiconductor materials of the groups III-to-V of the periodic table. Yet, the thickness of the system is far from the ultimate single-atomic thinness limit. With channels hundreds-of-nanometer-thick, the percentage of surface atoms involved in the transport of electrons in such devices is well below 1%. Although thin-film technologies are steadily aiming at the deposition of nanometer-scale high-purity films, their fabrication is increasingly complex and the list of materials that can be explored limited. In 2004, it was demonstrated that the ultimate thinness of a single atomic layer was at the reach of simple micromechanical exfoliation technique (Figure 1.1 d)). By cleaving a piece of graphite with scotch tape, Andre Geim and Novosolev demonstrated the isolation of a micrometer-sized, thermodynamically, and chemically stable, graphene sheet on SiO_2 substrates [14]. This feat was made possible due to the weak vdW out-of-plane interactions of the graphene sheets that compose graphite. Although graphene had already been identified and

explored in previous works in the 1961's by the means of the reduction of graphene oxide (GO) [15], the re-discovery in 2004 brought two-dimensional van der Waals materials to the spotlight by providing a seemingly effortless and valuable technique to reach one-atom-thick layers of this specific class of materials. Immediately after this finding, other 2D vdW materials were isolated. Transition metal dichalcogenides (TMDs) were the first set of vdW materials being explored for beyond graphene applications.

1.1.1 Graphene

1.1.1.1 Electronic properties

Graphene is a one-atom-thick hexagonal lattice of sp^2 -hybridized carbon atoms with lattice constant $a = 2.46 \text{ \AA}$ and carbon-to-carbon distances $a \sim 1.42 \text{ \AA}$ [16]. Figure 1.2 summarizes the electronic properties of graphene emerging from their crystal structure. Figure 1.2 a) shows an artistic impression of a sheet of graphene, and Figure 1.2 b) shows the trigonal planar crystal structure, with each carbon atom sharing covalent sigma (σ) bonds with the three closest carbon atoms. The resulting hexagonal lattice can be subdivided in two interpenetrating triangular lattices A and B. Figure 1.2 c) shows the energy dispersion relation in graphene, with a conic linear dependence around the Fermi level, E_F , and the linear density of states (DOS). A tight-binding Hamiltonian that considers the nearest and next-nearest neighbors of this lattice leads to the prediction of a gapless band structure at the K and K' points of the Brillouin zone (BZ) with conic energy dispersion E , which close to the Fermi level can be approximated as $E_{\pm}(\mathbf{k}) \approx \pm v_F |\mathbf{k}|$, where k is the crystal momentum relative to the K and K' points, and v_F the Fermi-velocity of the electrons, approximately of $1 \times 10^6 \text{ m s}^{-1}$. Due to the linear energy dispersion, the calculation of the effective mass results in massless electrons. The term *massless Dirac Fermions* was coined since the predicted electron wave function at K and K' follows the 2D Dirac equation.

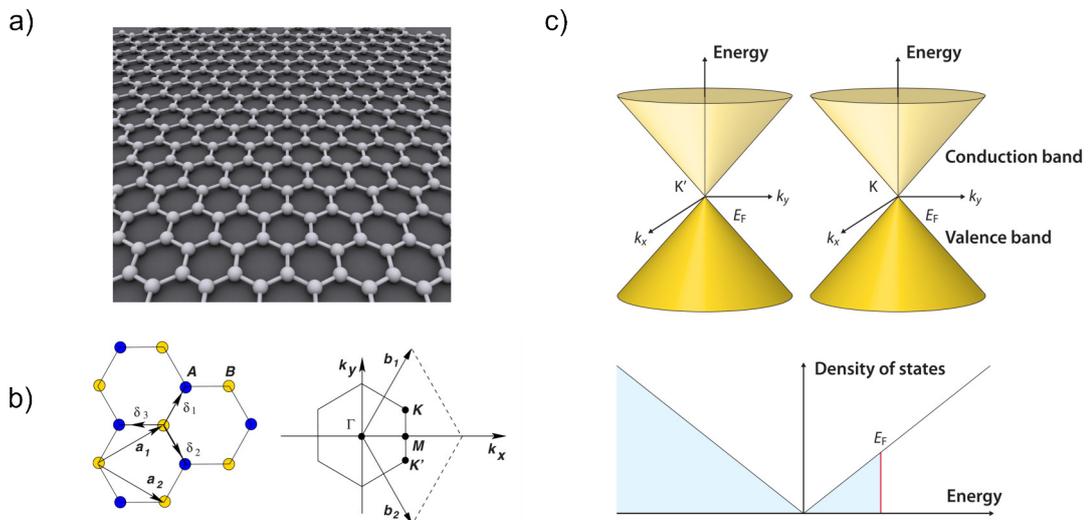


Figure 1.2 a) Artistic impression of a graphene sheet. b) Hexagonal lattice of graphene (left) and its Brillouin zone (right) composed of two interpenetrating triangular lattices A and B, with unit vectors a_1 and a_2 . δ_1 , δ_2 and δ_3 are nearest-neighbour vectors. c) Dirac cones near the K and K' points, with linear energy dispersion around the Fermi level, E_F (top). Density of states near the Fermi level (bottom). Figures adapted from a) Wikipedia, b) Ref. [16], c) Ref. [17].

The K and K' points of the BZ are also known as Dirac points. In short, electrons in graphene close to the Fermi level behave as charged photons, although with propagation velocities two orders of magnitude lower than the speed of light.

The demonstration of the operation of graphene for ambipolar field-effect transistors was first realized in 2004, with reported mobility using SiO_2 dielectric of $3 \times 10^3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [14]. Applying a magnetic field out-of-plane and measuring the magnetoresistance allowed for the observation of Shubnikov de Haas (SdH) oscillations, with the linear dependence of the SdH oscillation frequency with the induced carrier density confirming the 2D nature of charge carriers in graphene. SdH oscillations are usually regarded as a precursor for quantum Hall effect (QHE), the later also confirmed in Ref. [14], [18]. In graphene, the unusual feature of a pinned zeroth Landau level at the charge neutrality point leads to an anomalous case of integer QHE, referred to as half-integer QHE. Figure 1.3 shows the first experimental observations of the quantization of the cyclotron orbits in graphene under an external magnetic field with resulting half-integer QHE, demonstrating the two-dimensional nature of the electron gas structurally confined in the one atomic layer of carbon atoms.

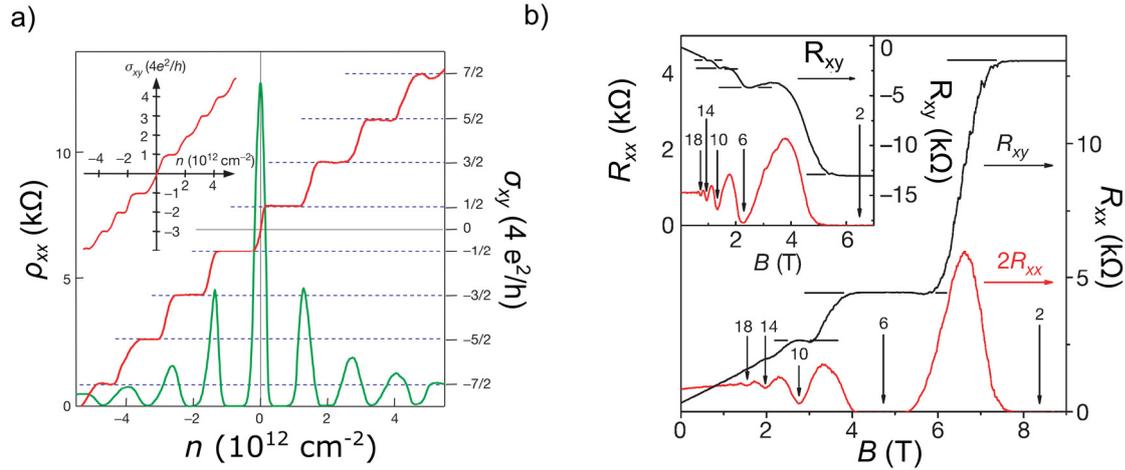


Figure 1.3 Half-integer Quantum Hall effect in graphene. a) Longitudinal resistivity and transversal conductivity as a function of the carrier density, with fixed external magnetic field. b) Longitudinal and transversal resistivity as a function of the magnetic field, measured at a carrier doping. Images adapted from Ref. [14] and [18].

Although electrons in graphene are expected to be ultra-relativistic, the determined effective mass via the cyclotron mass revealed it to be approximately $0.06 m_0$, with m_0 being the free-electron mass [14]. This result comes as consequence of the presence of defects and impurities in the graphene lattice.

1.1.1.2 Mobility engineering

Since the first demonstrations of graphene exhibited mobility well-below the predicted $10^6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [19], initial efforts focused on the optimization of the dielectric environment. Encapsulating with oxides as Al_2O_3 deposited via atomic layer deposition processes lead to the screening of ionized impurities at the surface of graphene, resulting in improved performances ($\sim 8 \times 10^3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) at room temperature [20]. By suspending graphene between two contacts, Bolotin *et. al.* showed that, even without the presence of a substrate, a purely 2D structure could retain its crystal order, and by freeing its surface from the effects of the oxide substrates typically used to exfoliate graphene one could reach mobility of the order of $1.7 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [21]. Probing high-purity graphene flakes with Landau level spectroscopy in the THz range at very low magnetic fields, Neugebauer *et. al.* demonstrated carrier mobility up to the $10^7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ mark [22].

In the search for other substrates that would get rid of the charge trapping and ionized impurities that had strong detrimental effects in graphene's electrical properties another 2D vdW material, boron nitride (BN), was found to be a perfect match [23]. With a trigonal planar structure, BN offered the ideal flat surface free of dangling bonds, where van der Waals forces between the graphene and BN surface would ensure an ultraclean interface. The stacking of 2D materials came then as an additional route towards improving the performance of the graphene devices. Graphene devices encapsulated in BN have been demonstrated to exhibit ballistic transport up to the 28 μm mark [24], and field-effect mobility of $5 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [25].

1.1.1.3 Large-area monolayer graphene

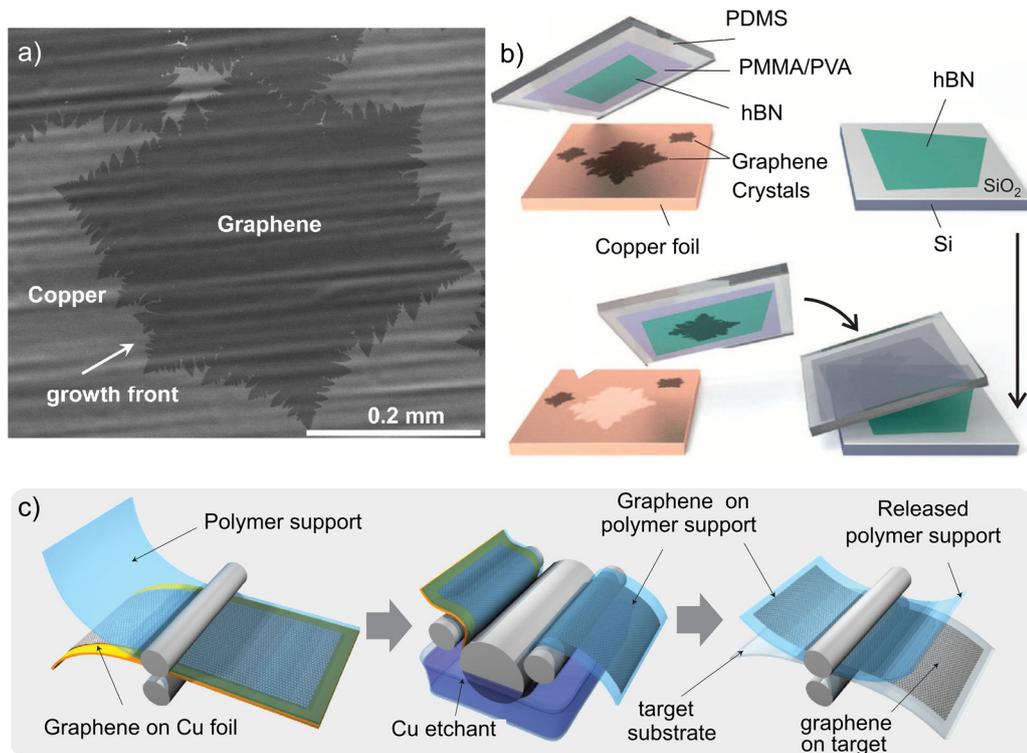


Figure 1.4 Large area production of monolayer CVD graphene. a) Self-limited growth of a graphene single crystal on copper substrates using a mixture of CH_4/H_2 at 1100 $^\circ\text{C}$. Taken from Ref. [26]. b) Ultra-clean dry transfer technique of CVD graphene via oxidation of copper foils and encapsulation with BN pick-up techniques. Adapted from Ref. [27]. c) Roll-to-roll production of CVD graphene. Adapted from Ref. [28]

Although the initial approaches to study electronic transport in graphene used micrometer scale exfoliated samples as a template for the experiments, soon after, the synthesis of large area polycrystalline monolayer graphene was demonstrated by chemical vapor deposition (CVD) and other surface precipitation methods [29]–[34].

Figure 1.4 shows different advances towards the large-scale fabrication and production of high-quality CVD graphene films, required for the introduction of graphene as an alternative to CMOS technologies. One downside of the CVD methods was the use of transition metals as a growth substrate, which lead to unavoidable contaminations from leftover residues during the wet etching processes. Together with the polycrystalline structure, CVD graphene electronic properties are hindered when compared to those of pristine exfoliate graphene, with typical mobility values for CVD samples on SiO₂ of $2\text{--}3 \times 10^3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [35]. Even so, all-dry transfer techniques using BN encapsulation and re-usable copper foils have been demonstrated to enable FET operation with mobility up to $3.5 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [27]. Benefiting from the possibility of fabricating large area devices, QHE has also been demonstrated at the millimeter scale [36], [37], surprisingly showing that edge transport in graphene survives even at the macroscale. The availability of CVD grown graphene opened doors to the large-scale fabrication of graphene devices based on photolithography technologies, while also including the roll-to-roll production of graphene films [28].

1.1.1.4 Limitations and applicability of graphene electronics

A clear limitation of graphene-based electronics, predicted from the absence of a bang gap, was the expected high current OFF-state of FETs made with graphene channels. The ON/OFF ratio, defined as the ratio between the maximum and minimum current obtained in the transfer characteristic, respectively, was in the one order of magnitude range in the first demonstrations. Opening a gap was attempted and predicted in three possible ways, namely by reducing the width of the graphene channel down to the nanoribbon range, by applying a perpendicular electric field to a graphene bilayer, or by applying strain [38]. But the strength of graphene for electronic applications would come not only from typical transistor-like applications, but oriented towards high-frequency response devices due to the high mobility of the electrons in graphene. For high-frequency operation, a transistor requires short channels, thin gates

and mobile charge carriers, in order to quickly respond and amplify small oscillations of the gate voltage. The transistor gain unity-cut-off frequency is the frequency at which the transistor gain rolls off to 1. Graphene transistors with cut-off frequency of 300 GHz have been demonstrated [38].

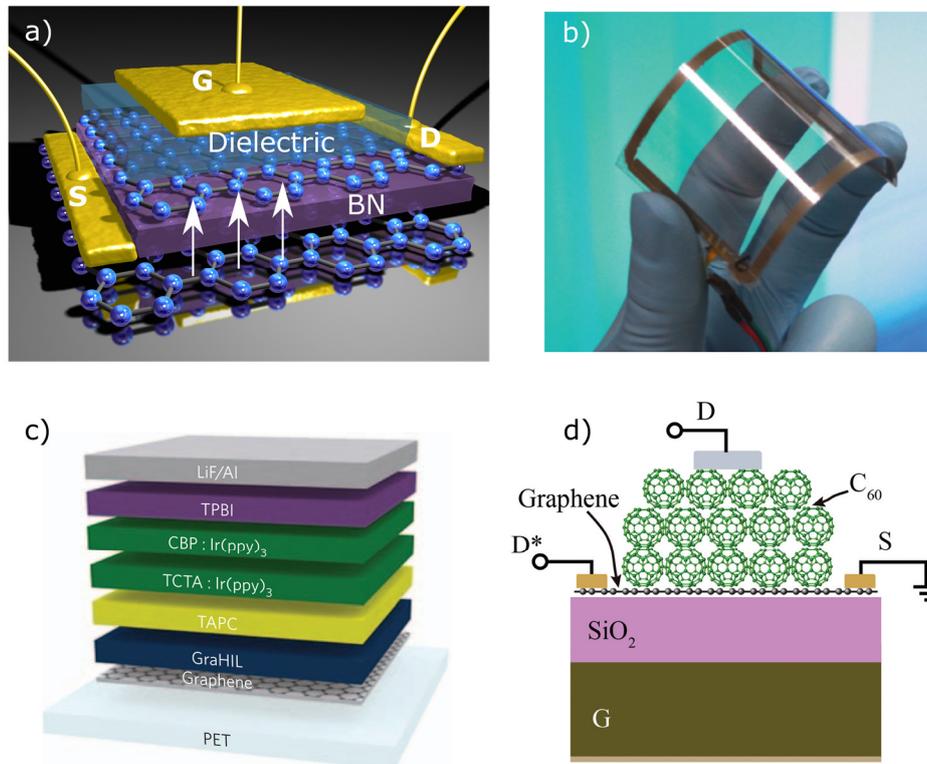


Figure 1.5 Electronic applications based on graphene. a) Resonant tunneling vertical graphene devices. Adapted from Ref. [39]. b) Bendable touch-pad based on graphene/polyethylene-terephthalate (PET). Adapted from Ref. [28]. c) Organic light emitting diode, where graphene plays the role of transparent electrode. Adapted from Ref. [40]. d) C₆₀-graphene heterostructure for vertical organic transistor operation. Adapted from Ref. [41].

The low density of states (DOS) of graphene also makes it a suitable material to explore its intrinsically low capacitance, also known as quantum capacitance. Quantum capacitance emerges whenever in an equivalent parallel plate capacitor one of the plates has a DOS orders of magnitude lower than typical metals as Au or Cu. Experimental measurements of the quantum capacitance of graphene place it at the level of 2-to-7 $\mu\text{F cm}^{-2}$, depending on the charged impurity concentration level [42]. Since the resistor-capacitor (RC) time constant depends both on device geometry considerations and on the sheet resistance of the graphene channel, the cut-off frequency f_{-3dB} of a graphene

diode is predicted to reach the terahertz operation regime. In such a case, graphene could also be a candidate for far-infrared rectennas [43], [44].

Figure 1.5 shows several electronic applications developed based on the unique properties of graphene.

Being one atom-thick, conductive, flexible, and transparent to visible light, graphene was also sought as an electrode for flexible organic light emitting diodes (OLEDs) [45], [46], and for substituting indium titanium oxide (ITO) in liquid crystal devices [47]. Additionally, benefiting from its weak screening to electric fields, due to the low DOS and electrostatically tunable work-function, graphene role as electrode for organic materials also enabled vertical transistor architectures, where the leading mechanism for transistor operation is the gate tunable Schottky energy barrier formed between the electrode and the semiconductor material [41]. These electrode features make graphene widely promising for contacting organic materials and enabling vertical transistor operation.

1.1.2 Transition metal dichalcogenides

1.1.2.1 Electronic properties

Immediately after graphene came beyond-graphene approaches [48]. Beyond-graphene refers to equivalent 2D materials that exhibit physical properties that overcome some of the problems of having a linear gapless energy dispersion close to the Fermi level, or having low spin-orbit coupling (SOC). Transition metal dichalcogenides (TMDs) were sought as first contenders for beyond graphene applications as they also share the weak out-of-plane vdW bonds, which among other benefits allow for microcleaving techniques to be employed to exfoliate single or few-layer flakes. TMDs are layered materials with formula MX_2 , where M is the transition metal element and X the chalcogenide element. These materials have been demonstrated to exhibit a wide range of electronic properties, from superconducting NbSe₂, magnetic CrSe₂, and semiconductor MoS₂ [49]. Group-VI transition metal dichalcogenides, namely (M = Mo, W; X = S, Se, Te), are known to have similar band dispersion and have trigonal prismatic structures [50]. They undergo an indirect-to-

direct transition when in the monolayer limit, have charge carrier effective masses comparable to those of Si, strong SOC, and some unique features as non-centrosymmetric crystal structures. A strong coupling between the spin and valley degrees of freedom emerges from the lack of an inversion symmetry in the crystalline structure [51]. These properties made TMDs highly appealing for electronic and optoelectronic applications [49]. Figure 1.6 summarizes the electronic properties of TMDs emerging from their crystal structure. Figure 1.6 a) and b) show the crystal structure of multi-layer TMDs, with AB-type stacking, and energy level alignment of the $M = \text{Mo}, \text{W}$; $X = \text{S}, \text{Se}, \text{Te}$ family, respectively.

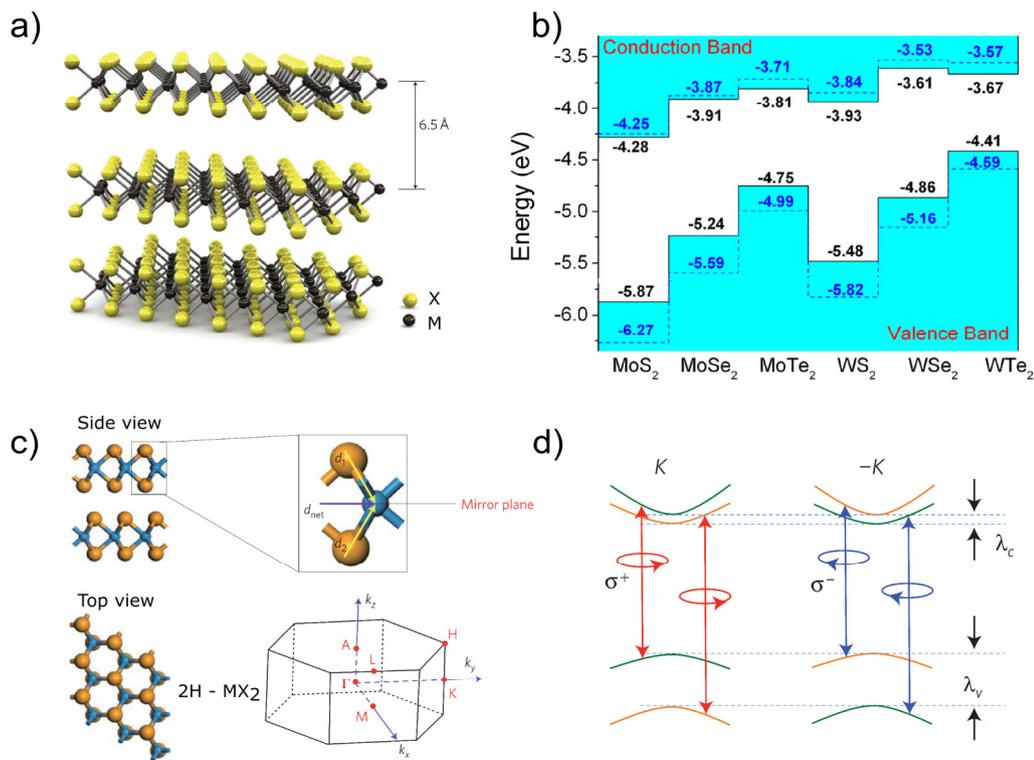


Figure 1.6 a) Trigonal prismatic crystal structures of MX_2 for the $M = \text{Mo}, \text{W}$; $X = \text{S}, \text{Se}, \text{Te}$ family. b) Band alignment of MX_2 monolayers. c) Side view and top view of AB stacking in bilayer MX_2 , resulting in the canceling of the net in-plane dipole moments from each monolayer. Brillouin zone of trigonal prismatic MX_2 . d) Spin-orbit coupling induced splitting, λ_C and λ_V , of the conduction and valence bands of monolayer MX_2 , with spin-valley locking due to the non-centrosymmetric crystal structure. Figure a) adapted from Ref. [52], b) from Ref. [50], c) from Ref. [53] and d) from Ref. [51].

For the particular case of MoS_2 and WSe_2 , they show an electron affinity of 4.3 and 3.6 eV, respectively, and band gaps of 1.8 eV and 1.6 eV in the monolayer limit,

respectively [50]. They are both semiconductors, with MoS₂ being a highly-doped *n*-type semiconductor, while WSe₂ is a *p*-type semiconductor.

Figure 1.6 c) and d) detail how due to the non-centrosymmetric crystal lattice TMDs exhibit spin-valley locking, making them useful for exploring valley physics.

The first demonstrations of MoS₂ single layer transistors were reported on dual-gated channels contacted with evaporated gold, using HfO₂ top gate and SiO₂ back gate [52]. Although the first reported field-effect mobility was determined to be 200 cm² V⁻¹s⁻¹, nearly one order of magnitude higher than what was reported for MoS₂ transistors on SiO₂, the real mobility has been found to be highly overestimated due to the floating top-gate in some of the transfer measurements. Later analysis led to a corrected value of 15 cm² V⁻¹s⁻¹, on par with regular SiO₂ devices [54]. Regardless of metal contact, MoS₂ transistors persist on exhibiting *n*-type behavior, with different metallic contacts exerting small changes in the transistor operation. This strong Fermi level pinning is a result of the presence of surface states due to the sulfur vacancies. Accessing *p*-type transport in MoS₂ was achieved via sub-stoichiometric molybdenum trioxide (MoO_x, $x < 3$) high work function contacts [55]. Improving the mobility of MoS₂ transistors was again performed via encapsulation with BN, but this time using graphene electrodes to overcome the high contact resistances of traditional metal contacts [56]. The graphene electrodes were themselves contacted to metal contacts via one-dimensional approaches to minimize contact resistance. Up to date, the highest performing MoS₂ FET was an edge contact multi-terminal BN-encapsulated MoS₂ monolayer using graphene electrodes, with the transistor operation showing field-effect mobility as high as 3.5×10^4 cm² V⁻¹ s⁻¹, together with SdH oscillations.

WSe₂ transistors on the other hand were demonstrated to largely depend on metal contact, with *n*-type transistors being a result of the use of low work-function metals as In [57], ambipolar transistors by using metals with mid-range work-functions as Pd or graphene [58], and *p*-type transistors resulting from the use of high work function metals as Pt [59]. Focusing on unipolar operation allows one to obtain higher mobility devices, although losing the ambipolarity. For ambipolar devices, the higher Schottky barriers affect the current density and therefore the extracted mobility. Both materials have strong localization effects that lead to metal-insulator transitions based on carrier density [59], [60].

1.1.2.2 Applicability and limitations of TMDs

In a similar way to graphene, TMDs benefit from atomically flat vdW substrates as BN. Using ultra-clean double encapsulation with BN techniques, TMD-based electronics has been associated to promising performances and applicability in electronic and optoelectronic for beyond CMOS technologies, being demonstrated in logic circuits as complementary inverters, ring oscillators, field-effect transistors, vertical field-effect transistors based on band-to-band tunneling effects, and also light emitting diodes.

Figure 1.7 shows several electronic realizations of highly performing TMD-based devices.

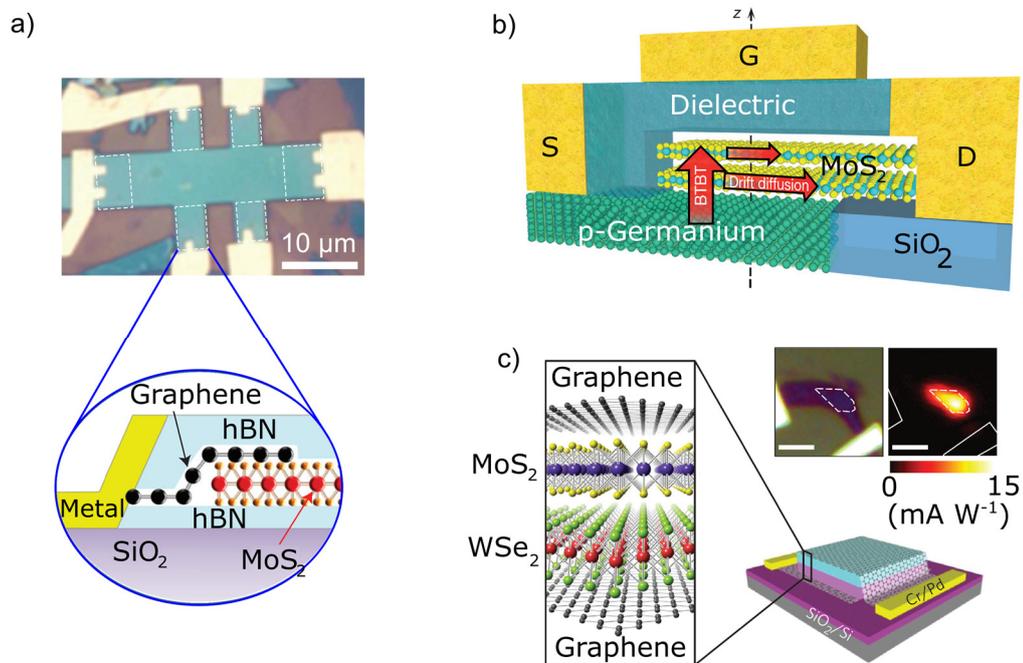


Figure 1.7 Electronic devices based on TMDs. a) Multi-terminal encapsulated MoS₂ transistor with graphene contacts with highest reported mobility of 34000 cm² V⁻¹ s⁻¹. Adapted from Ref. [56]. b) Sub-thermionic emission transistor concept based on band-to-band tunneling, using MoS₂ channel. Adapted from Ref. [61]. c) Light emitting diodes based on a vertical *p-n* junction of WSe₂ and MoS₂. Adapted from Ref. [62].

The demonstrations of highly-performing devices have relied on complex device designs to address one of the fundamental detrimental effects in TMDs based electronics, which is the strong current fluctuations at low-doping regimes. TMDs exhibit strong fluctuations of the electrical current based on the carrier density and carrier mobility oscillations [63]–[68]. These fluctuations emerge from intrinsic (channel) and extrinsic

sources (contacts, dielectrics, environment conditions), and can be a limiting factor in the performance and application of TMDs in nanoscale devices. By studying the power spectral density (PSD) of the current fluctuations in MoS₂ FETs, the understanding of the nature of the fluctuations is converging over correlated carrier number-mobility fluctuations as the main mechanism driving the emerging low-frequency noise (LFN) [64], [68]–[72]. Additionally, the LFN shows a strong dependence with channel thickness, dielectric, and environment conditions, with some conditions pointing at $1/f$ -type Hooge mobility fluctuations (HMF) as the origins for LFN in MoS₂ device [65]. Besides oscillations of the electrical currents, the dielectric environment and surface contaminations strongly affects current transient decays, which on SiO₂ substrates have been demonstrated to reach hour long relaxations [73], [74]. These strong decays and fluctuations adversely affect electrical studies of TMDs at low-doping regimes.

1.2 Two-dimensional materials in the context of spintronics

The core entity in spintronics is the electron spin. By generating, detecting and manipulating spins, spintronics aims to control the intrinsic magnetic moment of electrons for information processing. In this context, one of the first experimental realizations of a device based on spin transport was the multilayer stack of alternate ultra-thin ferromagnetic and non-magnetic metals proposed by A. Fert and P. Grunberg [75], [76]. While these devices exhibited a large change in resistance with the magnitude of the magnetic field applied parallel to the ferromagnetic layers, they did not allow for the manipulation of the spins. Manipulating spins would require thicker non-magnetic channels with longer spin relaxation lengths. In this regard, conductive carbon-based materials are well suited for spintronics since they benefit from low intrinsic spin-orbit coupling and are therefore expected to provide long spin relaxation lengths, λ_s . In a diffusive conductive non-magnetic material, the spin relaxation length is connected to the spin relaxation time, τ_s , and spin diffusion coefficient, D_s , by the relation $\lambda_s = \sqrt{D_s \tau_s}$. Therefore, combining high mobility and low SOC, graphene was initially predicted to be a unique platform for millimeter long relaxation lengths.

1.2.1 Graphene

1.2.1.1 Lateral spin valves

The initial approaches used to demonstrate spin transport in graphene were lateral local and non-local spin valves [77],[78]. Figure 1.8 shows a lateral non-local spin-valve with the injection, detection, and transport scheme. The principles of operation of a non-local spin valve consider the use of ferromagnetic electrodes to inject a spin polarized current into the non-magnetic channel through a tunnel barrier, generating a local accumulation of a spin-polarized chemical potential in the graphene channel underneath the ferromagnetic electrode and tunnel barrier [79]–[81].

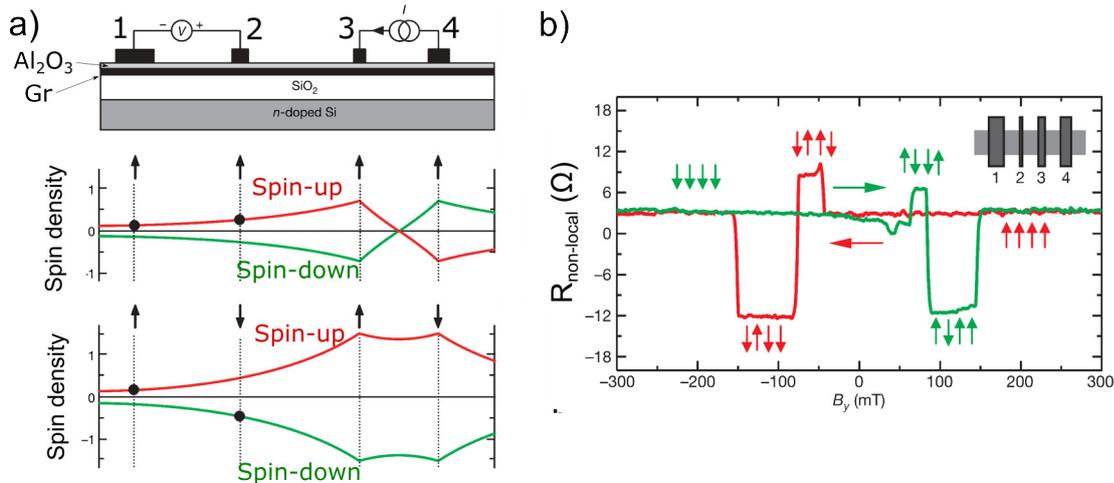


Figure 1.8 a) Non-local lateral spin-valve. Spin density profiles indicate operation and detection principles. Black arrows show the in-plane orientation of the magnetization of the ferromagnetic electrodes. Black spots indicate the voltage reading of the electrodes. b) Non-local resistance ($R_{NL} = V_{21}/I_{34}$) at 4 K for a non-local lateral spin-valve with four ferromagnetic electrodes. Vertical arrows indicate the magnetization orientation of the electrodes. Horizontal arrows show the direction of the magnetic field sweep. Figures adapted from Ref. [77].

The non-equilibrium local accumulation will drive the spins to diffuse isotropically across the graphene channel according to Ohm's law for each species ("up" and "down"), with the spin-polarization decaying exponentially with distance, with characteristic spin-relaxation length λ_s . Measuring the voltage drop between a ferromagnetic electrode placed close-by the injecting electrode and an electrode placed in such a way that the chemical potential of both species are equal (no spin-polarization) would allow for the determination of the spin-signal related to the imbalance at the ferromagnetic detector. Following Figure 1.8 a) device scheme, the two most right-side ferromagnetic electrodes inject an electrical current from electrode 3 to 4, and electrodes 2 and 1 measure the voltage drop between them. The spin density profiles indicate the chemical potential of the two different spin species along the device structure during operation, with the arrows indicating the relative orientation of the electrodes magnetization, and the black dots the relative voltage reading of the electrodes due to their magnetization. By applying an external magnetic field parallel to the ferromagnetic electrodes orientation, from an initially all-electrode saturated in the same orientation -300 mT (or 300 mT), the device switches into an anti-parallel state of the ferromagnetic electrodes with lower non-local resistance ($R_{NL} = V_{21}/I_{34}$) (Figure 1.8

b)). The spin signal is defined as the difference between the non-local resistance for the parallel and anti-parallel configurations of the injection and detection electrodes.

One of the on-going drawbacks of spintronics is the magnitude of the generated spin-signal. Since these structures are at the micrometer size and use tunnel-barriers, the excitation currents are limited to the microampere range. The non-local voltage signals generated will also be in the same range of microvolts. Future electronic applications must rely on larger signals if they are to be implemented in logic devices [82]–[85].

The use of lateral diffusive spin valves also allows for the manipulation of the spin orientation diffusing along the channel with an external magnetic field. One of the ways to do so is via the Hanle-effect, where by applying a magnetic field perpendicular to the orientation of the spin and its direction of propagation in the graphene channel leads to the precession of the spin via the Lorentz force. The dynamics of the spin precession and the dependence of the non-local spin signal with the magnetic field are encoded in the Hanle precession equation [77]. The precession of the spins will lead to a dependence of the non-local signal with the magnetic field. Fitting the experimental Hanle curve to the model allows for the determination of the spin-relaxation length without requiring a length dependence of the graphene channel. This feature is highly-regarded as the fabrication of tunnel barriers is still not reliable, which impacts the extraction of a spin relaxation length via transmission-line methods.

The first experimental demonstrations of spin transport in graphene have found λ_s to be greatly off the predicted millimeter long mark, although still exhibiting impressive 1.5-2 μm lengths [77]. The low-mobility of the initial samples and spin injection were found to be the limiting factors. By improving the dielectric environment and the tunnel barriers these numbers have been considerably improved to 24 μm in BN encapsulated graphene [86], and spin lifetimes exceeding 12 ns [87]. With the aid of spin-drift, λ_s was demonstrated to reach up to 90 μm length scales [88].

Although graphene has been found to be a great material for spin transport, spin manipulation for practical device purposes with fields other than an external magnetic field is yet to be demonstrated. The Datta-Das spin transistor [89], which envisions the manipulation of the spins via the interaction of the spin-orbit coupling with an external electric field (via Rashba spin-orbit interaction), has been demonstrated once in a

platform other than graphene [90]. Alternative device architectures have demonstrated the use of vdW heterostructures of graphene and MoS₂ for spin switches, where the TMD acts as a spin-sink controlled via electron gating effects [82].

1.2.1.2 Spin Hall effect

In systems with strong spin-orbit interaction (SOI), one additional effect emerges from the asymmetric spin-dependent scattering that leads to the accumulation of spins at the lateral boundaries of the conducting channel [91], [92]. This effect is similar to the Hall effect, where under the application of a magnetic field perpendicular to the conducting channel plane the Lorentz force drives an accumulation of charges at the boundaries of the conductor. Figure 1.9 shows the spin accumulation resulting from the spin Hall effect (SHE) at the edges of a semiconductor, and the electrical detection relying on the SHE of a spin current injected from ferromagnetic electrodes.

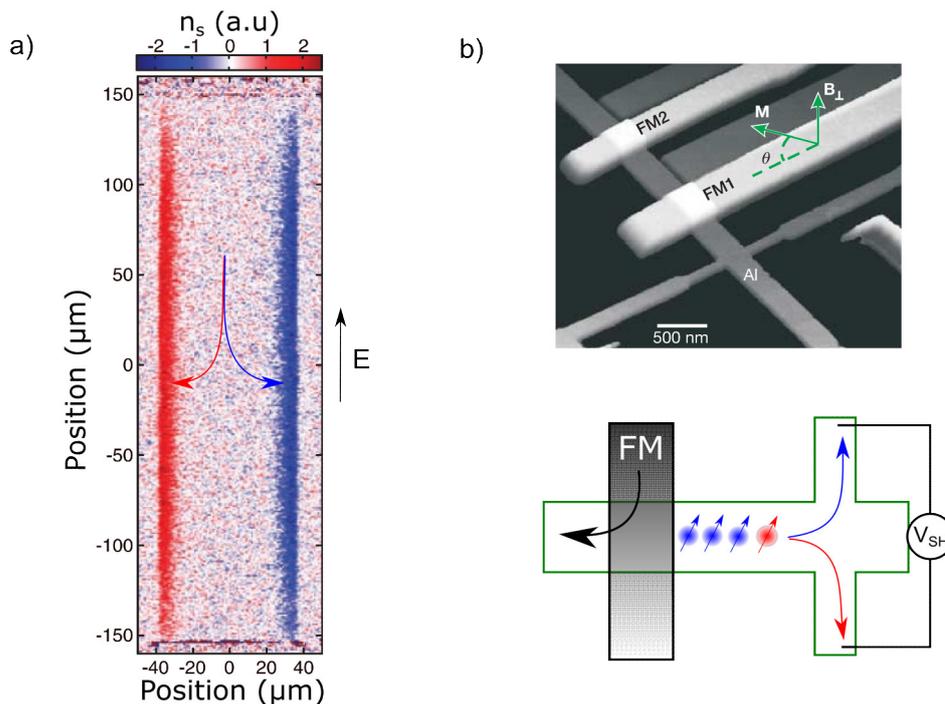


Figure 1.9 a) Accumulation of opposite spins at opposite edges of a GaAs stripe via spin Hall Effect, measured by optical Kerr effect. Adapted from Ref. [93]. b) Electrical detection of a spin polarized current via inverse spin Hall effect, injected by a ferromagnetic (FM) electrode. The injected spin-polarized current leads to the generation of a transverse charge current. Adapted from Ref. [94].

In the case of a system with strong SOI, and in the absence of an external magnetic field, spins “up” and “down” will scatter in opposite directions, transverse to the current flow, due to the strong SOI, generating a spin-polarized accumulation of charges at the boundaries of the conductor. The conversion of a charge current density, J , into a spin current density, J_s , is referred to as spin Hall effect [95], and the efficiency of the conversion is measured by the spin Hall angle, $\theta_{SH} \equiv J_s/J$. The coupling of spin and charge currents leads to an inverse effect where a spin-current generates a charge current, designated as inverse spin Hall effect (ISHE). This particularity of the SHE and ISHE generated a set of non-local strategies to release spintronics from the cumbersome magnetic elements (ferromagnetic contacts) used to inject and detect the spin signals, relying only on a single non-magnetic material to perform all the tasks.

1.2.1.2.1 Nonlocality

Nonlocality refers to the demonstration of spin generation, transport and detection using a single non-magnetic transporting channel, relying on spin Hall and inverse spin Hall effects. Non-local strategies use an attractively simple H-bar shaped channel to achieve such goal, implement the full electrical, free of magnetic elements, spin generation, transport and detection. By injecting a current in one arm of the H-bar and detecting a voltage in the other arm of the bar it is possible to pin-point spin Hall-related origins to non-local voltages detected [96]. In the particular case of graphene, two strategies were followed to demonstrate spin transport based on non-local measurements. First, by inducing SOC in the graphene channel, and, second, relying on external magnetic fields to generate spin currents via Zeeman induced splitting of the spin sub-bands [97]. With the H-bar shaped graphene channel, one can devise a non-local method based on the SHE and ISHE to inject and detect spin signals. Both research directions have been demonstrated in graphene. In the first case by the means of spin-orbit proximity effects [98], hydrogenation [99], [100], and even plain CVD grown graphene [101], relying on transition metal impurities. In the second case, by using pristine graphene on SiO₂ or encapsulated on BN and applying external magnetic fields perpendicular to the channel [97], [102].

Figure 1.10 a) and b) show giant non-local effects in high-quality pristine graphene on BN samples, and Figure 1.10 c) and d) show non-local signals emerging in

plain CVD samples on SiO_2 substrates due to the spin-orbit induced by the residual copper impurities.

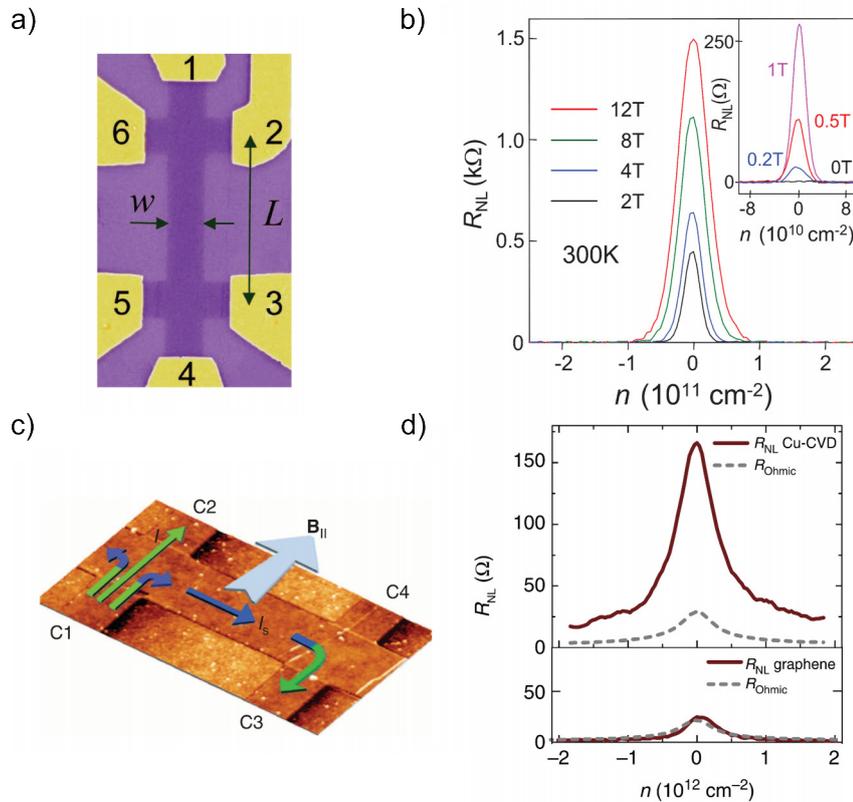


Figure 1.10 a) H-bar shaped pristine graphene sample on BN for Zeeman induced SHE/ISHE spin injection and detection of giant non-local signals. b) Non-local signal as a function of carrier density, greatly enhanced at the Dirac point and increasing with higher magnetic fields. c) H-bar shaped CVD graphene sample on SiO_2 . d) Non-local signal as a function of carrier density at RT for CVD graphene samples, with enhanced nonlocality at the Dirac point. Ohmic contributions indicated. Figures a) and b) were taken from Ref. [102], and Figures e) and f) from Ref. [101].

By the means of a perpendicular applied magnetic field, the Zeeman induced spin splitting of the bands allows for spin currents to be generated and detected via SHE and ISHE, respectively. In a H-bar shaped sample, driving a current through contacts 6-2 allows for the spins generated to diffuse through the channel and reach contacts 5-3. The non-local signal in Figure 1.10 a) is taken as $R_{NL} = V_{53}/I_{62}$. This giant increase in the non-local signal happens at the Dirac point in graphene [97]. For this reason, a gate dependent study of the non-local signal shows a strong dependence with the electron density. The studies rely on the consideration that the classical non-local signal sources are only related to the van der Paw “Ohmic” background from the injected current.

Figure 1.10 d) shows non-local signals induced by SOC without any external magnetic field. The use of in-plane magnetic fields parallel to the injection of charge current is used for the spin manipulation of the spins in the channel, achieving an equivalent Hanle-like precession and modulating the spin signal. Although the non-local signals have been reported at room temperature, the Hanle precession feature has so far only been detected at liquid helium temperatures [98], [99], [101], [103].

1.2.2 Transition metal dichalcogenides

Spin transport in TMDs has not developed as strongly as in graphene devices. Although TMDs exhibit strong SOC, the presence of the non-centrosymmetric crystal structure also leads to the prediction of long spin relaxation times [104], which have been demonstrated to exceed 3 ns [105]. Probing for spin effect in TMDs has been only at the reach of optical pumping techniques [105], [106]. Spin injection and detection via the regular lateral non-local spin valves using ferromagnetic electrodes is yet to be demonstrated in TMDs, although several works have already hinted at the possibility of achieving spin injection via spin absorption methods in 2D vdW heterostructures [82].

1.2.2.1 Weak-localization effects

Due to the strong localization effects and SOC in TMDs, alternative methods to access spin information via electrical measurements were pursued exploring weak (anti)-localization. In thin-films of disordered conductors, the coherent interference of backscattered electrons leads to a correction to the resistance that depends on the SOI. Materials with strong SOI exhibit a positive correction to the conductivity (weak anti-localization), while materials with weak SOI exhibit a negative correction to the conductivity (weak-localization). This correction to the resistance can be suppressed by applying a magnetic flux perpendicular to the surface of the conductor, destroying the quantum interference. The contribution to the resistance from the weak (anti)-localization effect can then be studied using magnetoresistance measurements. The theoretical framework of Hikami-Larkin-Nagaoka (HLN) captures these effects, and allows scattering related information to be extracted, namely elastic, inelastic, and spin-orbit scattering rates [107]. Since spin scattering mechanisms are related to SOI, by

studying the dependence of the spin-orbit scattering rate with the mean free path of the disordered conductor it is possible to infer on the nature of the spin scattering mechanisms present in the material [108]. When the spin relaxation time is inversely proportional to the electron mean free path, the spin scattering mechanisms is known as Dyakonov-Perel (DP); when the spin relaxation time is proportional to the electron mean free path, it is designated as Elliot-Yaffet (EY).

The proportionally between the spin-orbit relaxation time, determined from magnetoresistive measurements in the framework of the Hikami-Larkin-Nagaoka (HLN) theory, and the spin lifetime in materials with strong SOC would work as an indicator for the spin transport of MoS₂ [109]. For electron densities over 10^{13} cm⁻², Schmidt et. al. determined Dyakonov-Perel to be the main spin relaxation mechanism in highly doped MoS₂ [110].

One additional application of TMDs for spintronics comes from proximity effects, where by being placed in contact with graphene, the strong SOI present in the TMD layer can be felt by the electrons in the atomically thin 2DEG [98], [111].

1.3 This thesis

In this thesis, we explore a range of two-dimensional materials for electronics and spintronic applications, namely graphene, MoS₂, WSe₂, and BN. In chapter 1 we motivate the current line of research in 2D-material-based electronics and spintronics, namely on graphene and TMDs. In chapter 2 we introduce the required concepts to understand charge transport in metal/semiconductor and metal/insulator/semiconductor junctions, magnetoresistive effects in 2D materials, and full electrical non-local spin transport strategies. In chapter 3 we present the experimental techniques used to fabricate the 2D vdW-based devices. In chapter 4 we attempt to study the magnetoconductance of MoS₂ few-layer devices on SiO₂ under low-doping regimes using Hall bar geometries and electron doping via field-effect, and are lead to study the roots of the low-frequency noise and current decays in such FETs. In chapter 5 we explore WSe₂ FETs on oxides and study the impact of having BN as both a dielectric and encapsulating layer. In chapter 6 we deal with CVD graphene magnetoresistance and explore non-local effects at the macro and microscale. Chapter 7 and 8 deal with graphene electronics, namely exploring CVD graphene electrodes for organic semiconductor lateral and vertical FETs, and the large-scale fabrication of lateral metal/insulator/graphene diodes, respectively. In chapter 9 we conclude about the work presented in the thesis.

Chapter 2

Transport in two-dimensional materials

In this chapter, we introduce the necessary concepts to address electron and spin transport in two-dimensional materials. We start with the fundamentals of electron transport in metal/semiconductor and metal/insulator/semiconductor junctions. These concepts will be useful for understanding the operation of the MoS₂ and WSe₂ field-effect transistors (explored in chapter 4 and 5), the driving mechanisms for current fluctuations (chapter 4), the operation of lateral and vertical organic field-effect transistors using graphene electrodes (chapter 7), and of metal/insulator/graphene in-plane lateral diodes (chapter 8). Afterwards, we introduce magnetoresistive phenomena characteristic of two-dimensional systems, namely the theoretical framework for the interpretation of weak-(anti) localization effects and its connection with spin transport in TMDs, and the quantization of conductance in graphene samples. We finish with non-local signals in the spin Hall regime, and the effects of external magnetic fields in semi-metals with linear energy dispersion and its contribution to spin transport (chapter 6).

2.1 Electronic transport across metal/semiconductor junctions

The transport theory of metal/semiconductor junctions is based on the band theory of solids [6]. Understanding metal/semiconductor junctions is fundamental to understand metal/semiconductor rectifying systems, and the formation of low-resistance ohmic (linear current-voltage characteristics) contacts that ease the passage of current in and out of semiconductors channels.

An energy barrier, $q\Phi_B$, where q is the elementary charge and Φ_B the barrier potential, is formed whenever a metal contacts a semiconductor [6]. Mobile charge carriers in the metal and semiconductor have distinct energy levels. While the energy

states of the mobile charge carriers in the metal mainly lie at the Fermi level energy, in semiconductors, the energy states lie at and over the conduction band, with charge carriers being thermally excited from the valence band, leaving unoccupied states (holes) behind. When the two materials are brought together, the abrupt gradient in the electrons energy will drive the charge carriers from one material into the other until a thermal equilibrium is reached, and the Fermi level energy is equal and constant throughout both materials. Because of this re-distribution of charge carriers, the non-mobile donor/acceptor impurities in the semiconductor close to the interface will become uncompensated and distribute deeply into the semiconductor channel. This profile will generate an electric field that will bend the conduction and valence bands of the semiconductor. The band bending in the metal will be insignificant due to the DOS being orders of magnitude larger than the DOS of the semiconductor. This thermalization process is described in the energy band diagram in Figure 2.1 for the case of a metal/*n*-type semiconductor junction.

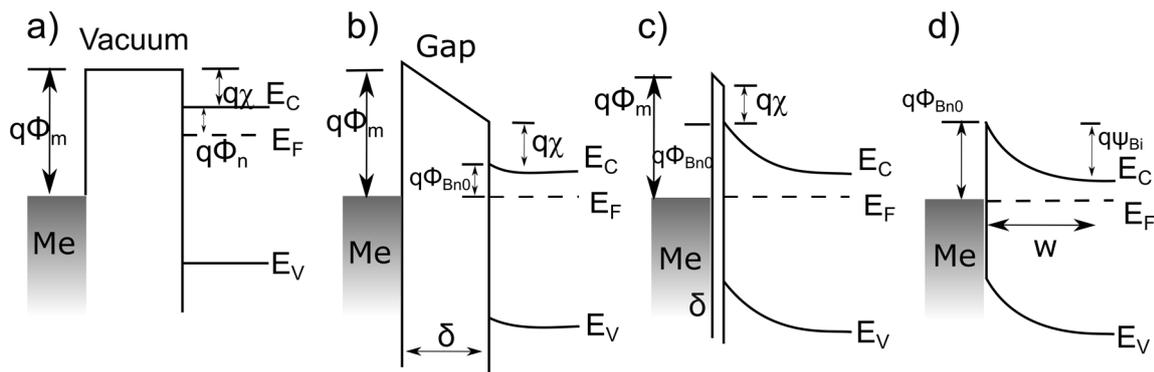


Figure 2.1 Energy band diagram of a metal/*n*-type semiconductor contact. a) Energy alignment when the metal and semiconductor are not in contact and are isolated. b) Bringing these two materials together leads to the development of an electric field and to a re-alignment of the vacuum and Fermi levels. c) Reduced gap. d) Metal/*n*-type semiconductor in contact. Figure adapted from Ref. [6].

The metal has work function $q\Phi_m$, which is the difference between the vacuum level ($E = 0$ eV), and the Fermi level, E_{Fm} , of the metal. The semiconductor has electron affinity $q\chi$, with E_F placed in the band gap closer to the conduction band, with energy E_C , to represent the larger number of electrons than the number of holes in the valence band, E_V . The difference between the metal work function and the semiconductors electron affinity gives the height of the energy barrier, $q\Phi_B$, designated as Schottky barrier. The uncompensated ionized impurities will result in a built-in potential, ψ_{bi} ,

with energy, $q\psi_{bi}$. At the interface, in the semiconductor side, the energy difference between the Fermi level and the conduction band will be larger than when in the bulk of the channel, indicating a lower density of electrons than further away from the interface. The charge depleted region is referred to as depletion layer, with width W .

When this junction is biased with a voltage difference V between two electrodes placed at each of the materials, current will flow unevenly for positive and negative bias, V . The forward bias is referred to as the V for which the current density J has larger magnitude, and the reverse bias as the one with the lowest J magnitude. The coexistence of the energy barrier and of the band bending will result in three main transport mechanisms influencing the current-voltage (I - V) profiles of the junction: thermionic emission, diffusion, and quantum tunneling. The charge transport in metal/semiconductor junctions is referred to as a majority carrier transport.

Thermionic emission is a mechanism in which only the electrons that are thermally excited with enough thermal energy $k_B T$ to overcome the barrier $q\Phi_B$ will contribute to the transport across the junction. Clearly, this mechanism is strongly temperature dependent. The full derivation of the total current density flowing through a metal/semiconductor junction can be found in Ref. [6]. The complete thermionic emission transport equation is given by the equation,

$$J = \left[A^* T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right) \right] \left[\exp\left(\frac{qV}{k_B T}\right) - 1 \right], \quad (1)$$

where A^* is the Richardson constant, T the thermodynamic temperature, k_B the Boltzmann constant, and V the applied bias. This expression is usually written in a more compact way by substituting the first solid bracket term and re-writing as

$$J = J_{TE} \left[\exp\left(\frac{qV}{k_B T}\right) - 1 \right], \quad (2)$$

where, J_{TE} refers to the thermionic emission current saturation at zero bias. The quantum tunneling current contribution included into the thermionic emission theory results in

$$J = J_0 \left[\exp\left(\frac{qV}{\eta k_B T}\right) - 1 \right], \quad (3)$$

where J_0 is the saturation current density obtained by extrapolating the current density from the log-linear plot at $V = 0$, and η is the ideality factor, related to the slope.

When the main contribution mechanism is thermionic emission, the saturation current corresponds to the saturation current of thermionic emission, and η is close to unity. Whenever the tunneling contribution increases, the ideality factor diverges from unity and J_0 increases. The tunneling contribution arises due to the band bending. When the depletion width is small enough, it allows for electrons with energy lower than the Schottky barrier to tunnel through the depletion layer into available states at the semiconductor or metal. Metal/semiconductor junctions with a large energy barrier are usually referred to as Schottky diodes due to the asymmetric and non-linear I - V curves, favoring electron transport for the forward bias polarity.

Real metal/semiconductor junctions on the other hand will exhibit device performances that do not always follow the above predictions. Undesired processes during fabrication may lead to the presence of thin layers of materials in between the metal and the semiconductor.

2.1.1 Metal/insulator/semiconductor diode

When an insulator layer in the range of a few nanometers is introduced between the metal and semiconductor a tunnel diode is formed. The additional insulator layer will introduce an additional energy barrier, and will effectively decrease the Schottky barrier between the semiconductor and the metal, since there will be a voltage drop developing across the insulating layer. The transport between the semiconductor material and the metal will have tunneling and thermionic emission contributions. The output characteristics equation for such devices is written as

$$J = \left[A^* T^2 \exp(-\sqrt{\zeta} \delta) \exp\left(-\frac{q\Phi_B}{kT}\right) \right] \left[\exp\left(\frac{qV}{\eta kT}\right) - 1 \right], \quad (4)$$

where ζ and δ are the effective barrier and thickness of the introduced interfacial layer. While the $\exp(-\sqrt{\zeta} \delta)$ term can be seen as a correction of the Richardson constant, A^* , one additional effect of the presence of the insulating layer is the increase of the non-linearity of the device, η , due to the presence of increased tunneling effects.

2.1.2 Metal/insulator/metal diode

If instead of a semiconductor in a metal/insulator/semiconductor junction we now have a metal, the metal/insulator/metal junctions will exhibit interesting transport properties based on tunneling effects [6]. Ideally, the contact between two metallic electrodes leads to a linear I - V output characteristics, with low resistance. Low-resistance Ohmic contacts are important to ensure that the electronic properties of the channel can be probed without having a large portion of the applied bias dropping through the contact resistance. Although low-resistance Ohmic contacts are a requirement for the easy injection and extraction of electrons from one material to another, adding a thin enough insulating layer in-between two materials provides more than a constant series resistance. Figure 2.2 shows the energy alignment between two metal electrodes of the same material separated by a thin insulating layer, and the resulting tunneling processes under bias.

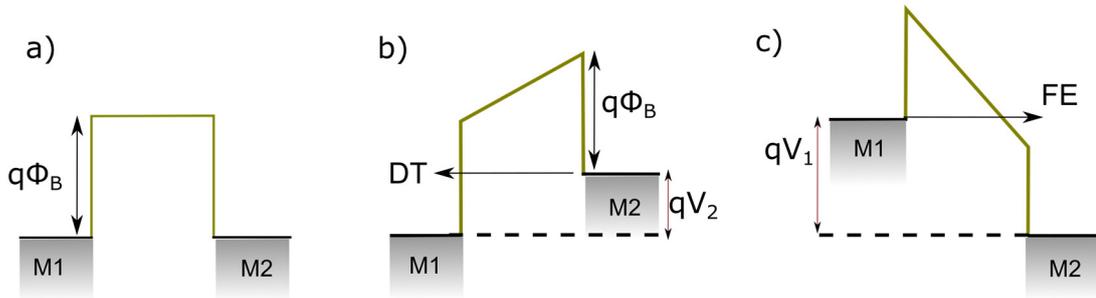


Figure 2.2 Tunneling processes between two metal electrodes separated by a thin insulator. a) Energy level alignment between the metal electrodes (M1,M2) and the insulator. b) Direct tunneling (DT). c) Field emission process (FE).

For an arbitrary insulating tunnel barrier between two electrodes, the output characteristics is given by the Simmons approximation [112], written as

$$J = \frac{q}{4\pi^2\hbar d^2} \left\{ \left(q\Phi_B - \frac{qV}{2} \right) \exp \left(-\frac{2d\sqrt{2m_e}}{\hbar} \sqrt{q\Phi_B - \frac{qV}{2}} \right) - \left(q\Phi_B + \frac{qV}{2} \right) \exp \left(-\frac{2d\sqrt{2m_e}}{\hbar} \sqrt{q\Phi_B + \frac{qV}{2}} \right) \right\}, \quad (5)$$

where d is the barrier width, and m_e is the electron effective mass (in the metal electrodes). This expression outputs a non-linear symmetric I - V output characteristics.

In the low-bias and high-bias case, two approximations can be performed to the tunneling current that output distinct dependences with V .

In the low-bias regime, the barrier between electrodes is approximated as a rectangular barrier and the resulting tunneling current referred to as non-resonant and direct. The Simmons equation under these conditions reduces to a linear I - V relationship

$$I \propto V \exp\left(-\frac{2d\sqrt{2m_e q \Phi_B}}{\hbar}\right). \quad (6)$$

In the high-bias regime, the barrier becomes trapezoidal due to leveling of the metal electrodes Fermi level, and if V exceeds the barrier height, the output characteristic becomes,

$$I \propto V^2 \exp\left(-\frac{4d\sqrt{2m_e q \Phi_B^3}}{3\hbar q V}\right). \quad (7)$$

Metal/insulator/metal junctions rely on the speed of transport of the electrons and the non-linear I - V s to provide the most suitable platforms for ultra-high frequency applications.

2.1.3 Metal/insulator/semiconductor capacitor

Metal/insulator/semiconductor capacitors are fundamental building blocks for logic devices. In this case, the width of the insulator is such that it prevents tunneling, and the energy gap such that the thermal activated electrons from the metal or semiconductor cannot access the conduction band of the insulator. The most common structure is the metal/SiO₂/Si heterostructure, where Si benefits from the thermal growth of SiO₂ at high temperature and under an oxygen rich environment. Figure 2.3 summarizes the two types of metal/insulator/semiconductor capacitors under biasing conditions, representing the three most important conditions of operation: accumulation, depletion, and inversion. Accumulation refers to the addition of mobile majority carriers at the oxide/semiconductor interface by applying a positive/negative bias for n -type/ p -

type semiconductors, respectively, between the metal and the semiconductor. Depletion on the other hand refers to the decrease of the majority carriers in the n -type/ p -type semiconductors via a negative/positive bias for n -type/ p -type semiconductors. The inversion condition happens when the negative/positive bias for n -type/ p -type semiconductors is large enough to drive enough band bending such that at the interface of the oxide/semiconductor the majority carrier inverts from electrons/holes to hole/electrons for n -type and p -type semiconductors, respectively.

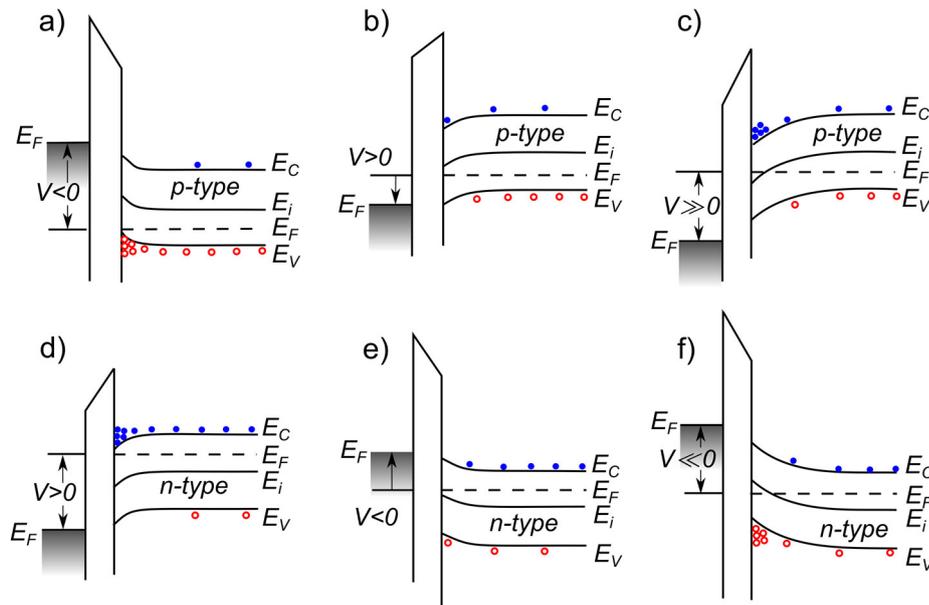


Figure 2.3 a), b), and c), metal/insulator/ p -type semiconductor accumulation, depletion and inversion conditions, under negative, positive and further positive bias, respectively. d), e), f) metal/insulator/ n -type semiconductor accumulation, depletion and inversion conditions, under positive, negative and further negative bias, respectively. Figures taken from Ref. [6]

Most importantly, the Fermi level crosses the intrinsic energy level of the semiconductor. When the applied bias, V , is such that the resulting adjustment of the bands is a constant energy level for the conduction and valence bands, the capacitor is said to be in the flat-band condition. In these structures, the thickness of the insulator layer is such that resulting current density is negligible. One useful quantity to describe the device operation is the surface potential, which is defined as the energy difference between the intrinsic energy level at the interface and bulk.

The usefulness of these structures becomes apparent when seen from the point of view of a metal-oxide-semiconductor field-effect transistor.

2.1.3.1 Metal-oxide-semiconductor field-effect transistors

The metal-oxide-semiconductor field-effect transistor (MOSFET) is up to date the most useful building block for logic applications [6], [38]. MOSFETs are three-terminal devices composed by the MIS capacitor, commonly referred to as gate, and by drain and source metallic contacts (with energy barriers lower than $3 k_B T$) to inject charge carriers into the semiconductor. The resistivity of the channel is controlled with a gate bias, V_G , which modulates the carrier density of the semiconductor close to the interface with the oxide. A transversal bias applied to the semiconductor between the drain and source electrode, V_{DS} , will drive the charge carriers. The two important characteristics of a MOSFET are its output and transfer characteristic. Figure 2.4 a), b) and c) show the typical structure of a Si MOSFET, the transfer and the output characteristic, respectively.

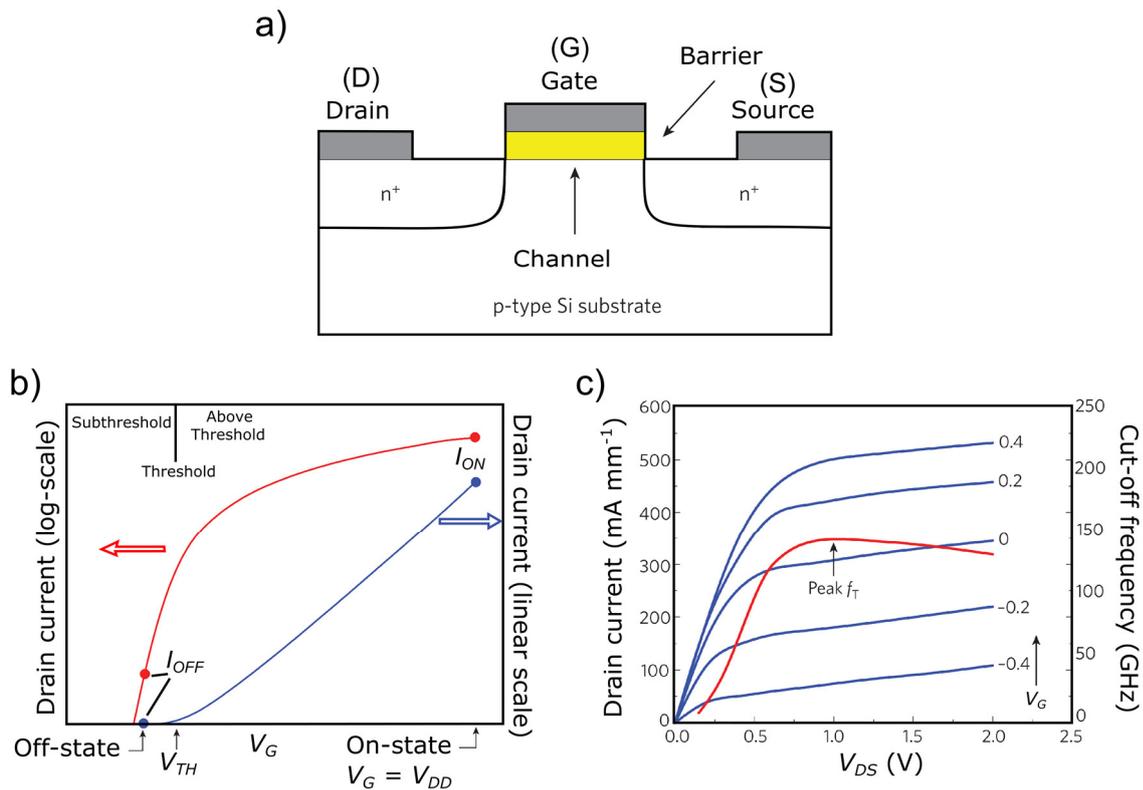


Figure 2.4 a) Cross-section of a *p*-type Si MOSFET. b) Transfer characteristic in linear (blue) and log (red) scale. c) Output characteristics (blue) and gain cut-off frequency (red). Figures a), b) and c) are adapted from Ref. [38].

In the transfer characteristics of the MOSFET there are three important regimes: the off-state, the subthreshold region, and the above-threshold region. The off-state

defines the static power consumption of MOSFETs. For sufficiently low gate voltage (ideally 0 V, to make sure the power consumption is small), the MIS structure in the MOSFET does not drive an inversion layer. When the V_G is increased, V_{DS} will drive increased amounts of current through the device. While V_G is below a threshold limit, V_{TH} , the current will increase exponentially with the gate bias. Over the threshold limit, the current characteristic will depend nearly linearly with the increasing gate bias. In this regime, the change in I_{DS} for a given change in V_G is called terminal transconductance, g_{mt} . This value is usually taken in as an estimate of the intrinsic transconductance when using two-point measurements. Four-point measurements allow for the resistances introduced by the source and drain contacts to be excluded and for a better estimate of the intrinsic transconductance. The device is considered ON when V_G equals V_{DS} . Typical figures of merit taken for the transfer curve involve the ON/OFF ratio of the device, which is the ratio between the I_{DS} when the device is ON divided by I_{DS} when the device is OFF, the field-effect mobility, $\mu_{FE} = \frac{Lg_{mt}}{WC_GV_{DS}}$, where L is the channel length, W the width, C_G the gate capacitance per unit area (in planar structures estimated from a plate capacitor model of the gate), the transistor gain, $G = g_{mt}/g_{DS}$, where g_{DS} is the conductance of the channel, and the sub-threshold swing (SS) defined as the necessary change in gate bias for an increase in current of one order of magnitude, $\frac{\partial V_{GS}}{\partial(\log I_{DS})}$.

The output characteristic shows how I_{DS} depends with V_{DS} for several V_G . For a given V_G , as V_{DS} increases, I_{DS} will increase linearly. But as V_{DS} increases, field-effect induced charge density below the drain contact reduces due to a lower V_{DG} difference, leading to a non-linear dependence of I_{DS} with V_{DS} (shoulder in Figure 2.4 c)). At some point, this drain-induced depletion below the contact will balance the inversion layer and reduce the induced charge density to 0. This point is known as the pinch-off point. For even further increasing V_{DS} , the pinch-off point will move in the channel to closer to the source contact with I_{DS} saturated.

2.1.3.2 Interface states

One detrimental condition for the performance of field-effect transistors emerges from problems in setting up ideal versions of its building blocks, the metal/semiconductor junction and the metal/insulator/semiconductor capacitor [6].

Interface states are electron states localized close to the surface with energy inside the band gap of the semiconductor material. Impurities and defects can also generate states inside the band gap, but they tend to be distributed along the bulk of the material as well. Surface states, which exist only at the surface of the material, are generated from the interruption of the crystal lattice, due to the breaking of the translational symmetry. Another type of surface states can be induced by proximity to another material. Surface states are usually referred to as simply interface states. Figure 2.5 summarizes the effects of the additional interface states in a metal/semiconductor junction.

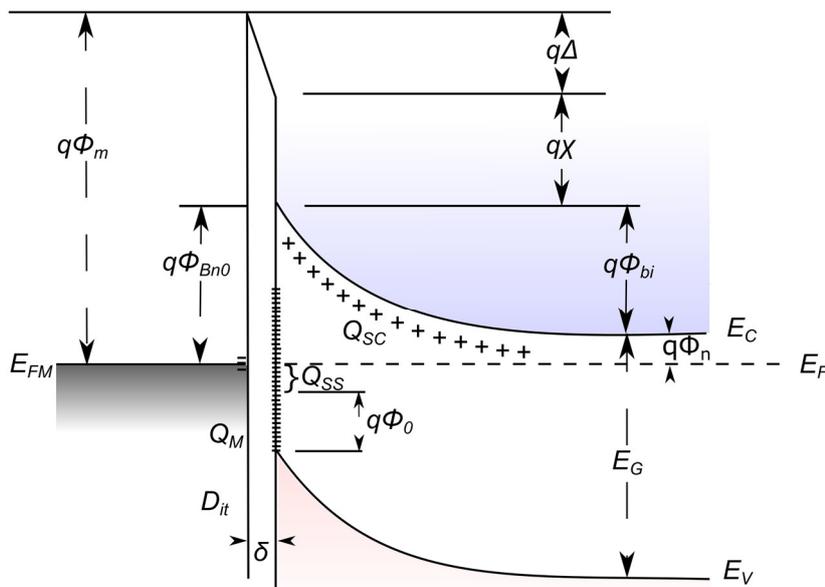


Figure 2.5 Energy diagram of a metal/(n-type)semiconductor junction with contribution from interface states at the semiconductor surface. Above the neutral level of the interface states, $q\phi_0$, the accumulated interface-trap charge density, Q_{SS} , is negative (below Fermi level, and above $q\phi_0$). The balance of the charges induced in the metal, Q_M , the charges at the semiconductor Q_{SC} , and the surface states Q_{SS} , will lead to an interface dipole measured by the quantity $q\Delta$. If the density of trap states D_{it} is larger than the DOS of the metal, the metal's Fermi level E_{FM} position will be pinned at the semiconductors Fermi level.

Working in similar fashion to impurities, interface states can be donor or acceptor levels. Donor levels are neutral if filled and positively charged when empty. Acceptor levels are neutral if empty and negatively charged when filled. In thermal equilibrium, the Fermi level is constant throughout a material, and while at the bulk these states do not exist and therefore do not have to be filled, close to the surface, these states will be filled as well. Since the number of electrons in the system is fixed, the additional charging at the surface will decrease the available electrons in the conduction band. This characteristic spatial distribution leads to depletion of electrons close to the surface of the material, and therefore to the band bending. Interface states greatly affect the performance of metal/semiconductor junctions, and of MIS capacitors.

When a metal surface is brought in contact with the semiconductor, the presence of these interface states can result in two limiting cases. If the density of interface states is much larger than the DOS of the metal, then the barrier height of the metal/semiconductor contact will be entirely determined by the semiconductor material band gap and charge neutrality point, being independent of the metal's work function. In this regime, the metal contact is said to be pinned by the semiconductor (Fermi level pinning). In the ideal case, where there are no interface states, then the barrier height should entirely depend solely on the metals work function and semiconductors' electron affinity.

For MIS capacitors, interface states in the band gap of the semiconductor and localized in the insulator will trap electrons of the semiconductor channel in the insulator. This charging effect will lead to screening of the field-effect induced in the semiconductor channel by means of the applied gate bias. Since the trapping process is an active process, the states will be occupied and unoccupied with characteristic lifetimes, leading to fluctuations of the semiconductor channel resistance.

Ultimately, interface states can affect the contact energy barrier, the capacitance of the gate, and lead to transient effects and fluctuations of the channel resistivity.

2.1.3.3 Noise in field-effect transistors

Current fluctuations are ubiquitous in electronic systems [67], [113]. In FETs, they can be classified into four types: thermal or Johnson noise, shot noise, generation-recombination noise, and $1/f$ noise. Thermal and shot noise originates from the random

motion of charge carriers, although shot noise is only seen in systems with extremely low density of states. Generation-recombination noise comes from populating and depopulating processes of trapping states with characteristic lifetime τ and Lorentzian power spectral density (PSD). One of the origins of $1/f$ noise in FETs is the superposition of individual generation-recombination noise sources distributed along a lifetime range, which results in the characteristic $1/f$ -type PSD. Figure 2.6 depicts how the interface states localized in the insulator of a MOSFET, in contact with the semiconductor layer, lead to individual generation-recombination sources of noise and how their superposition results in $1/f$ -type noise. Interface states on contacts and impurities on the surface of the channel can also lead to similar fluctuations.

Although the current fluctuations are more pronounced for the lowest frequency of energy excitation, commonly referred to as low-frequency noise (LFN), these frequency levels up-converts to higher frequencies due to the non-linearity of the building blocks used in the electronic systems. When at the nanometer scale, these noise levels can be enhanced and deteriorate the electronic performance of the devices.

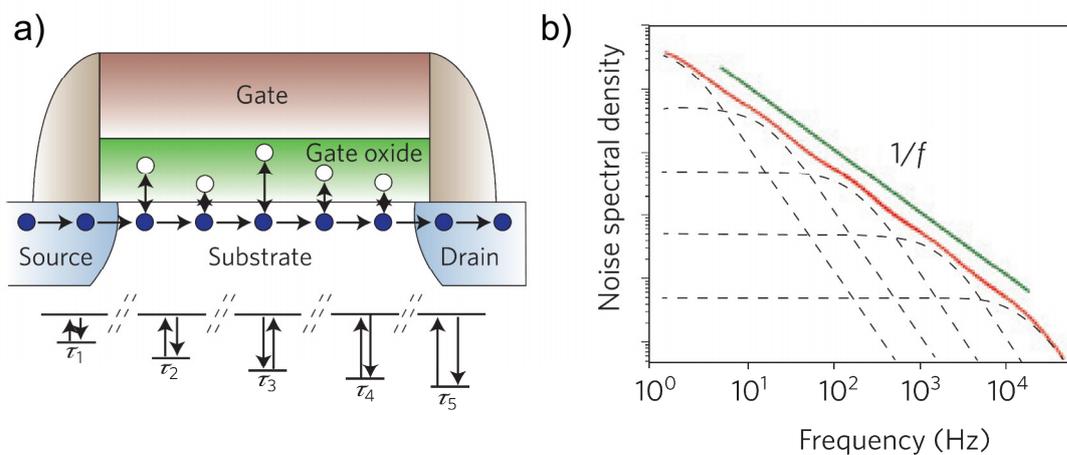


Figure 2.6 a) Cross-section of a field-effect transistor with top gate. The presence of trap states localized in the insulator (gate oxide) with different lifetimes results in fluctuations of generation-recombination character. b) Individually, each trap state has a Lorentzian power spectral density. The effect of several generation-recombination sources can lead to $1/f$ -type power spectral density. Figures a) and b) are adapted from Ref. [67].

From a Drude's model construction of the electrical current, one can identify two mechanisms for $1/f$ -type fluctuations of current: via changes in the carrier concentration, δn , or via fluctuations in mobility, $\delta\mu$, conceptually expressed as $\delta I \propto$

$q\mu\delta n + qn\delta\mu$. Two models are commonly employed to study the power spectral density of current fluctuations in MOSFETs, which are the Hooge model [114] for mobility fluctuations, and the McWorther model [115] for carrier-number fluctuations. Both formulations are based on a power-law description of the dependence of the PSD with the frequency of the fluctuation, given by $S_I = \frac{\alpha I^2}{f^\beta}$, where $S_I(f) = \lim_{T \rightarrow \infty} \langle \frac{1}{T} \left| \int_0^T I(t) e^{-i2\pi f t} dt \right|^2 \rangle$, which is the average value of the square of the Fourier transform of the current time series, $I(t)$, α and β are characteristic parameters, and I the average current driving through the device. $1/f$ noise type fluctuations are described in this framework as the having β values between 0.5 and 1.5. The McWorther model considers that the mechanism driving the carrier-number fluctuations is the tunneling of electrons from the conducting channel to the traps in the gate oxide, affecting the carrier density of electrons in the channel. In this model, α shows a dependence with the conducting channels carrier concentration n given as $\alpha^{-1} \propto n^2$.

The Hooge model for mobility fluctuations is mainly based on fluctuations on the scattering processes of the channel, which at room temperature are mainly dominated by phonon scattering. In the Hooge model, α will show an inverse dependence with carrier density given as $\alpha^{-1} \propto n$.

Consequently, for materials with carrier concentrations of the order of the 10^{12} cm^{-2} , by using an external electrostatic doping source, it is possible to evaluate the mechanism of low-frequency noise by gating the material and evaluating the dependence of the Hooge parameters with n . This technique is useful for semiconducting and semi-metal 2D materials where the carrier densities lie in the 10^{12} - 10^{13} cm^{-2} range, and where by using common SiO_2 dielectric substrates it is possible to induce carrier concentrations of the same order. As a rule of thumb, current fluctuations based on the change in the number of electrons are common for less conductive systems as semiconductors, while fluctuations in mobility dominate in metallic systems.

2.2 Magnetoresistance effects and quantum transport in a 2DEG

Magnetoresistive effects refer to changes in the resistance of a material under the application of an external magnetic field. 2DEGs in particular exhibit a plethora of magnetoresistive effects. These effects can be due to semi-classical effects, as ordinary magnetoresistance, or be quantum in nature, as quantum Hall and weak (anti)-localization effects.

2.2.1 Quantum Hall effect

When a strong magnetic field is applied to a 2DEG, the cyclotron orbits of the charged carriers in the 2D plane become quantized [116], [117]. Cyclotron orbits are the resulting characteristic circular motion of a charged particle under a perpendicular magnetic field, with angular frequency $\omega_B = \frac{eB}{m_e}$ designated as Larmor frequency.

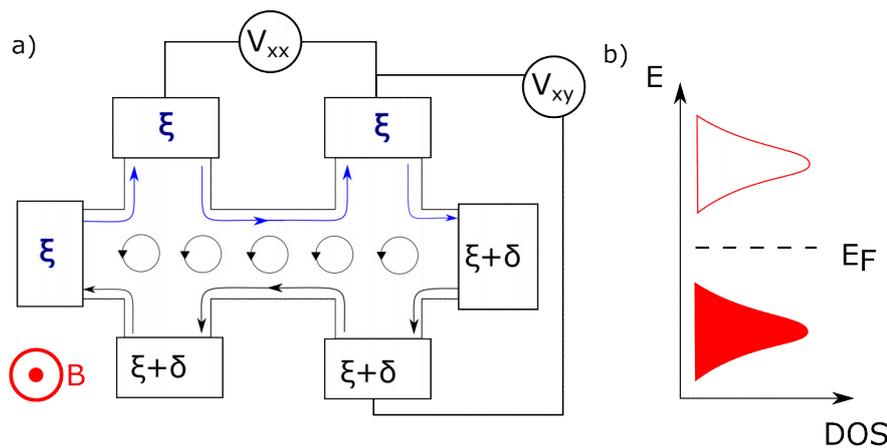


Figure 2.7 a) Non-dissipative edge transport in a Hall bar of a 2DEG resulting from the skipping cyclotron orbits at the edge of the conductor. In the quantum Hall regime, the non-dissipative transport of the electrons injected by electrodes 1 and 2 (blue and black) leads to $V_{xx} = 0$ and $V_{xy} = \delta$. b) Landau quantization of the energy of the cyclotron orbits for sufficiently high magnetic fields perpendicular to the 2DEG. The number of states increases with increasing magnetic field.

Figure 2.7 shows the case of a Hall bar of a 2DEG channel under an external magnetic field, with resulting cyclotron orbits, and skipping cyclotron orbits at the edge of the conductor, leading to a one-dimensional (1D) flow of non-dissipative charge carriers through the edge. In the classical Hall effect, charge carriers under a magnetic field build up a voltage drop at the edges of the conducting channel proportional to the

magnetic field applied perpendicular to the surface. Using Ohm's law and the tensor notation of the conductivity to summarize the effect, for a current being driven in the x -direction in a channel in the x - y plane, the transverse Hall resistivity is given by $\rho_{xy} = \frac{E_y}{J_x} = R_H B$, where R_H is the Hall coefficient, which is inversely proportional to the carrier density n , $R_H = \frac{1}{en}$. The linear relationship between the resistivity and B breaks down for sufficiently high magnetic fields, where the induced Landau level (LL) splitting leads to the emergence of transverse resistivity plateaus. Under a magnetic field, the energy levels of the cyclotron orbits become discrete, with energy value $E_j = \hbar\omega_B(j + \frac{1}{2})$, where j is an integer. Each energy level is highly degenerate, with degeneracy $N = g_s BA/\Phi_0$, where Φ_0 is the flux quantum given as h/e , and g_s is the spin degeneracy. The quantization of the cyclotron orbits has consequences for both ρ_{xx} and ρ_{xy} . When the chemical potential is between Landau levels the conductivity $\sigma_{xx} = 0$, which results in $\rho_{xx} = 0$ and $\rho_{xy} = \frac{1}{\sigma_{xy}} = \frac{h}{e^2} \frac{1}{\nu}$, where ν is an integer indexing the Landau level, also known as filling factor. The vanishing longitudinal resistivity is a consequence of the occupancy of the LL. Since the amount of energy an electron loses via inelastic scattering defines the longitudinal resistance, when after a scattering event there are no available states in the occupied LL and the thermal energy is not enough to access the next Landau level, scattering processes become forbidden, and the resistance drops to close to 0. The center of the plateau occurs for specific values of B , namely when $B = \frac{2\pi\hbar n}{ve} = \frac{n}{\nu} \Phi_0$. Figure 2.8 a) shows the first realization of the quantum Hall effect, demonstrated by von Klitzing in 1980, and Figure 2.8 b) the quantum Hall effect in graphene.

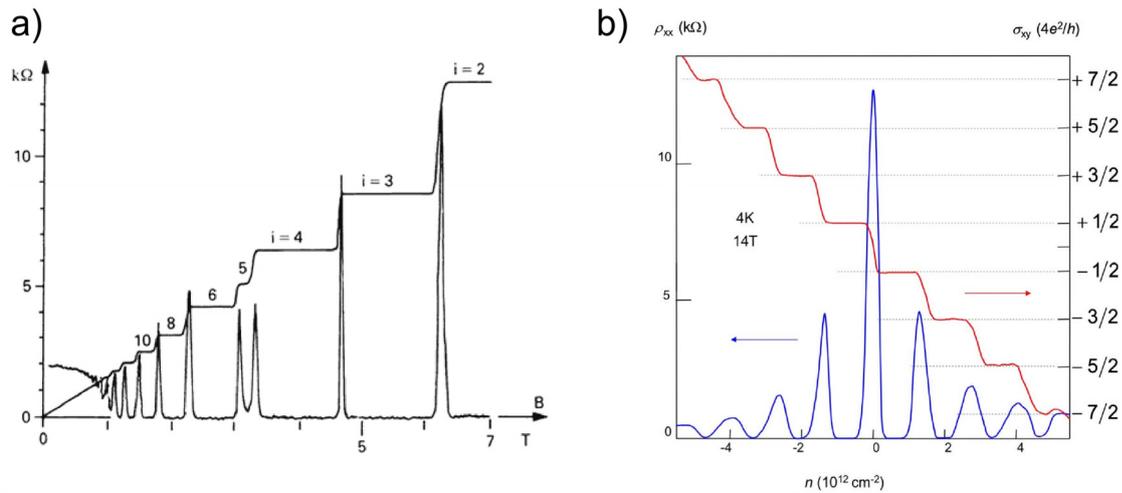


Figure 2.8 Quantum Hall Effect probed in two different ways. a) Integer QHE. Longitudinal and transversal resistance of a 2DEG as a function of the applied magnetic field for a fixed carrier density. b) Half-integer QHE. Longitudinal resistivity and transverse conductivity of graphene as a function of the carrier density for a fixed magnetic field. Figures a) and b) taken from Ref. [118] and from Ref. [16], respectively.

Graphene is a unique case of integer quantum Hall effect, usually referred to as an anomalous integer case [18], [119]. For graphene, $\sigma_{xy} = \pm 4(i + 1/2) \frac{e^2}{h}$, for $i = 0, 1, 2$, etc, without any plateau at the Dirac point. This particular case for graphene emerges from the topological nature of the graphene's electronic structure [18]. The particle-hole symmetry of graphene from the time-reversal invariance and the relativistic nature of the carriers due to the linear band dispersion lead to an odd function of the transversal conductivity σ_{xy} across the Dirac point. Simultaneously, graphene shows a robust zeroth LL at the Dirac point, where the energy of the LL does not change with magnetic field, unlike all others. The QHE plateaus are visible when the Fermi level is between Landau levels, jumping by an amount proportional to $4 \frac{e^2}{h}$ when crossing the LL. Moving the Fermi level (via gate bias) through the LL pinned at the DP, will not show a plateau, with the first σ_{xy} plateau for electrons and holes emerging only at $\pm 2 \frac{e^2}{h}$, respectively (with total change $4 \frac{e^2}{h}$). These conditions result in the “half-integer” expression determined for the quantization of σ_{xy} .

2.2.2 Weak (anti)-localization

Weak localization effects emerge in disordered conductive thin films at low temperatures [107]. The constructive interference of time-reversed back-scattered electrons in disordered metals leads to positive corrections to the resistivity of the channel, referred to as weak-localization. Applying a magnetic field perpendicular to the time-reversed paths destroys the interference and leads to an increase in conductivity. In systems with strong SOI, the effect is reversed and leads to negative corrections of the resistivity, also known as weak anti-localization. Applying a magnetic field disrupts the interference effects and consequently to the decrease in conductivity. Both effects are captured by the theory of Hikami, Larkin and Nagaoka (HLN) for the magnetoconductance of thin films, where $\Delta\sigma_{\square}(B) = \sigma_{\square}(B) - \sigma_{\square}(0) = \frac{R_{\square}(0) - R_{\square}(B)}{R_{\square}(0)R_{\square}(B)}$, is defined as the magnetoconductance, and R_{\square} is the sheet resistance. According to HLN,

$$\Delta\sigma_{\square}(B) = -\frac{e^2}{2\pi^2\hbar} \left[f\left(\frac{B_1}{B}\right) - \frac{3}{2}f\left(\frac{B_2}{B}\right) + \frac{1}{2}f\left(\frac{B_{\phi}}{B}\right) \right] \quad (8)$$

with $f(x) = \psi\left(x + \frac{1}{2}\right) - \ln(x)$, being $\psi(x)$ the digamma function, and B_1, B_2 and B_{ϕ} the characteristic magnetic fields, defined as $B_1 = B_e + B_{s.o.} + B_s$, $B_2 = B_i + \frac{4}{3}B_{s.o.} + \frac{2}{3}B_s$ and $B_{\phi} = B_i + 2B_s$, where (e) corresponds to the elastic, (i) inelastic, (s.o.) spin-orbit and (s) magnetic scattering mechanisms. The characteristic magnetic fields can be converted into the respective relaxation lengths using $l_i = \sqrt{\hbar/4eB_i}$, where $l_i = \sqrt{D\tau_i}$ and $B_i = \hbar/(4eD\tau_i)$.

Figure 2.9 shows the concept behind the construction of the weak localization theory, and the demonstration on Mg devices alloyed with Au to introduce SOC.

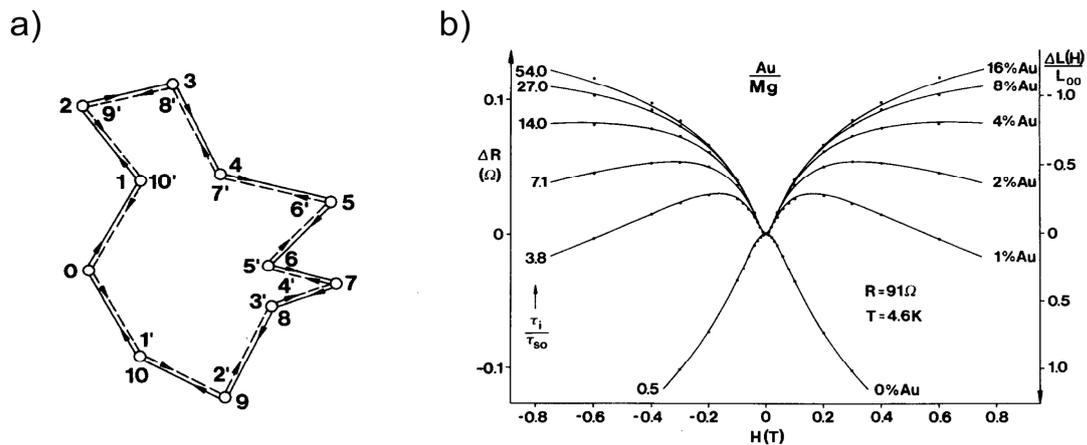


Figure 2.9 a) Scattering path of electrons in a disordered metal. Both the non-time reversed and time-reversed propagations directions of the electrons are represented, leading to a finite probability of an electron reaching its starting point, and each path interfering with each other. b) Change in resistance of Mg films under an external applied magnetic field. Weak-localization crossover to weak anti-localization with increasing concentration of Au. Figures adapted from Ref. [107].

Weak localization techniques are then useful to extract information about the relaxation lifetimes, namely of spin-orbit scattering mechanisms. Since spin-flip events are associated with spin-orbit scattering rates, weak-localization can be used to infer on the spin relaxation length of a material. Studying its dependence with the conductivity of a channel can help clarifying if the scattering events are of Dyakonov-Perel [120] or Elliot-Yafet type [121].

2.3 Nonlocality in the spin Hall regime

2.3.1 Spin Hall effect and its inverse

The spin Hall effect resembles regular Hall effect, where charges of opposite sign flowing in the same direction accumulate at opposite edges of a conducting channel (under an external applied magnetic field) [95]. In the spin Hall effect, this description changes slightly to “spin states of opposite sign flowing in the same direction accumulate at opposite edges of a conducting channel” (this time without any external magnetic field).

The original formulation of the spin Hall effect was developed by Dyakonov and Perel in 1971 [91], [92], further extended by Hirsch in 1999 [122], observed in 2004 for GaAs semiconducting stripes [93], and demonstrated electrically in Al in 2006 by Valenzuela [94]. In materials with strong SOC, the current-induced spin accumulation is driven by an asymmetric scattering of the spin of the charge carriers with the SOC centers. Two important figures of merits for assessing the efficiency of the SHE are the spin Hall conductivity and the spin Hall angle. The spin Hall conductivity is defined as $\sigma_{SH} \equiv -\frac{J_{s,y}}{E_x}$, where $J_{s,y}$ stands for the pure spin current density, J_s , generated in the y -direction for an electric field E applied along the x -direction, with $J_s = J^\uparrow - J^\downarrow$, where $J^{\uparrow,\downarrow}$ are the current density for spin-up and spin-down. The spin Hall angle $\theta_{SH} \equiv \frac{J_{s,y}}{J_x}$ quantifies how much of the charge current is converted into spin current. Platinum is currently the material which holds the largest spin Hall angle, with charge-to-spin conversion efficiencies of 20% [123].

Figure 2.10 a) and b) sketch the implementation of a non-local injection and detection strategy based on the spin injection by a ferromagnetic electrode and the detection of the spin current by SHE. Once in the non-magnetic channel, the spin polarized current will diffuse isotropically along the channel. Spins of opposite sign will accumulate at different edges, and due to the imbalance of spins, a spin Hall voltage, V_{SH} , will be detected between the voltage reading terminals V_{SH+} and V_{SH-} . Sweeping the magnetization with an external magnetic field would allow for the manipulation of the spin orientation and to the modulation of V_{SH} .

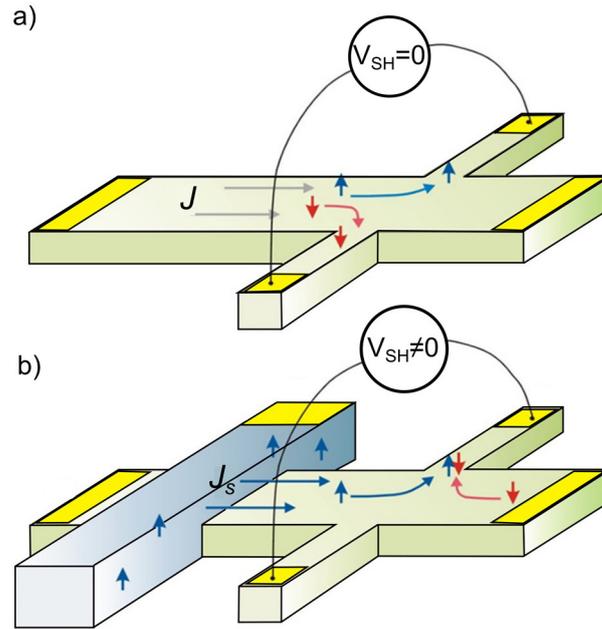


Figure 2.10 a) Spin accumulation at the edges of a conductor with strong SOC induced via SHE without resulting in a net transverse voltage. b) Device concept for the manipulation and detection of spins via SHE. By injecting a spin polarized current with a ferromagnetic electrode (blue bar), the accumulation of opposite spins on opposite edges will be uneven, leading to a net voltage. Figures adapted from Ref. [124].

Studying the dependence of the spin Hall resistance, $R_{SH} = V_{SH}/I$, with the channel length, L , could be used to infer on the spin diffusion length λ_s via the relation $\Delta R_{SH} = \frac{P}{t} \frac{\sigma_{SH}}{\sigma_c^2} \exp(-L/\lambda_s)$, where $\Delta R_{SH} = \max(R_{SH}^{+B}) - \max(R_{SH}^{-B})$, P is the spin polarization, given as $\frac{G^\uparrow - G^\downarrow}{G^\uparrow + G^\downarrow}$, where $G^{\uparrow,\downarrow}$ are the tunnel conductance's for spin-up and down, σ_c is the channel charge conductance, and t the thickness.

Abanin *et. al.* extended the construction of the signal emerging either from SHE or ISHE to the cases where both SHE and ISHE were used to generate and detect spin current with a single non-magnetic material [96]. This construction would latter lead to the non-local strategies employed to study spin transport without the use of ferromagnetic leads. Figure 2.11 shows the construction of non-local signals mediated by the spin diffusion in the spin Hall effect regime.

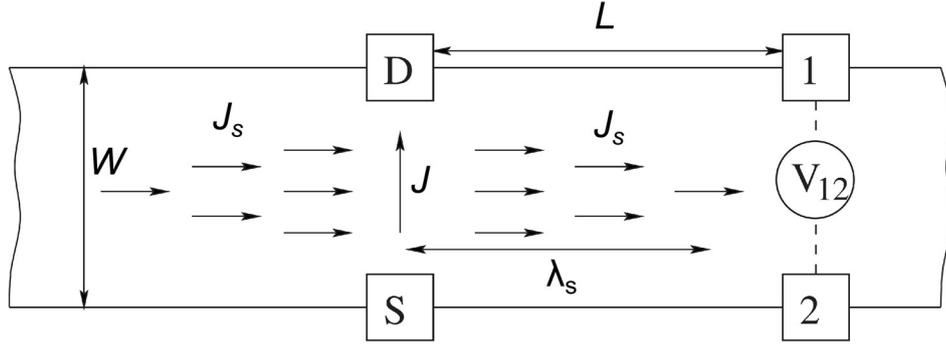


Figure 2.11 Slab of a conducting material with strong spin-orbit coupling, where by injecting a charge current, J , between drain (D) and source (S) terminals, a spin current, J_s , is generated transverse to the charge current via spin Hall effect. The spin current decoheres with distance, and a voltage difference is detected at the terminals 1 and 2 from the conversion of the J_s to a charge current via inverse-spin Hall effect. Figure taken from reference [96].

In this framework, the non-local resistance would be determined from the expression $R_{NL} = I_{DS}/V_{12}$, and the dependence of its magnitude with the distance between electrodes related by the expression,

$$R_{NL} = \frac{1}{2} \theta_{SH}^2 \rho \frac{W}{\lambda_s} \exp(-L/\lambda_s), \quad (9)$$

where θ_{SH} is the spin Hall angle, ρ the channel resistivity, and λ_s the spin relaxation length.

Manipulating the spins with an external magnetic field applied parallel to the channel's surface and parallel to the direction of the injected current leads to a Hanle-like dependence of the non-local signal, given by

$$R_{NL} = \frac{1}{2} \theta_{SH}^2 \rho W \operatorname{Re}[(\sqrt{1 + iw_B \tau_s / \lambda_s}) \exp(-\sqrt{1 + iw_B \tau_s / \lambda_s}) L]. \quad (10)$$

Abanin *et al.* applied this model of the non-local detection of spin diffusion mediated by SHE and ISHE to a particular case of materials with linear dispersion relationships, where even in the absence of SOC, a strong magnetic field would lead to similar spin Hall generation and detection of spin currents.

2.3.2 Zeeman spin Hall effect

The Zeeman spin Hall effect occurs in graphene-like systems [97]. While far away from the charge neutrality point, the Hall resistivity is given by the classical $\rho_{xy}(n) = -\frac{B}{ne}$, close to the charge neutrality point the coexistence of both types of charge carriers smears down the transverse resistivity, leading to dependence shown in the inset of Figure 2.12 a). Applying an external magnetic field perpendicular to the graphene sheet lifts the spin degeneracy via Zeeman interaction and imbalances the Hall resistivity of the different spin species. Due to the large $\frac{\partial \rho_{xy}}{\partial n}$ close to the Dirac point the large difference between the Hall resistivity for each spin will result in a strong spin Hall response.

Figure 2.12 shows the expected spin Hall coefficient as a function of the carrier density for several temperatures at an applied magnetic field of 1 T in graphene, and the principles of operation for the non-local determination of spin-signals generated from the SHE and ISHE in a graphene H-bar.

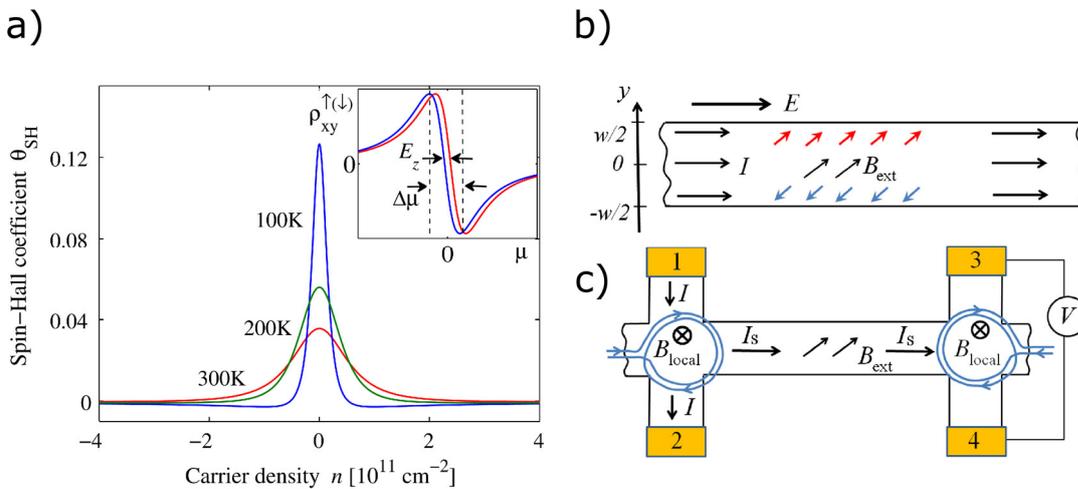


Figure 2.12 a) Spin Hall coefficient as a function of carrier density under a given applied external magnetic field $B = 1$ T for different temperatures. E_z refers to the Zeeman splitting. Inset: transverse resistivity for each spin species with applied magnetic field. b) Accumulation of spins at the edges of a graphene nanoribbon. c) H-bar strategy for the injection of a pure spin current transverse to the injection direction (contacts 1 and 2) and detection at the two other terminals (3 and 4). The blue lines on Figure c) represent coils generating a local magnetic field to enable the generation and detection of spins. Figures taken from Ref. [97].

For the determination of an equivalent spin Hall angle, Abanin's model considers a uniform channel carrying a current I , and the transverse gradients of the electrochemical potentials, μ , for each spin species as

$$\nabla_y \left(\phi + \frac{n_\uparrow}{ev_\uparrow} \right) = \frac{\rho_{xy}^\uparrow}{\rho_{xx}^\uparrow} E, \text{ and } \nabla_y \left(\phi + \frac{n_\downarrow}{ev_\downarrow} \right) = \frac{\rho_{xy}^\downarrow}{\rho_{xx}^\downarrow} E,$$

where $n^{\uparrow,\downarrow}$ and $v^{\uparrow,\downarrow}$ are the spin-up and down concentration and density of states, respectively, ϕ the electric potential, and E the electric field along the x -direction (see Figure 2.12 b)). The spin accumulation at the edges of the ribbon $n_s = n_\uparrow - n_\downarrow$ is determined to be

$$n_s = \frac{\theta_{SH} w e E}{v_\uparrow^{-1} + v_\downarrow^{-1}},$$

with the spin Hall coefficient being defined as $\theta_{SH} \equiv \frac{\rho_{xy}^\uparrow}{\rho_{xx}^\uparrow} - \frac{\rho_{xy}^\downarrow}{\rho_{xx}^\downarrow} \approx E_Z \frac{\partial \rho_{xy}}{\partial \mu \rho_{xx}}$, where E_Z stands for the Zeeman energy. Stronger magnetic fields lead then to a larger θ_{SH} at the Dirac point. By studying the dependence of the non-local signal at the Dirac point in graphene with the external magnetic field, and evaluating it versus other possible sources of non-local signals, as the van der Pauw Ohmic contribution, it would be possible to pin-point the spin origin of the signal.

The full derivation of the dependence of the spin Hall coefficient with the magnitude of the magnetic field and temperature can be found in reference [97]. Interestingly, the same theoretical framework developed for the spin diffusion in the spin Hall regime can be used here to evaluate the dependence of the non-local signal with the distance between electrodes, and also for the Hanle precession.

Chapter 3

Experimental techniques

Here we introduce the fabrication and characterization techniques followed to produce and study the devices in this thesis. Combining the techniques described in this chapter we fabricate MoS₂ field-effect transistors (FETs) (chapter 4), ambipolar WSe₂ FETs on BN substrates (chapter 5), macro- and microscale Hall bars of chemical vapor deposition (CVD) graphene (chapter 6), organic field-effect transistors using graphene electrodes (chapter 7), and lateral metal/insulator/graphene diodes (chapter 8). On each respective chapter, the process flow, electrical measurement setup, and characterization will be specified for each device type.

3.1 Fabrication of devices using 2D vdW materials

Fabricating devices with 2D materials still relies on two fundamental steps: their growth (or isolation), and transfer. 2D materials differ from common materials used in CMOS technologies in the sense that they cannot be directly grown over a wide range of substrates, as you can do with thermal and e-beam evaporation approaches used for metals, semiconductors, and oxides. This need for a transfer procedure is at the root of many of the problems with 2D materials. Growth via precipitation techniques as CVD has been established for graphene, BN [125], MoS₂ [126], WSe₂ [127], and most of the TMDs [128]. However, for proof-of-concept and fundamental studies, the most common isolation technique relies on the micromechanical cleavage of either natural crystals extracted in mines (MoS₂) [129], bi-products of the production of steel (Kish graphite) [130], or crystals produced from liquid-solid processes as the Czochralski, Bridgman, and Verneuil methods.

Micromechanical cleavage techniques are usually referred to as exfoliation approaches. The first exfoliation technique used Scotch-tape to peel off mono-to-few

layers of vdW crystals [14]. The transfer of the cleaved flakes from the tape surface to the desired substrate was done by pressing the tape against the surface. These techniques have been refined to overcome the leftovers of polymeric residues and environment exposure. Some earned the name of the groups that developed it, as the *Manchester technique* [131], or the polymer used, as *polydimethylsiloxane (PDMS) stamping* [132], and *Scotch tape* [14].

3.1.1 Transfer procedures

3.1.1.1 Exfoliation

In this thesis, we follow two approaches for the isolation and transfer of flakes onto a substrate: Blue tape and PDMS stamping [132]. Figure 3.1 summarizes the exfoliation procedure for both cases. The vdW crystals used were acquired from commercially available suppliers: MoS₂ from SPI supplies [129], the WSe₂ and BN from HQgraphene [133].

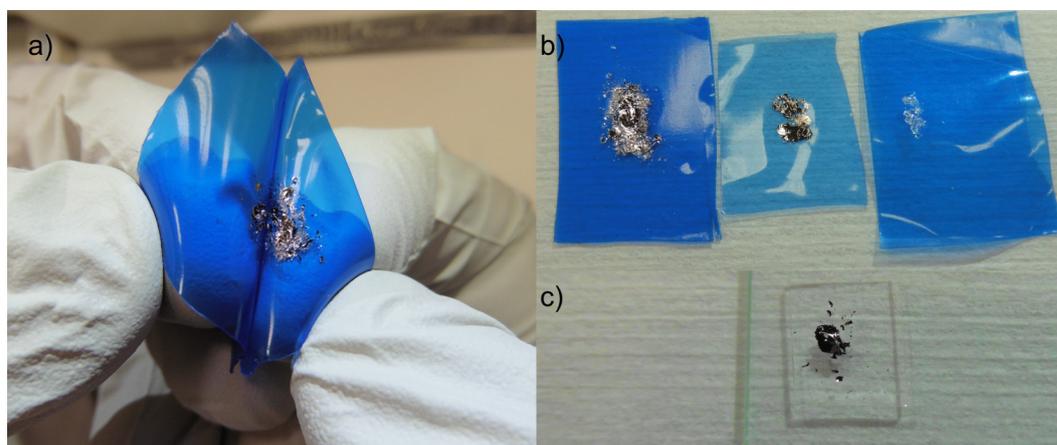


Figure 3.1 Images of the exfoliation of 2D vdW crystals. a) Blue tape-on-tape exfoliation of the flakes from the material supply tape onto a fresh tape. b) From left to right: material supply of MoS₂, WSe₂, and BN. c) Exfoliation of the fresh blue tape flakes on a PDMS stamp attached to a microscope slide.

Blue tape is a direct variant of the Scotch tape. It differs on the tape quality, Nitto SPV 224P [134], which is known to leave less polymeric residues on surfaces [135]. The initial step of an exfoliation procedure is to generate a material supply. First, using a double-sided Scotch tape and defining a window of $0.5 \times 0.5 \text{ cm}^2$, thick chunks

of crystals cut from the original bulk are placed onto the tape. Then, using Blue tape, the crystals are pressed from the top and quickly peeled. This process is repeated for several pieces of Blue tape as desired, forming the material supply. To exfoliate the material on a desired substrate, we pick an individual clean and fresh Blue tape and press it against one of the Blue tapes stored as material supply (Figure 3.1 a)). The two are peeled again, cleaving the crystals sandwiched in between. The clean tape will now hopefully have mono-to-few layer crystals of the vdW material. The next step involves pressing the resulting Blue tape surface onto the substrate. Figure 3.2 shows the typical outcomes of transfer procedures onto SiO₂, with material leftovers accumulated underneath the flake with the shape of bubbles, wrinkles, and badly adhered regions.

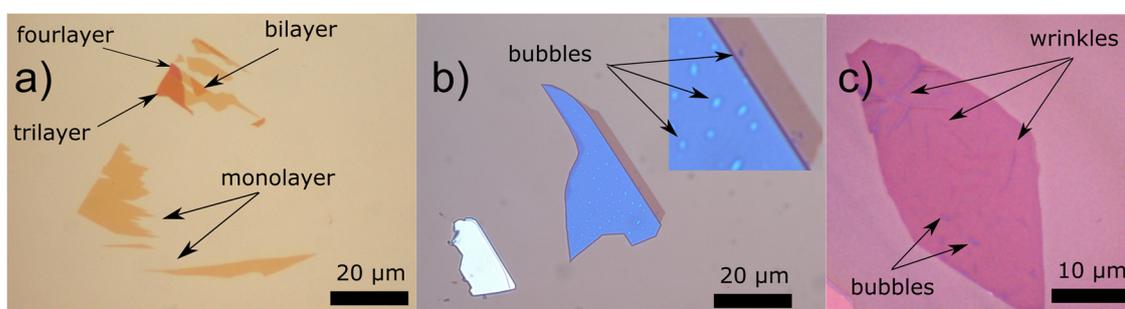


Figure 3.2 Optical microscope pictures of the Blue tape exfoliation of MoS₂ and WSe₂ on Si/SiO₂ (250 nm) substrates. a) MoS₂ flakes without visible defects. Mono-to-fourlayers. b) MoS₂ flake with bubbles clearly visible underneath the thicker bulk-like region (blue) and the monolayer. c) Wrinkles and bubbles after exfoliation of WSe₂.

Depending on the material and on the substrate, different conditions may be required for finally transferring the flakes. For TMDs and BN in particular we found that hard pressing seemed to be an efficient way to obtaining tens of micrometer-sized flakes, and that warming up the sample immediately before the exfoliation did not improve the results. The outcome of the exfoliation approach is random. Flakes will be transferred aleatory on the surface of the substrate without any control over the distribution.

In the PDMS stamping approach, instead of transferring onto a substrate, we add an additional step of exfoliating the fresh Blue tape on a PDMS stamp, placed at the edge of a microscopic slide (Figure 3.1 c)). This microscope slide and stamp will be incorporated with a deterministic setup allowing for the selective transferring of the flakes in the next section.

Most important, the surfaces transferred onto have been also prepared previously, usually via acetone/isopropanol (IPA)/ de-ionized water (DI) sonication, drying with nitrogen flow, and then placing them in a hotplate for a few minutes at temperatures above 100 °C.

In device structures that require the careful placement of flakes onto each other, as is the case of vdW heterostructures, it is not sufficient to rely on blue tape exfoliation. For the placement of a desired flake with micrometer control, deterministic transferring techniques based on PMDS (transparent viscoelastic polymer) have been developed to overcome this technical shortcoming.

3.1.1.2 Deterministic dry transfer

Polydimethylsiloxane (PDMS) stamping relies on the viscoelasticity and transparency of the polymer to enable the identification of mono-to-few-layers of the vdW materials and selectively transfer the chosen flake. The setup required for this transfer is more elaborate than the previous Scotch-tape-like method, while still relying on user-dependent, manual steps. Figure 3.3 shows the different elements necessary to make the deterministic all-dry transfer of 2D vdW flakes.

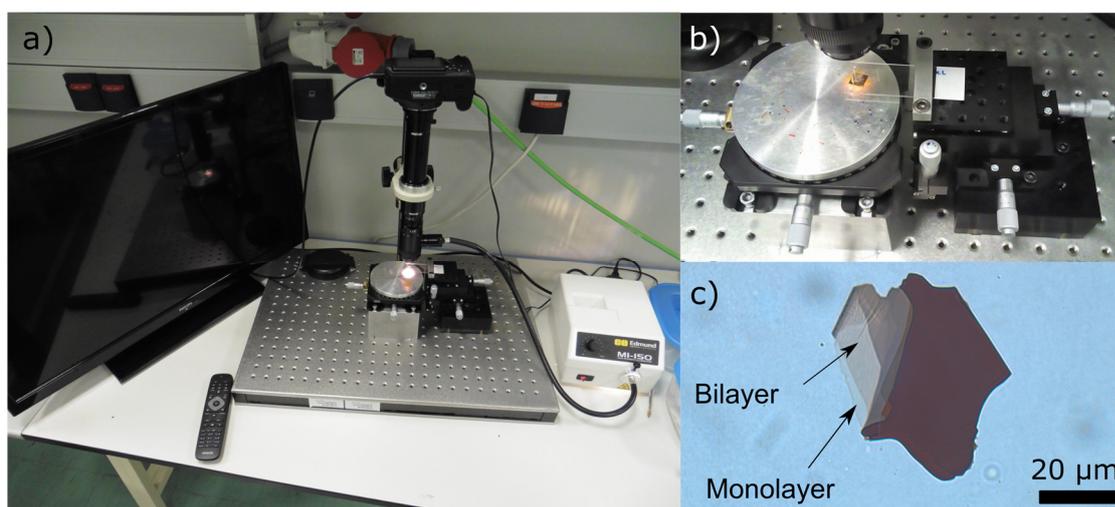


Figure 3.3 All-dry deterministic transfer setup for vdW flakes. a) Screen, stage, micromanipulator, camera, lens, light source. b) Detail of the micromanipulator with the microscope slide clamped, and positioned on top of a sample. c) WSe₂ flake on PDMS before transferring.

For the deterministic transfer one needs a material support (Blue tape, as before), PDMS, which can be fabricated in-lab or bought in a commercially available supplier (we opted for Sigma Aldrich [136]), a microscope slide, a micromanipulator with a campling system, a camera with a lens attached, with zooming and focus capability, an external light source, and a television screen. This setup allows for the transfer procedure to be monitored in-situ (Figure 3.3 a)).

The procedure goes as follows: first the material source is exfoliated with another piece of Blue tape to ensure the cleavage of clean, fresh flakes. A piece of PDMS is placed at the edge of the microscopic slide, the blue tape pressed onto the PDMS surface and peeled off quickly to cleave again the flakes (as seen in chapter 3.1.1). The flake leftovers in the PDMS surface will be inspected in a microscope using either transmission or reflection mode (Figure 3.3 c)). Thicker flakes will be clearly opaque to light, while thinner ones will gradually become more transparent, with a quite noticeable change for mono-to-few layers. In section 3.2, we will describe in more detail the use of material characterization techniques as Raman spectroscopy and atomic force microscopy employed to the flakes to confirm the thickness of the material. One of the convenient properties of TMDs is the large band gap, which results in strong absorption of light in the visible spectrum, depending strongly with layer number. A single monolayer of the TMDs explored in this work absorbs 5% of the incident optical light. In the early stages of our work, we matched the optical contrast and its variability to the determined thickness by Raman and AFM and concluded that the optical contrast could already provide enough evidence for the precise determination of the layer thickness, for layer thicknesses below or equal to 3.

Once the flake has been selected, the microscope slide is attached (clamped) to a micromanipulator that allows for x,y,z control of the position (Figure 3.3 b)). The substrate is attached to the stage with the help of a dual-sided adhesive and aligned with the stamp using the optics of the camera. Afterwards, using the large focus range of the camera setup, the flake is identified on the PDMS, and then by using the micromanipulator, the microscopic slide is moved down until it reaches the desired transfer area. The PDMS is pressed against the surface, and then slowly released, benefiting from the viscoelastic properties to ensure that the adhesion between the

polymer and the flake is reduced to a minimum, therefore allowing the flake to be released onto the surface.

Figure 3.4 shows the outcome of an all-dry deterministic transfer, pointing to defects found after transferring flakes or stacking them.

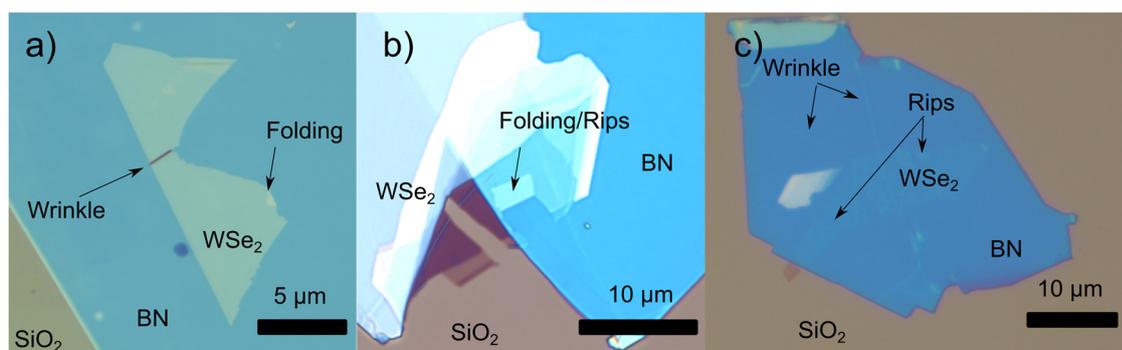


Figure 3.4 Optical microscope images of WSe₂ flakes transferred onto BN. a), b) and c) Typical outcomes observed on a vdW stack using PDMS stamping. Darker blue BN means thinner flakes. The contrast of WSe₂ depends strongly with BN thickness.

This deterministic technique allows for several flakes to be stacked vertically following an iterative procedure. This feature is useful for studying 2D vdW heterostructures. One limitation of this technique is the exposition of one side of the bottom vdW flake to polymeric residues from PDMS. PDMS residues are hardly removed by acetone and IPA baths, and are challenging to be removed. These residues will stay in-between layers and can limit the transport properties.

For proof of concept devices, there are alternative ultra-clean transfer procedures using vdW stacking, where polycarbonate (PC) coated PMDS stamps are used to encapsulate graphene or other TMDs in BN. This approach relies on the ability to pick-up and drop-down flakes from and onto an oxide substrate by warming up the oxide substrate [135]. With this pick-up technique it is possible to stack vertically up to 10 or more layers of different 2D vdW flakes [131], while encapsulating them in an ultra-clean dielectric environment.

While the presented exfoliation and transfer techniques enable the transfer of flakes, for the particular case of large area CVD grown materials, the procedure has to follow a different approach.

3.1.1.3 Wet transfer of CVD graphene

In the case of CVD graphene, the growth process of the material source rules out exfoliation techniques as the ones indicated above.

The CVD used in this thesis was acquired from a commercially available supplier, Graphenea S.A. [137], both in copper foils or already transferred on Si/SiO₂ (300 nm) 1x1 cm² chips. CVD graphene can be grown using precipitation techniques on transition metal elements, as nickel or copper [34]. The CVD graphene acquired was grown on Cu. Figure 3.5 shows a sketch of the wet graphene transfer from the copper foil onto the substrate.

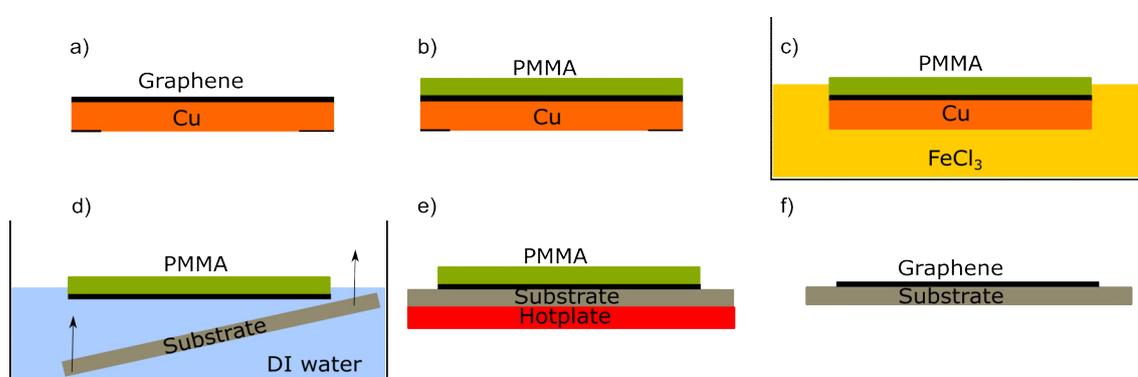


Figure 3.5 Sketch of the CVD graphene transfer from a copper foil. a) CVD growth of Gr on Cu. b) Spin coating of PMMA on top of graphene, followed by a removal of the backside graphene by oxygen plasma. c) Immersion of the stack in a strong copper etchant, as FeCl₃. d) Gr/PMMA stack in clean DI water to remove the leftovers of FeCl₃. Fishing procedure using a substrate. By tilting slightly the surface one can drag the Gr/PMMA stack from the water, with minimal water trapped in between. e) The stack is left drying over-night, and placed onto a hot plate at 180 °C for 30 mins. f) The PMMA film is finally stripped with acetone and IPA, finalizing the transfer procedure.

One of the positive remarks of the fishing approach is the possibility of transferring graphene into a large variety of surfaces. First, in order to detach the graphene from the copper foil, the active area of the foil is spin coated with poly(methyl methacrylate) (PMMA) (Figure 3.5 b)). Afterwards, the graphene grown on the backside edges of the copper foil is removed with oxygen plasma. The resulting Cu/Graphene/PMMA stack is then placed on a tin with FeCl₃ (Figure 3.5 c)), which is a strong etchant of Cu. The Gr/PMMA stack will be left floating in the etchant. The stack is then transferred from the tin into another one with DI water (Figure 3.5 d)), repeating this process several times until it's visibly free of contaminants. The Gr/PMMA will be

left floating in the DI water, with the Gr in contact with water. To *fish* the stack from the water, we used a substrate with dimensions larger than the floating Gr/PMMA stack. Notice the angle between the substrate and the stack. This technique ensures that the stack will adhere gradually to the surface, pushing off the water in between and leaving the minimal water trapped in between the substrate and the stack. The transferred layer is left drying at room temperature overnight, and then baked in a hot plate at 180 °C for 30 mins (Figure 3.5 e)). The PMMA covering the graphene is then finally stripped by dipping it in warm acetone for 10-15 mins (Figure 3.5 f)). Figure 3.6 shows the outcome of the wet transfer procedure of a CVD graphene foil onto 300 nm thick SiO₂.

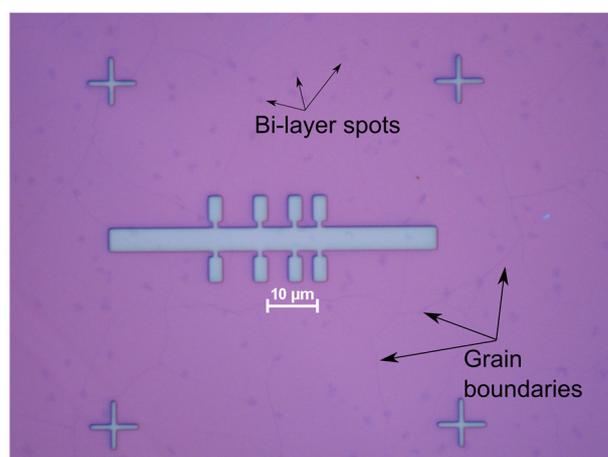


Figure 3.6 Optical microscope image of a continuous CVD graphene layer transferred onto SiO₂, with a DL PMMA Hall bar patterned by electron beam lithography. White scale bar of 10 μm. The dark spots in the picture are bilayer regions of graphene. The grain boundaries define graphene domains larger than 10 μm.

3.1.2 Lithography techniques

For the patterning of the resulting transferred flakes or CVD layer, two standard lithography techniques were employed: e-beam lithography and photolithography. Lithography is suited for nanometer scale devices and it is highly versatile for printing small-scale complex patterns. This technique is then suited for flakes. Photolithography on the other hand is suited for large-scale fabrication, matching with the parallel fabrication of many devices on large area films as CVD graphene.

3.1.2.1 Electron-beam lithography

The principle of e-beam lithography is the crosslinking of polymers known as *resists* when exposed to the impact of energetic electrons [138]. These crosslinked resists will then become sensitive or insensitive to specific chemistries that will allow them to be selectively dissolved, or *developed*. There are two types of resist image: positive or negative tones. Figure 3.7 shows examples of the two cases, and the outcome of their exposure to an e-beam and development with appropriate developer.

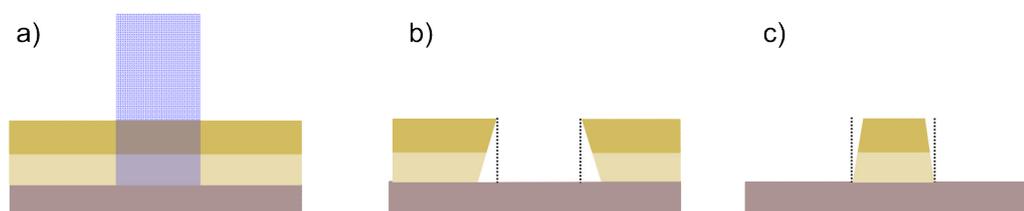


Figure 3.7 a) Sketch of the exposure of a double layer resist (light and dark brown) to an e-beam (light purple) according to its tone. b) Resulting profile after developing a positive resist, with associated undercut. c) Negative resist, with resulting overcut.

Positive resists are those whose exposed area becomes soluble by the developing agents (Figure 3.7 b)). Negative resists are those whose exposed area becomes insoluble to the developing agent (Figure 3.7 c)). Printing a pattern with a positive resist will result in a pattern in the shape of the *positive* of the pattern. Using a negative resist will result in a pattern in the shape of the *negative* of the pattern.

The electron-beam microscope works by focusing a beam of accelerated electrons (beam currents of pA to nA, depending on aperture) and exposing the desired area to a controlled charge density (dose), usually in the $\mu\text{C cm}^{-2}$ range. This value

depends on the resist thickness and weight of polymeric chain (measured in MDa). Since the designed features will be much larger than the area of focus of the beam, e-beam lithography works by rastering the design pixel-by-pixel, according to the dose desired and the size of the pixel. The time of write can be roughly estimated by dividing the total charge required to expose the surface and the beam current. The pixel size can be adjusted by the electromagnetic control of the electron-optics, which allows the size of the pixel to be changed.

The systems used in this work were the Raith150TWO and Raith e-Line Plus [139], [140]. Qualitatively, both systems have the same working principles, requiring a scanning electron microscopy (SEM) column, a pattern generator, and a laser interferometric stage. The SEM uses a filament to generate a cloud of electrons, which are then subjected to a voltage drop (of 10 kV in this work). The electron beam is guided by electromagnetic lenses along the column, leaving it through an aperture that controls the current flow (10 μm or 120 μm -wide, depending on the desired current flow). The column stands at a working distance (WD) of 10 mm of the surface of the sample. The pattern generator divides the designed structures into write-fields (WF, 100 μm or 1 mm-wide) from whose center the column is aligned and made expose by deflecting the e-beam in the necessary directions (rastering). In this thesis, we mainly worked with PMMA, which is a positive image resist, diluted in anisole. The EBL recipes used are shown in Table 3-1.

Table 3-1 Conditions followed for the preparation of devices using EBL. Process step flow from left to right. Processes related to empty columns are skipped.

R. I	Resist	Spin-coating	Baking	Exp. ($\mu\text{C cm}^{-2}$)	Dev.	LO
Pos. (DL)	PMMA 495	4k RPM, 0.2k	180 °C,	-	-	-
	A4	RPM/s, 60 s	90 s			
Pos.	PMMA 950	2.5k RPM, 1k	180 °C,	190	1:3 MIBK/IPA (IPA stopper)	Acetone
	A2	RPM/s, 60 s	90 s			
Pos.	ZEP	4k RPM, 1k RPM/s	180 °C, 240 s	80	ZEP520A	ZEP remover

R.I – Resist image; Pos. – Positive; Exp. – Exposure; Dev. – developer; DL – double layer; LO – lift-off; RPM – rotations per minute.

For the preparation of samples in our work, we would transfer the flakes or CVD graphene using the approaches discussed in 3.1.1, 3.1.1.2, and 3.1.1.3, and then

spin coat, expose, and develop the samples.

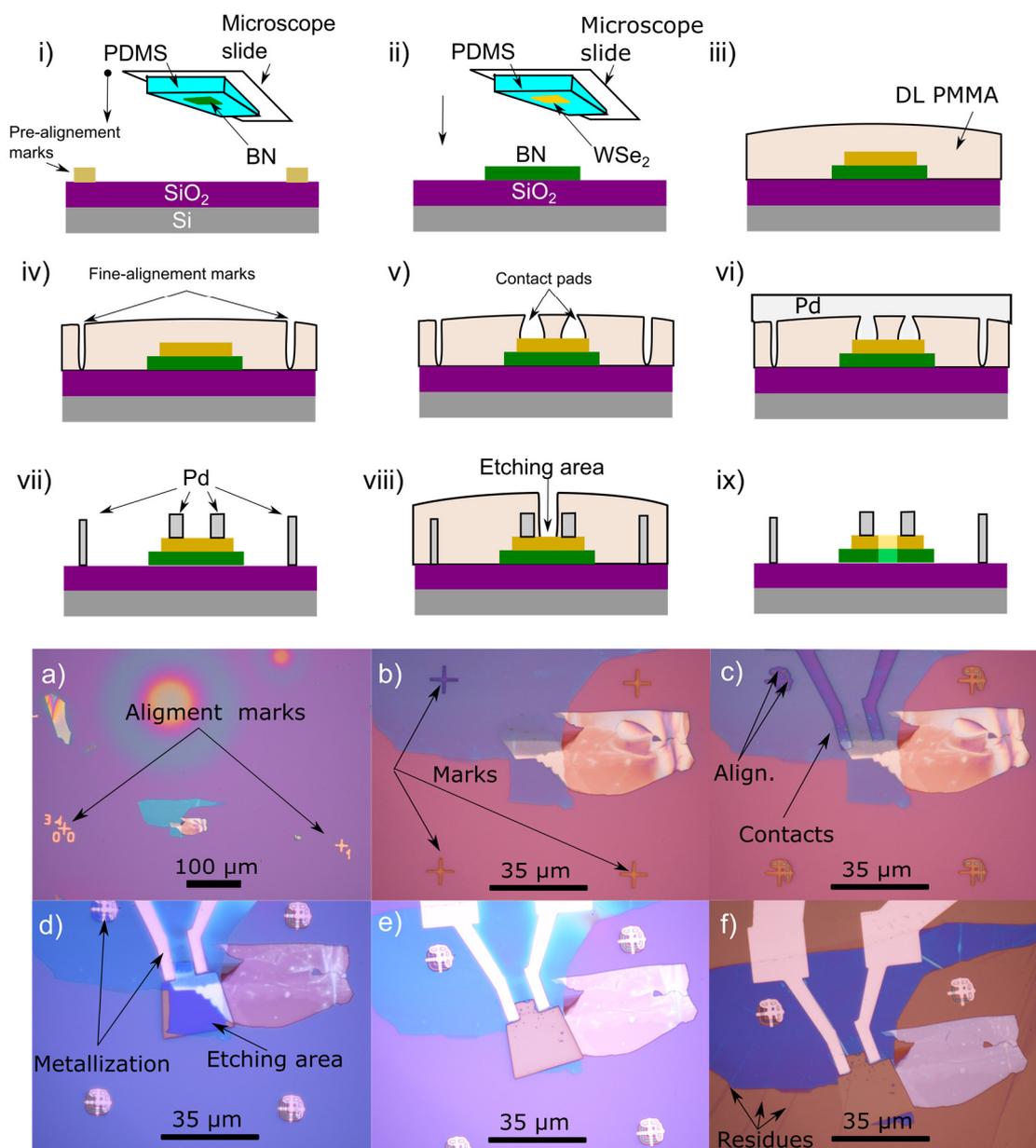


Figure 3.8 Scheme and optical microscope pictures of the EBL procedure followed for the preparation of a vdW stack of WSe₂ on BN. i), ii) Dry transfer of WSe₂ on BN. iii), iv) Spin coating, exposure and development of the fine-alignment markers. v), vi), Opening of metal contacts. vii) Device after lift-off. viii) Definition of etching area. ix) Final device. a) Determination of the flakes position using pre-patterned marks. b) Patterning of four fine alignment marks. c) Contact patterning using the marks to precisely align the position of the flake relative to the marks. d) Alignment of the etching area. e) Outcome of the etching procedure, still with the polymeric sacrificial layer. f) Result after stripping the resist with warm acetone.

The spin coating allows, via centrifugal forces, to spread a uniform layer of the polymer (resist) on the surface. The thickness of the resulting film will depend on the

rotations per minute and the process time.

The exposure via EBL defines the pattern, and the development removes the polymer from the undesired areas. This process would be integrated with the dry etching and metallization (chapter 3.1.4 and 3.1.5, respectively) to fabricate the devices. Figure 3.8 shows the scheme and optical microscope images of the typical procedure followed for the fabrication of a vdW stack of BN/WSe₂ contacted with Pd, which involves most of the procedures introduced in this chapter. Since the flakes were micrometer long, we used pre-patterned marks to localize them (Figure 3.8 a), i)). Using this rough alignment, we defined smaller marks on the resist around the flake (Figure 3.8 b), iv)). Using these marks one could use the highest magnification of the optical microscope to define the position of the flake with higher precision, as well as the structures to be patterned (Figure 3.8 b)). Using a specific software option of Raith, we could track the marks and precisely align the design to the position of the flake. Comparing Figure 3.8 b) and c) we can see the four marks with additional vertical and horizontal scans to determine the center of each, and expose based on the resulting alignment. To minimize the process time and maintain well defined and clean contacts on the flakes, we developed a two-step exposure process. The areas to be exposed were divided in two regions. One region 100 μm -wide around the flake, where we would perform a more controlled exposure of the resist, using 10 μm aperture (\sim pA current), 100 μm -wide WF, 10 mm WD and 10 kV of beam voltage; and a second area to bring the contacts further away from the sample to the final contact pads, onto which we would use cold-pressed indium to do the electrical wiring (chapter 3.2.1). For this second case we would use 120 μm apertures (\sim nA current), 1 mm-wide writing fields, 10 mm of WD and 10 kV of e-beam voltage. Developing the structures was done immersing the samples in a solution of 1:3 Methyl isobutyl ketone (MIBK)/IPA for 60 seconds. The stopping agent used was IPA. In case some additional etching was required, we would again use the same marks to align further layers (Figure 3.8 d)), and perform the etching (Figure 3.8 e), viii) and f), ix)).

3.1.2.2 Photolithography

Photolithography uses photons instead of electrons to crosslink photosensitive resists. Instead of rastering an electron beam, photolithography works by illuminating simultaneously the whole sample surface. By placing a mask with the desired design opaque to the ultra-violet (UV) light, the design can be printed into the photosensitive resist. This principle of operation allows for the preparation of large samples in minutes, which greatly enhances the output of the equipment. One clear limitation is the lack of versatility, as once a design is fixed it cannot be changed, requiring other masks for the purpose. The second limitation is the resolution of the features, bound by the diffraction limit of light's wavelength, which limits how close two structures can be defined. For micrometer resolved structures, masks are typically fused silica plates, transparent to UV light, with a chromium metal film deposited in the design regions (opaque to UV). Figure 3.9 shows the EVG 420 mask aligner used in this thesis, the mask with several layers for exposition of 2×2 cm² chips, and the image of the device fabricated for the study of metal/insulator/graphene lateral diodes, fabricated on Si/SiO₂ (300nm) (Figure 3.9 c)) and on sapphire (Figure 3.9 d)). Each chip has 200 devices.

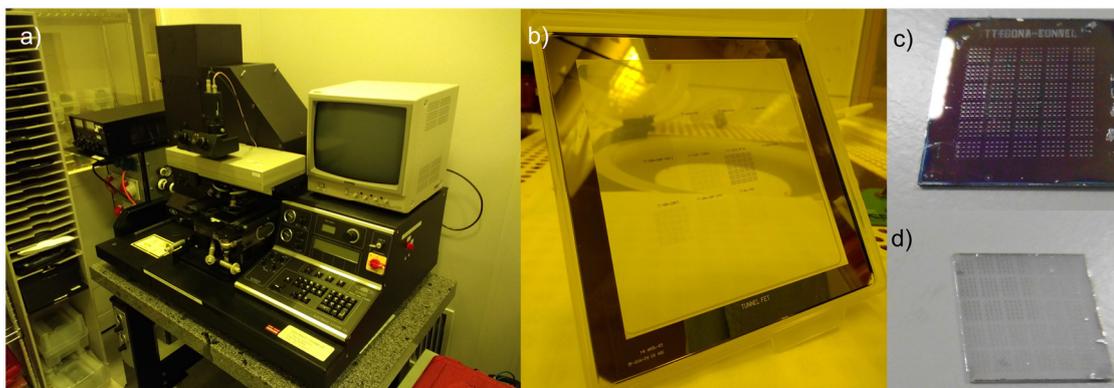


Figure 3.9 Image of the mask aligner setup used in this thesis. a) EVG 420 mask aligner. b) 15×15 cm² Fused silica mask, c) 2×2 cm² Si/SiO₂ chip with hundreds of devices fabricated onto it. d) 1.5×1.5 cm² sapphire substrate with hundreds of devices fabricated.

The equipment model used in this thesis was a semi-automatic EVG 420 6" mask-aligner (Figure 3.9 a)). The UV mercury arc lamp requires 350 W, and provides a 405-nm wavelength line (H-line). The total dose is controlled by setting the time of exposure, with constant power.

The principles of preparation of a photoresist layer are similar to the ones used for an EBL resist, but may require additional pre-bakes, post-exposure bake, and flood exposure steps. Resists as the AZ5124E are highly reactive to water, crosslinking when in contact. For this reason, the substrates require a pre-bake to remove water from the surface. AZ5124E in particular also has image-reversal properties. By submitting the sample to a post exposure-bake, the resist changes from a positive tone to a negative tone. Flooding is the exposure of the full area of the surface to UV. It is usually a non-critical step which helps with the reliability of the process. Figure 3.10 illustrates the steps followed during the photolithography using the image-reversal AZ5214E process as a template, and Table 3-2 details the recipes for the different photoresists used in this thesis.

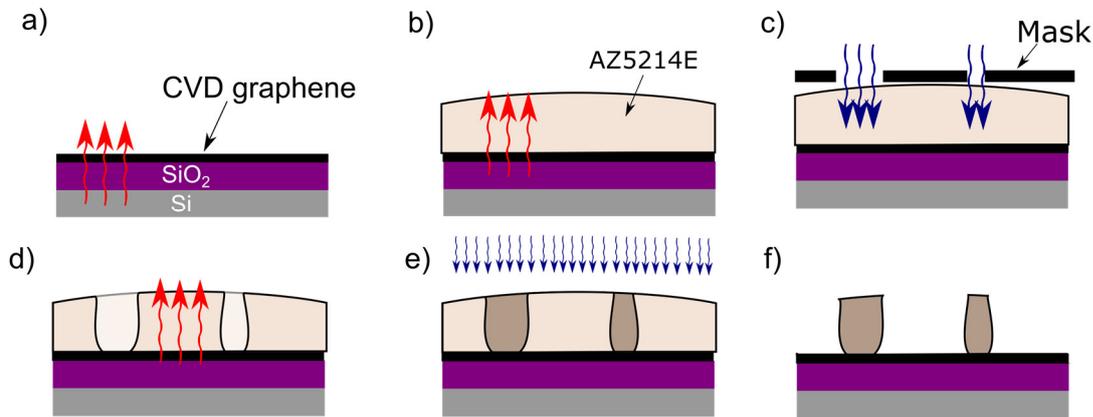


Figure 3.10 Image-reversal process of the AZ5214E resist. a) Pre-bake at 100 °C for 2 mins, to remove water at the surface. b) Spin coating at 3000 RPM for 35 s, and baking at 95 °C for 120 s. c) Exposure using hard contact-mode between the mask and the chip. At this stage the AZ5214E is still a positive image resist. d) Post-exposure bake, which inverts the image tone to negative. e) Flood exposure, without mask, of the whole chip. f) Development using AZ Developer for 8 s.

Table 3-2 Photolithography recipes for the different resists used. Process flow from left to right. Processes with dashes are skipped.

R. I	Res.	PB	SC	Bak.	Exp.	PEB	F	Dev.
Neg.	AZ5214E	100 °C	3k RPM	95 °C	7 s	115 °C	28 s	AZ Dev.
		120 s	35 s	120 s		60 s		8 s
Pos.	AZ5214E	100 °C	3k RPM	95 °C	7 s	-	-	AZ Dev.
		120 s	35 s	120 s		55 s		
Pos.	AZmir	100 °C	3.5k RPM	95 °C	16 s	110 °C	-	MF26A
	701	120 s	50 s	120 s		60 s		40 s
Neg.	LOR	100 °C	5.5k RPM	180 °C	-	-	-	-
		120 s	40 s	180 s				
(DL)	UVN30	-	3k RPM	110 °C	16 s	-	-	MF26A
			40 s	60 s				40 s

R.I – Resist image; PB – Pre-bake; SC – spin coating; Exp. – Exposure; PEB – Post-exposure bake; F. – Flood; Dev. – developer; DL – double layer; Note: all spin coatings done with 1000 RPM/s.

3.1.3 Atomic layer deposition

In the context of 2D vdW materials, atomic layer deposition (ALD) is usually employed to grow encapsulating layers of insulating materials, as HfO_2 , Al_2O_3 , and TiO_2 . Atomic layer deposition is a vapor phase thin-film technique that uses pulses of alternate gas species (precursors) to sequentially react on a surface, leading to the growth of the desired film. For compounds made of two distinct elements, a metal precursor is introduced and let adsorb on a surface. After a small period, the oxygen precursor is introduced (H_2O , or oxygen plasma) and given a time to react. The chamber is then purged with a flow of argon or nitrogen, and the cycle repeated. At the end of each cycle, a small layer of the film will be added to the surface of the material. Table 3-3 details the recipes used in this thesis with the Oxford FlexAL Plasma assisted ALD equipment.

Table 3-3 Recipes used for the growth of Al_2O_3 and TiO_2 .

Oxide	Reactant	Precursor	# Cycles	Stage T. (°C)	Thickness (nm)
Al_2O_3	H_2O	Trimethylaluminum	2000	150	40
TiO_2	O_2 plasma	Titanium tetrachloride	71	300	5.7
TiO_2	O_2 plasma	Titanium tetrachloride	25	300	1.7

T. – Temperature

The ALD films thicknesses were characterized using an M-2000 ellipsometer [141] calibrated with depositions of the materials on SiO_2 . The strong hydrophobicity due to the saturated in-plane bonds of 2D vdW materials, and the weak out-of-plane interactions make the ALD growth of thin, uniform, and conformal oxides on their surface a complex task.

3.1.4 Dry etching

Dry etching techniques are often employed to re-shape a material into a desired form. They are based on the generation of a highly energetic plasma of a specific gas mixture that can both chemically react and physically bombard a surface to remove the

target material [142]. In this thesis, the dry etching procedure is performed relying on polymeric sacrificial layers to select which areas to remove. Among the advantages of dry etching techniques are the low contamination, high anisotropy, selectivity, and the reliable etching of nanometer sized structures. For 2D vdW materials, flakes are often re-shaped to have a better control over the length and width of the channel, which are important geometrical parameters in order not to overestimate or underestimate electrical properties. Figure 3.11 shows typical outcomes of the dry etching of 2D materials using reactive ion-etching (RIE).

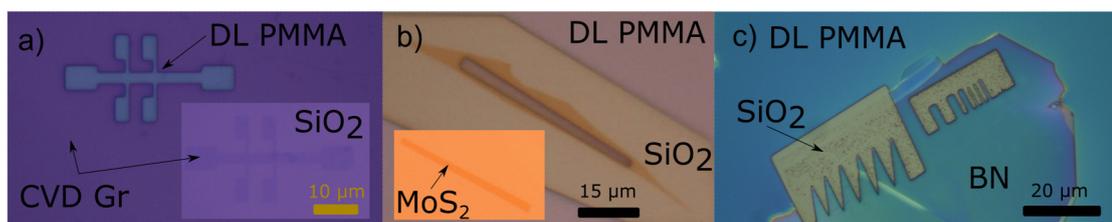


Figure 3.11 Optical microscope pictures of the outcome of reactive ion-etching procedures. a) CVD Gr Hall bar etched with Ar/O₂, b) Monolayer MoS₂ on SiO₂ etched with Ar:O₂, c) Bulk-like BN etched with SF₆:Ar. Table 3-4 shows further details about the etching recipes.

One of the disadvantages of using resists as sacrificial layers for the etching is the residues leftovers. For the particular case of DL PMMA, hardened PMMA cannot be striped by acetone or dichloromethane baths. For this reason, hard masks can be sought as an alternative, where thick metal or oxides layers are used to protect from polymer leftovers. After the etching process, these layers can later be removed with specific wet etchants. The drawbacks of this approach are the unintended doping of the 2D vdW layers with the metallic leftovers, and the damage done to the crystal lattice (1 atom-thick) from the energetic deposition of metals.

In this thesis, we used an Oxford Instruments Plasmalab 80 [143] and an Oxford PlasmaLab 100 [144]. There are two variants for the generation of the plasma, the capacitively coupled plasma (CCP), and the inductively coupled plasma (ICP). Figure 3.12 shows a simplified schematic of the chamber of a CCP and ICP RIE system.

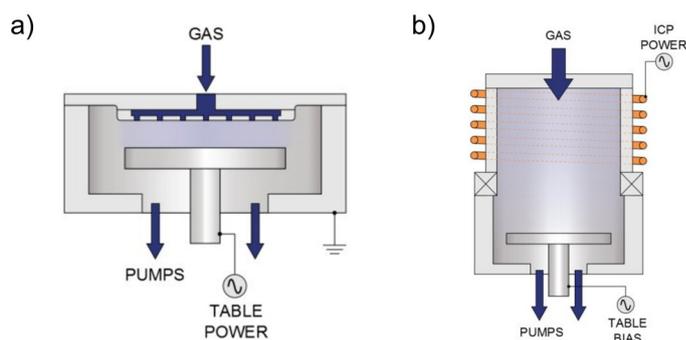


Figure 3.12 a) Sketch of a CCP system. b) ICP RIE system. In a CCP system, the plasma obtains its energy from the applied RF electric-fields between the two closely metallic plates, while in ICP the magnetic field driven by the electromagnetic coil drives the plasma formation. Figures adapted from Ref. [145].

In a CCP RIE, the plasma is formed in between two parallel metallic plates, with the base electrode being covered by an insulating layer (Figure 3.12 a)). The gas flow into the chamber is build up until a desired striking pressure and kept at a constant value during the plasma process. A strong DC bias is applied to strike the plasma, and an AC signal is driven across the two plates at a frequency of 13.56 MHz with a given power, depending on the gas and plasma density desired.

Table 3-4 RIE etching recipes for CVD graphene, CVD graphene encapsulated with Al_2O_3 , and the etching of TMDs on BN.

Mat.	Type	E. M	E. C	Flow (sccm)	C.P (S.P) (mTorr)	RF P. (W)	P.T (s)
Gr	CCP	DL PMMA	Ar	80	60	100	40
			O_2	5	(40)		
Gr/ Al_2O_3	ICP	AZmir701	SF_6	80	10	50	70×4
			O_2	20			+ 40
TMDs on BN	CCP	DL PMMA	SF_6	10	100	100	20
			Ar	10			
1-3L TMDs	CCP	DL PMMA	Ar	80	60	100	40 to
			O_2	5			(40)

Mat. – Material; E.M – etch mask; C.P - Chamber Pressure; S.P – striking pressure; RF P. – radio frequency power; P.T – process time. Scm - standard cubic centimeters per minute.

Most importantly, a feedback system allows for the impedance matching to be adjusted to maintain the plasma. In ICP RIE the plasma is generated via electromagnetic induction, with the RF power supplying the electrons with enough energy to sustain the plasma (Figure 3.12 b)). The higher plasma density of ICP processes require the stage to

be cooled down using an efficient heat sink, usually with He flow, and for the recipes to be divided in several steps with cooling intervals in between. ICP plasma densities can be up to two orders of magnitude higher than regular CCP systems. This higher number of ions per unit volume makes ICP RIE more reactive, and capable of achieving higher etch rates, enabling the etching of hard materials as HfO_2 or Al_2O_3 . Table 3-4 presents a summary of the recipes followed during this work.

3.1.5 Metallization

In the context of electronic transport in 2D materials, metallization processes refer to the deposition of thin films of polycrystalline metals with the purpose of forming electrical contacts [146]. In research environment, the selective deposition of the metal for the formation of electrical contacts is commonly employed using polymeric sacrificial layers that are later removed together with the excess metal, in the so-called *lift-off* process. Depending on the type of contact that one wishes to make between a metal and the 2D material, different thin-film technologies are more well suited than others. Figure 3.13 shows two types of contact configurations that can be explored with 2D vdW materials. These are the top-contacts (2D) and the lateral (1D) contacts.

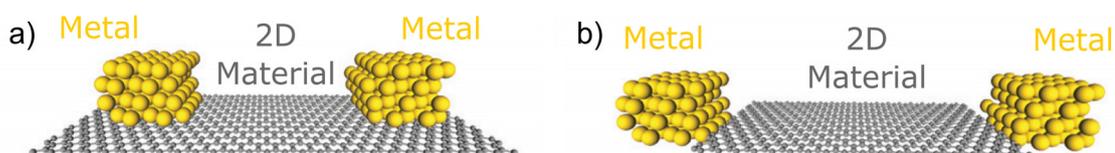


Figure 3.13 Contact configuration between metallic electrodes and channels based on 2D vdW materials. a) Top-contact. b) 1D lateral contact. Figures adapted from Ref. [147]

In a top contact configuration, the metallization is done covering a large area of the surface of the 2D material. Due to the saturated in-plane bonds of vdW materials, the metals evaporated on top are not able to strongly hybridize with the orbitals of the 2D material, leading to the presence of a small vdW gap between the metal and the channel, which ultimately increases the contact resistance. The use of lateral approaches allows for the reactive edges of the 2D materials to be used to covalently bond to the evaporated metal, resulting in enhanced carrier injection [147].

For top contacts, we used both e-beam and thermal evaporation techniques from open chamber systems as Oerlikon [148], UNIVEX 350, and the EPVD75 Kurt J. Lesker [149], which can achieve base pressures of 10^{-6} mbar. Alternatively, ultra-high-vacuum systems (UHV) were also used for e-beam evaporation (Createc [150]) and thermal evaporation (Mantis [151]). In UHV setups, a loadlock allows for the exchange of samples in and out of the system while maintaining the chamber pressure at 10^{-9} mbar. For edge contacts, we used a Von Ardenne CS730 Cluster sputtering system [152]. Figure 3.14 shows a scheme of a e-beam evaporation process versus sputtering.

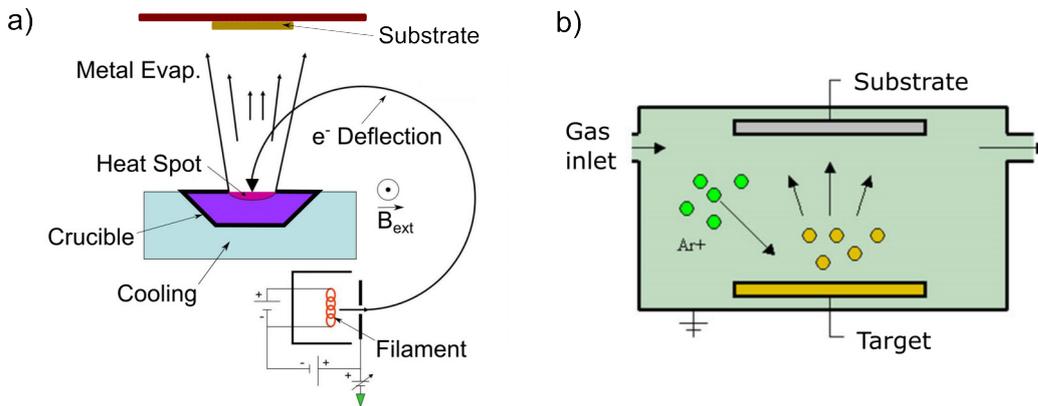


Figure 3.14 Metallization processes. a) E-beam evaporation. The filament emits a flow of electrons deflected by the external magnetic field. The electrons hitting the crucible will locally warm the metal, and for some current setting there will be the evaporation of material onto a substrate surface place directly on top. b) Sputtering. The noble gas flowing through the chamber is made into a plasma of non-reactive elements and physically bombards the target surface, leading to the projection of material onto the substrate surface. Figures a) and b) adapted from Wikipedia.

In e-beam evaporation, a flow of electrons is focused onto a crucible with pellets of a metal (Pd, Ti, Cr, etc) and heated to the point of emitting a gas phase of the material, adsorbing onto the substrate. The directional nature of the evaporation methods allows for the highly anisotropic growth of the metal. To overcome some shortcomings of this approach, the stage might be set under rotation. For the thermal evaporation using effusion cells, the crucible is set at high-temperatures via Joule effect, where a metallic coil surrounding the crucible allows for stable, uniform, and wide range of temperatures to be achieved. This evaporation method uses a similar geometry to the e-beam evaporation process. At high enough temperatures, the material will sublime, being projected in the direction of the crucible opening.

While e-beam and thermal evaporation are highly directional deposition methods, sputtering is an isotropic process. In sputtering, a plasma of a noble gas (typically Argon) bombards a target of the metal to be deposited with ions, ejecting the material. The presence of the plasma randomizes the trajectory of the ejected metal atoms allowing for the deposition to happen isotropically. This feature is desirable to ensure that the sidewalls of the channel are well contacted, which is an important feature for lateral 1D contacts.

Table 3-5 summarizes the recipes followed for the working devices in this thesis. In columns with two metals, the first deposited metal is the top one followed by the bottom one.

Table 3-5 E-beam evaporation and sputtering recipes followed for the deposition of Ti, Au, Ni, Al, and Pd on different channel materials.

Material	Contact	Metal	System	Pressure (mbar)	Evap. Rate (\AA s^{-1})	Thick. (nm)
MoS₂ & Gr	Top	Ti	e-B	10^{-9}	0.7	5
		Au	e-B		1.6	35
Gr (S)	Lat.	Ni	Sput.	10^{-3}	2.5	25
		Al			8.3	50
Gr (D)	Lat.	Ti	Sput.	10^{-3}	2.5	20
		Al			8.3	50
WSe₂	Top	Pd	e-B	10^{-6}	0.6	50
N2200	Top	Al	Th.	10^{-9}	0.6	20

Sput. – Sputtering; Th. – Thermal; Evap. – Evaporation; Thick. – Thickness; S – Source electrode (devices in chapter 8); D – Drain electrode (devices in chapter 8).

3.2 Characterization of devices

3.2.1 Electrical characterization

The electrical characterization of the devices was made using standard direct-current (DC) techniques. The electrical characterization equipment was used together with a Quantum Design [153] property measurement system (PMMS) and Lakeshore [154] probe station. Figure 3.15 shows the several elements composing the PMMS and the probe station.

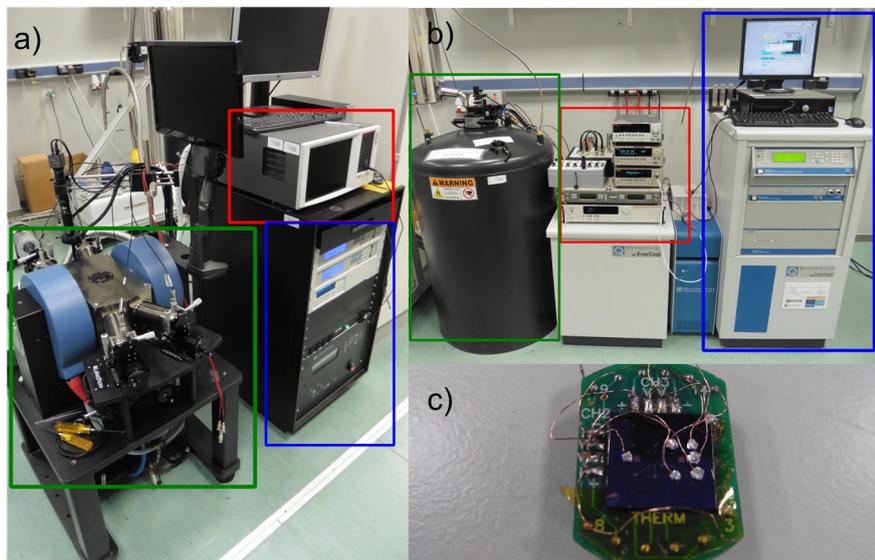


Figure 3.15 a) Lakeshore probe station. High-vacuum chamber with magnetic coils and probe arms (Green). Keithley 4200 semiconductor analyzer (Red). Software controllers (Blue). b) PPMS. Helium flow chamber with nitrogen jacket (Green), Keithley's 2636, 6221, and 2182, and manual/automatic switchboards (Red), computer and software controllers (Blue). c) Puck used to mount the samples. Copper wires connected onto sample metal pads using cold indium pressing.

The Lakeshore probe station has a high-vacuum chamber (10^{-6} mbar) with four movable arms and a metallic stage. It can apply magnetic fields up to 1 T, and reach temperatures down to 7 K and up to 350 K. The cabling is triaxial and allows for more precise measurements of low-level currents, down to 10^{-15} A. The Keithley 4200 semiconductor analyzer [155] is suited for highly resistive systems.

The PMMS uses a superconductor to generate magnetic fields up to 9 T, with horizontal and vertical angular rotators 0.053° precise. The liquid helium cryostat allows for temperatures between 1.8 K up to 400 K, with quick thermalization properties due to

the helium atmosphere, with chamber pressure of 10 Torr (Figure 3.15 b)). The cabling of the system is mainly composed of BNC cables, limiting current readings down to 10^{-10} A. Together with the PPMS, the DC setup used consisted of either a Keithley 6221/2182A current source and nanovoltmeter for conductive devices, or a dual channel Keithley 2636 for more resistive systems. The Keithley 6221/2182A pair uses a *delta-mode* system to remove thermoelectric (Joule) effects and background offsets from the measurements. Keithley 2636 offers a *four-wire* mode, from which a single channel can perform a four-probe measurement, leaving free the second channel to apply a gate voltage. The electrical connections of the samples to the Keithleys were made via a puck with eight pins (Figure 3.15 c)). This puck would then be mounted in a rod, and placed inside the He chamber. The contact pads of the samples were connected to the pins of the puck using cold pressed indium and copper wires. The sample was fixed to the puck with the help of scotch tape or GE – 7031 varnish.

3.2.1.1 Electrical configuration

The electrical characterization of the devices in this thesis was done following local and non-local strategies. Figure 3.16 summarizes the distinctions between the different versions of the electrical measurements explored in this thesis.

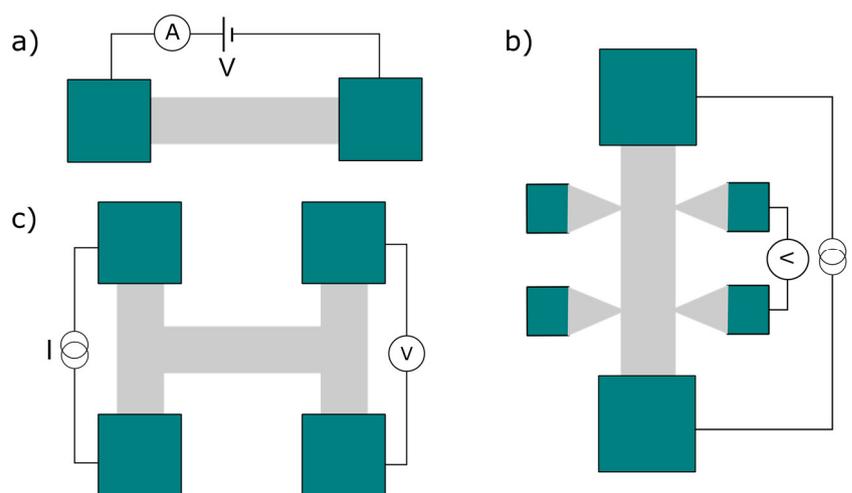


Figure 3.16 Electrical configurations for the devices measured. a) Two-points measurement of the channel resistance. b) Four-probe measurement of the longitudinal resistance of a Hall bar. c) Four-probe measurement of a non-local setup. In all cases, the gate voltage is applied between the n^{++} doped Si/SiO₂ substrate and the electron source electrode.

First, *local measurements* refer to the methods used to probe the direct effect of applying a voltage between two terminals. It can be done in two ways: with a two-point setup, where the current flowing through the device is read through the same terminals that apply a voltage; or with a four-point setup, where two additional terminals measure the voltage drop along the injected current path. While the two-point setup includes the effects of the contact resistance, the four-point method allows for the contact resistance to be disregarded, solely probing the resistance of the channel. The second strategy, *non-local measurement*, is inherently four-point, with the added difference that the voltage probes are not used to measure a voltage drop along the direct current path. In all cases, the resistance is defined always as the ratio between the voltage applied/measured and the current measured/injected, respectively. In all cases, the gate voltage is applied between the dielectric material used (n++ doped Si/SiO₂ substrates for the case of this thesis) and the electron source contact.

3.2.2 Material characterization

Two standard techniques used for characterization of mono-to-few layers of 2D materials are Raman spectroscopy and atomic force microscopy (AFM). During device fabrication, the optical contrast is used as an indicator of the thickness of a 2D vdW material, and the characterization of the device is usually delayed to after the electrical characterization. Common reasons for such practices are the ageing related deterioration of the performance, or the accidental damages done to the channel by using laser based techniques as Raman spectroscopy. To avoid inconveniences, the material characterization is usually left to the end if the process fabrication allows for it. AFM, for example, must be performed before any encapsulation of the channel.

3.2.2.1 Atomic force microscopy

Atomic force microscopy is a scanning probe technique that relies on the proximity of a narrow probe to a surface to detect its variations in height. This type of microscopy relies on piezoelectric elements to resolve structures heights down to 0.1 Å. The AFM is composed mainly of a photodiode, a laser, a cantilever with a tip, and a feedback electronic system that allows for two different modes of operation, the tapping and contact mode.

Figure 3.17 shows an AFM scan of HfO₂ grown on a MoS₂ layer, and the AFM of plain MoS₂ layers after etching using polymeric sacrificial layers.

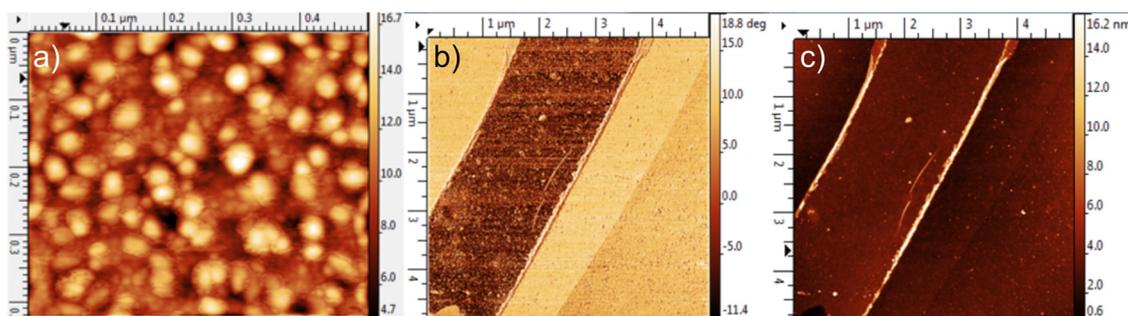


Figure 3.17 a) Atomic force microscopy of ALD-grown 30 nm of HfO₂ on MoS₂. Based on the height profile, the roughness was determined to be of 3 nm, and the maximum peak-to-peak height to be of 15 nm. b) Measurement of a MoS₂ flake. Phase mode. c) Amplitude (height profile) of a MoS₂ flake with the presence of etching residues at the edges.

In the tapping mode, the probe oscillates far from the sample at its resonant frequency. Any change in height will disturb the interactions between the tip and the surface, and the amplitude and phase will be affected. In contact mode, the tip is set in close contact to the surface. While the tapping mode is less invasive, the contact mode can lead to damages to the surface. AFM has been found to lead to inconclusive results when measuring ultra-thin films of 2D vdW materials, with the strong atomic repulsion at the edge of the samples leading to heights not in agreement with the expected thickness obtained from photoluminescence techniques as Raman. Ideally, AFM should be used together with other techniques to account for a better measurement of the thickness of 2D materials. In this thesis, we used a AFM from Agilent Technologies.

3.2.2.2 Raman spectroscopy

Raman spectroscopy is a photoluminescence technique that evaluates the change in frequency of the laser emission line after interacting with the material being probed [156]. By shining an element with a specific laser line, the vibrational modes of the atoms in the crystal lattice will shift the frequency of the emission. This small shift is referred to as Raman shift. The energy of the vibrational modes can be determined from theoretical calculations, and used to index the resulting spectra. Figure 3.18 shows the Raman spectra of CVD graphene, and of mono-to-bulk layers of MoS₂ at room temperature using a laser line of 532 nm.

In graphene, the relevant Raman peaks are denominated D, G and 2D peaks [157]. The G peak is related to the stretching of the bonds, E_{2g} phonon mode, and the 2D peak to the breathing modes of six-atom rings. The D peak is commonly attributed to defects in the lattice. These single Lorentzian peaks can be identified for Raman shifts of 1350, 1580, 2690 cm^{-1} respectively. Additionally, while the width of the G peak is barely affected with increasing layer number, multilayer graphene shows a wider 2D peak, corresponding to the superposition of multiple Lorentzian shaped peaks. For highly crystalline and defect-free monolayers, the ratio between the intensity of 2D and G peak should be $\gg 1$, and the intensity of D should be barely detectable. The polycrystalline nature of CVD graphene and the presence of transition metal impurities lead to a smaller 2D/G intensity ratio and to the presence of a D peak. For highly defective samples this trend develops to lower ratios and higher D peaks.

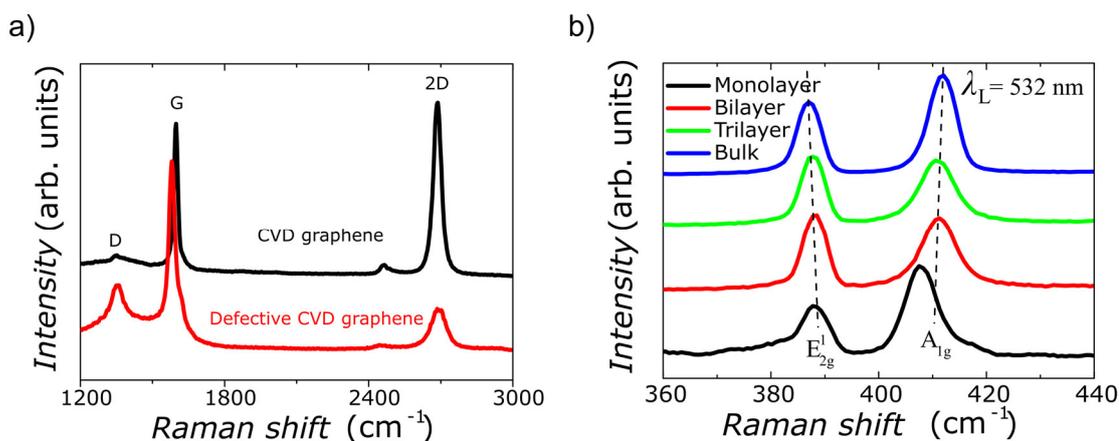


Figure 3.18 a) Raman spectroscopy spectra of CVD graphene and defective CVD graphene. The ratio between the intensity of peaks 2D and G is related to the crystallinity and thickness of the CVD graphene. High ratios indicate very thin films and high crystallinity. The presence of the D peak and of a G peak comparable to the 2D indicate the presence of defects in the lattice. b) Raman spectroscopy spectra of monolayer-to-bulk MoS₂ flakes indicating the two vibrational modes, E_{2g}^1 and A_{1g} , studied for each flake. The width between peaks allows for the identification of the layer count.

In MoS₂, the relevant vibrational modes are associated with the E_{2g}^1 and A_{1g} modes [158]. The E_{2g}^1 peak corresponds to the in-plane opposite vibration of two S atoms with respect to the Mo atom, and the A_{1g} peak to the out-of-plane vibration of S atoms in opposite directions. The E_{2g}^1 and A_{1g} modes can be detected roughly for Raman shifts of 390 and 410 cm⁻¹, with the difference between the frequency of the peaks being indicator of the layer number. The precise determination of the frequencies of each peak is done using a single Lorentzian least square best fit. For monolayers, bilayers, trilayers and bulk-like samples, the expected $\Delta(A_{1g} - E_{2g}^1)$ should be 18.9, 22.7, 23.2, 24.8 cm⁻¹, respectively. For thick flakes, Raman becomes less capable of the precise determination of the number of layers. In these cases, the use of AFM techniques is more effective for the correct thickness determination of the flake.

Although Raman characterization can be employed easily in MoS₂ to obtain a clear identification of the layer count, the same cannot be said for WSe₂, where the relevant quantities are no longer solely differences between the frequency of the peaks, but also the ratio between peak intensities [159]. The high sensitivity and calibration required for the comparison of different samples, makes it hard to implement using our

Raman setup. For this reason, AFM was used preferentially to Raman for the determination of the layer count of WSe₂ devices.

Chapter 4

Magnetoconductance and noise in MoS₂ field-effect transistors

After graphene, MoS₂ is one of the most widely studied 2D vdW materials. Its electrical properties have been extensively characterized, mainly using FETs and Hall bars as platform [55], [56], [60], [74], [160]–[163]. On the other hand, studying the spin transport properties of MoS₂ using lateral local and non-local spin valve strategies lacks an analogous degree of success, although it has been predicted [104] and demonstrated with optical pumping techniques [105] that MoS₂ and other TMDs possess long spin relaxation times. In this regard, weak-localization techniques emerged as an electrical characterization tool that, although unrelated to spintronics, allows for the determination of the relative contribution of spin scattering mechanisms to the diffusive transport of electrons, in this way providing an indirect evidence of the spin-transport properties of the material [164].

The work in this chapter is divided in two parts. First, we study the magnetotransport properties of MoS₂ Hall bars in low-doping regimes, and, second, we study the low-frequency noise (LFN) of the current output of the transistors to determine the origins of the strong current fluctuations.

4.1 Magnetoconductance of MoS₂

One of the motivations behind the study of magnetotransport in MoS₂ emerges from the connection between spin scattering mechanisms and spin-orbit interactions (SOI) [108]. Weak (anti)-localization measurements allows us to determine spin-orbit scattering rates, and in this way to determine if the spin relaxation mechanisms are of Dyakonov-Perel [120] or Elliot-Yafet nature [121] (see section 1.2.2.1, and section

2.2.2). Previous works on thick multilayer MoS₂ flakes placed spin orbit scattering lengths, $\lambda_{s.o}$ in the order of 200 nm, increasing with higher carrier densities [164]. Clarifying the underlying spin-flipping mechanism requires the spin-orbit relaxation time, $\tau_{s.o}$, and the momentum relaxation time, τ_p , to be determined from magnetotransport measurements. In materials that exhibit Dyakonov-Perel scattering mechanisms the relationship between both quantities is given as $\tau_{s.o} \propto \tau_p^{-1}$, while for the case of Elliot-Yafet $\tau_{s.o} \propto \tau_p$. The theoretical framework to determine the relative contributions of elastic, inelastic, and spin-orbit scattering rates in disordered metallic thin-film systems using diffusive transport measurements is given by the Hikami, Larkin and Nagaoka (HLN) theory [107]. By studying the magnetoconductance, $\Delta\sigma_{\square}(B)$, for various channel electron densities at low temperatures, one could in principle conclude about the nature of spin scattering in MoS₂.

Here we study the magnetoconductance of few-layer MoS₂ Hall bars on Si/SiO₂ (250 nm) substrates. Ideally, Hall bars require the voltage probes width to be lower than or equal to 1/10th of the distance between them. For this reason, we looked for natural slab shaped samples more than 10 μm -long and 5 μm -wide using Blue tape exfoliation approaches.

4.1.1 Electrical characterization

Before proceeding with the magnetoconductance studies, we performed preliminary electrical characterization of the fabricated devices in the PPMS system. We used the dual channel Keithley 2636a for the two-probe measurements, using one channel to apply the gate voltage and the other to apply the drain-source bias for the transfer curves. The four-point measurements in this section were done using the *four-wire* configuration of the Keithley 2636a. The fabrication and characterization followed the procedures indicated in chapter 3.

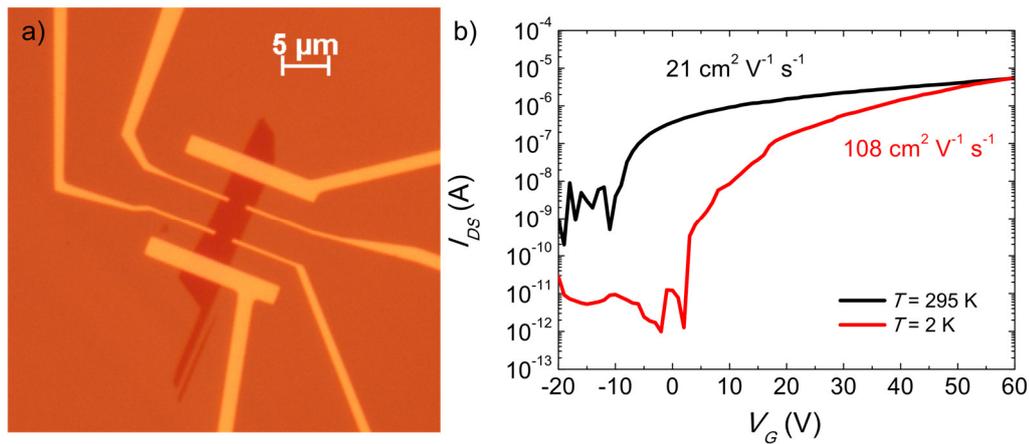


Figure 4.1 a) Optical microscope image of a trilayer MoS₂ Hall bar on 250 nm-thick SiO₂ with Ti (5 nm)/Au (40 nm) contacts. Scale bar: 5 μm. Layer thickness determined using Raman spectroscopy, with $\Delta(A_{1g} - E_{2g}^1) = 23.2 \text{ cm}^{-1}$. b) Drain-source current, I_{DS} , dependence with applied gate voltage, V_G , under a drain-source bias, V_{DS} , of 1 V, at room temperature and at 2 K.

Figure 4.1 a) shows a trilayer MoS₂ Hall bar with Ti (5 nm) /Au (40 nm) contacts. The determination of the channel thickness was done using Raman spectroscopy, with resulting $\Delta(A_{1g} - E_{2g}^1) = 23.2 \text{ cm}^{-1}$, in-line with the expected for a trilayer channel. The channel length, L , between source and drain contacts was of 11 μm and channel width W of 4 μm. The longitudinal distance between the inner electrodes, L_{4P} , was of 5 μm. Figure 4.1 b) shows the corresponding transfer curves using a two-point setup between source and drain contacts. At room temperature, applying a source-drain bias, V_{DS} , of 1 V, the onset of drain-source current, I_{DS} , occurs at a gate voltage, V_G , of -10 V, which is indicative of a n-doped channel, in line with the literature on MoS₂ transistors, where the onset is usually observed between $V_G = -20$ and -10 V for ~ 300 nm-thick SiO₂ dielectric. The maximum field-effect carrier mobility was calculated using the expression $\mu_{FE} = \frac{Lg_{mt}}{WC_GV_{DS}}$, where C_G is the oxide capacitance per unit area, determined from a parallel plate model as $C_G = \epsilon_r \epsilon_0 / d$, and g_{mt} the terminal transconductance, given as $\frac{\partial I_{DS}}{\partial V_G}$. For a 250 nm-thick SiO₂ dielectric, with $\epsilon_r = 3.9$, and ϵ_0 being the vacuum permittivity, the determined C_G was $1.38 \times 10^{-4} \text{ F m}^{-2}$. At room temperature, the device exhibits a maximum μ_{FE} of $21 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, ON/OFF ratio of 10^4 , and maximum subthreshold swing of 2 V/dec, limited by the thickness of the 250-nm oxide used. Lower oxide thicknesses would enable higher sub

threshold swing. The leakage currents (OFF state) are at the 10^{-9} A range at room temperature, being quite large when compared to typical figures of 10^{-11} A, likely due to a small leak through SiO_2 . When cooled down to 2 K, the leakage through the gate greatly decreases, with the current onset moving from -10 to 0 V, in line with previously reported studies on high-quality MoS_2 transistors [160]. At this temperature, the μ_{FE} increases to $108 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, with ON/OFF ratio of 10^6 . The crossing between the two output characteristics reveals the character of a carrier induced insulator-to-metal transition.

Since weak localization phenomena emerges at low temperatures, where the phonon induced inelastic scattering no longer suppresses the coherent backscattering required for the quantum corrections to the resistivity, magnetotransport studies are made at liquid helium temperatures. For this reason, we focus on the transport operation at those temperatures. Figure 4.2 shows the gate dependence of the two-point output characteristics of the device at room temperature, comparing it to the two- and four-point output characteristics at 2 K.

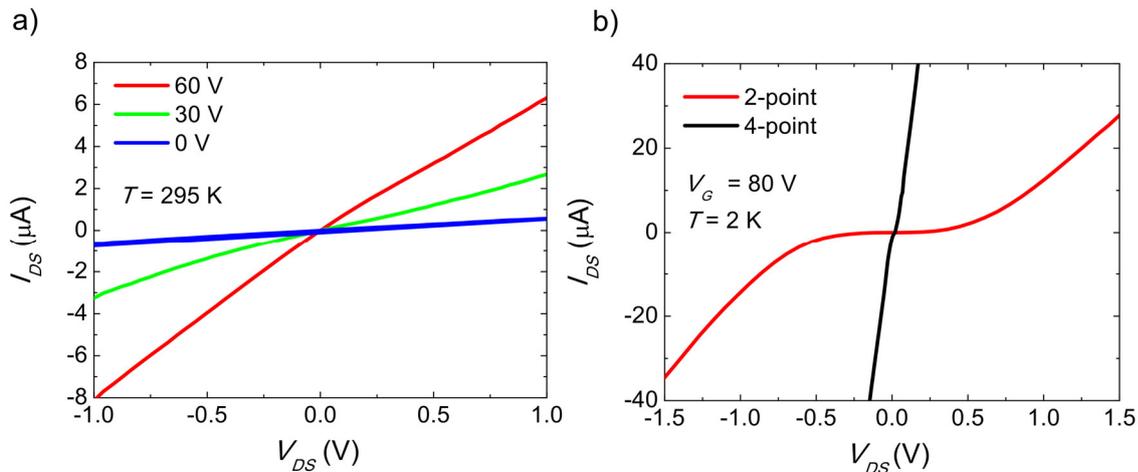


Figure 4.2 a) Two-point output characteristic of the MoS_2 FET at different gate voltages, at room temperature. b) Comparison between the I - V curve obtained with a two-point measurement and four-point measurement at 2 K, under 80 V.

At room temperature, the device shows a near-linear output characteristic across a large range of gate voltages, while at 2 K the output characteristics with $V_G = 80$ V reveals a strongly non-linear symmetric curve. These observations can be explained from a rigid band alignment of the metal/semiconductor contact between the Ti metal

electrodes and the MoS₂ channel. Figure 4.3 shows the energy level band alignment between Ti and MoS₂.

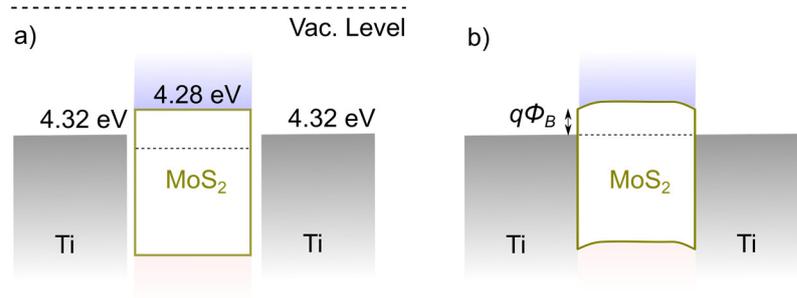


Figure 4.3 Energy level alignment of the FET composed of two Ti electrodes and MoS₂ channel. a) Rigid band model, before contact between the materials. b) Resulting band bending after the materials are brought into contact.

The resulting Schottky barrier due to the mismatch between the work function of the Ti (4.33 eV) metal contact and MoS₂ conduction band (4.28 eV) is of 0.05 eV. At RT, the large thermal energy ($k_B T$) of 0.026 eV, promotes ohmic-like output characteristics. At 2 K, the thermal energy is decreased by a factor of 150, and the small Schottky barrier is sufficient to promote strong non-linearity. The contribution of the interface dominated transport can be somewhat addressed using a 4-point measurement to determine solely the channel contribution. In Figure 4.2 b), the comparison between the 2-point and 4-point measurements shows that most of the voltage drop applied between the drain and source electrodes drops at the interface between the contacts and the MoS₂ channel. At a V_G of 80 V, the channel sheet resistance was determined to be of $R_{\square} = 1.1 \text{ k}\Omega$, in-line with previous studies of high quality MoS₂ FETs using 4-point measurements at low temperature [160]. By using both 2-point and 4-point methods one can extract the contact resistance with the equation $R_c = (R_{2P} - R_{4P} L/L_{4P})/2$ determined as a function of current. The contact resistance for contact pads with an area of $7.8 \text{ }\mu\text{m}^2$ was determined to be of $8 \times 10^4 \text{ }\Omega \text{ }\mu\text{m}^2$ for an I_{DS} of 40 μA . At lower currents, 2 μA , for example, the contribution of the contact resistance would increase up to $\sim 10^6 \text{ }\Omega \text{ }\mu\text{m}^2$.

4.1.2 Hall effect and magnetoconductance

For measurements as a function of magnetic field, prior to data acquisition, the gate voltage was set for one hour to stabilize. This requirement is due to the strong current transient decays observed with time constants of the order of several minutes. This strong exponential transient decay is responsible for the observed wide hysteresis in the trace/re-trace curves of 2D vdW semiconductors on oxide substrates [74]. The four-point measurements were done using the Keithley 6221 and 2182a current source and nanovoltmeter for increased sensitivity.

For the determination of the intrinsic carrier density at 2 K the transversal resistance, R_{xy} , was measured for sufficiently high gate voltages and extrapolated to $V_G = 0$ from the linear fitting of the n_{2D} vs V_G plot. Figure 4.4 a) shows R_{xy} as a function of magnetic field, B , at 2 K, for several gate voltages, and Figure 4.4 b) the extracted intrinsic carrier density.

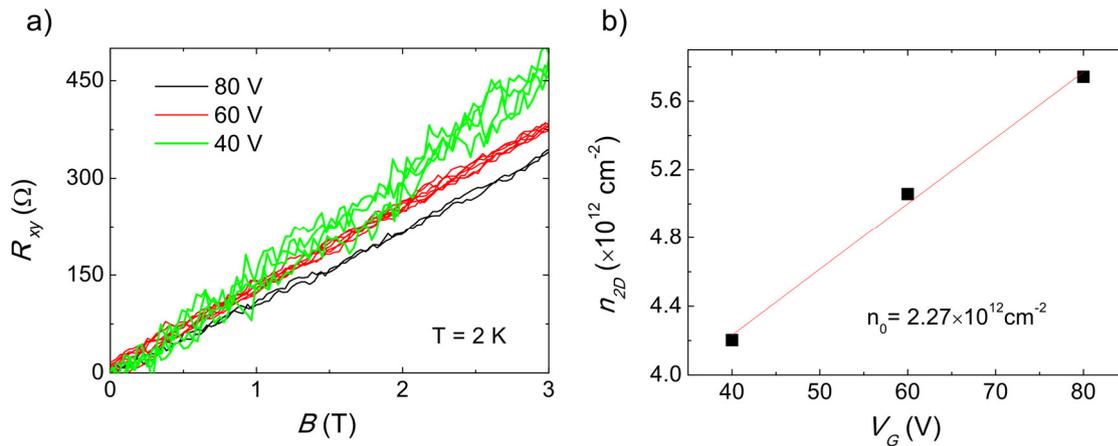


Figure 4.4 a) Transverse resistance, R_{xy} , of the MoS₂ Hall bar as a function of the magnetic field applied perpendicular to the sample's surface. Measurements done at $T = 2$ K, for gate voltages, V_G , of 40, 60 and 80 V. b) Carrier density, n_{2D} , extracted from the slope of the Hall measurement for each gate voltage. A linear fitting (solid red line) to the dependence shows an intrinsic doping of $2.27 \times 10^{12} \text{ cm}^{-2}$ at $V_G = 0$.

The carrier density at each gate voltage was determined using the expression $n_{2D} = \frac{1}{R_H e}$, where the Hall resistance, R_H , is the slope of $R_{xy}(B)$. The intrinsic doping level of the device studied was determined to be $2.27 \times 10^{12} \text{ cm}^{-2}$. Previous reports place the intrinsic doping of MoS₂ mono-to-few layer channels at the levels of $5\text{-}13 \times 10^{12} \text{ cm}^{-2}$, without any clear trend. Using four-probe measurements allows for the precise

determination of the Hall mobility, calculated as $\mu_H = R_H/R_{\square}$ at $V_G = 80$ V, resulting in $1023 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, on pair with the reported Hall mobility of MoS₂ flakes on SiO₂ substrates [160]. Already evident in Figure 4.4 a), the measurements at lower gate voltages are somewhat less stable than the ones at higher gate voltages. Several works regarding magnetotransport in MoS₂ particularly refer to the need of having a high carrier density for stable Hall and magnetotransport measurements in MoS₂, reporting only for carrier densities (with gate voltage included) over $8 \times 10^{12} \text{ cm}^{-2}$ and up to $2 \times 10^{13} \text{ cm}^{-2}$ [110], [164]. In our case the maximum reachable carrier density was $\sim 6 \times 10^{12} \text{ cm}^{-2}$. While a 10% deviation of the effective gate capacitance compared to a parallel plate geometry is expected due to the finite size effects (fringe fields), further deviations from the ideal model can be accounted from trap states. From the slope of the n_{2D} vs V_G plot we can extract the effective capacitance C_{eff} with the expression $C_{eff} = \frac{\partial n_{2D}}{\partial V_G} e$, placing it at the $0.7 \times 10^{-4} \text{ F m}^{-2}$. Roughly 50% of the predicted $1.38 \times 10^{-4} \text{ F m}^{-2}$. Using a series capacitance to model the contribution of the interface traps to the total capacitance, the density of interface traps, D_{it} , can be determined using the expression: $D_{it} = C_{it}/e^2$, where C_{it} is the interface trap capacitance, determined as $C_{it} = \frac{C_G C_{eff}}{C_G - C_{eff}}$. In our work, we observed a density of trap states of the order of $9 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$.

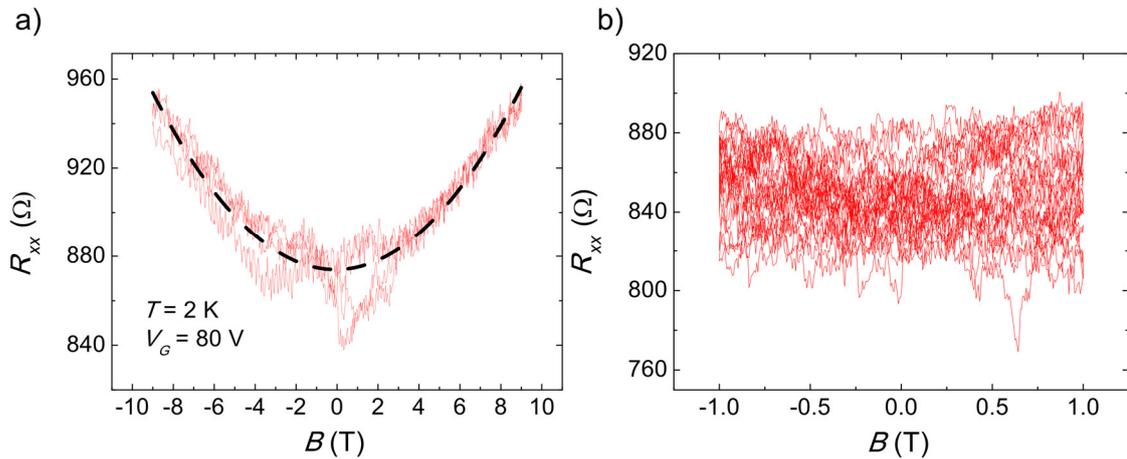


Figure 4.5 a) Longitudinal resistance, R_{xx} , dependence with external magnetic field applied perpendicular to the sample's surface for two consecutive trace and re-trace sweeps. Solid line is the fit to a B^2 dependence. b) Same as a), but focusing on -1 T to 1 T range. 10 consecutive trace and re-trace sweeps.

To study the magnetotransport measurements, the longitudinal resistance, R_{xx} , of the sample was measured at 2 K, applying $V_G = 80$ V and injecting a current of $10 \mu\text{A}$.

We explored the full range of magnetic fields available with the PPMS system used. Figure 4.5 shows the dependence of the four-point resistance with the external magnetic applied perpendicular to the surface. We observed a maximum magnetoresistance, $MR = \frac{R_{xx}(B) - R_{xx}(0)}{R_{xx}(0)}$, of 14%. At higher magnetic fields ($|B| > 6\text{T}$), a clear symmetric increase of magnetoresistance is visible, following a B^2 dependence, which can be attributed to ordinary magnetoresistance (OMR). At lower magnetic-fields, $|B| < 6\text{ T}$, two successive sweeps reveal a large fluctuation of the magnetoresistance. The unreliable data at $|B| < 6\text{ T}$ made it difficult to employ the HLN theory for weak localization effects to extract information about $\tau_{s.o.}$. For lower V_G , these fluctuations become larger, and for higher temperatures no feature would emerge other than the OMR for high magnetic fields. Further sweeps would reveal more fluctuations without a clear visible trend (Figure 4.5 b)). Although Figure 4.5 b) focuses on the -1 to 1 T range, the same would be seen if the range was increased to -4 to 4 T. Subsequent devices fabricated revealed to exhibit the same strong current fluctuation problems regardless of the device being monolayer to few nanometers thick. Previous studies on the magnetoconductance of few-layer MoS₂ flakes indicated a maximum magnetoconductance $\Delta\sigma_{\square}$ of the order of $0.3\text{-}1 \times 10^{-6}\text{ S}$ (excluding OMR effects)[110], [164]. In our case, with $R_{\square}(0) = 1.1\text{ k}\Omega$, the expected change in resistance, $R_{\square}(B) - R_{\square}(0)$, would be of 4-12 Ω , respectively. Clearly, the observed fluctuations greatly overcome this precision. Regarding the origin of current fluctuations in MoS₂, it has been shown that the presence of trapping and de-trapping processes at the channel to insulator or vacuum interfaces leads to the relaxation of the current time series with bi-exponential dependences, to time-dependent contributions to the electron transport characteristics, and to fluctuations in the carrier density [65], [73], [74]. Even though in our experimental procedure we included long setting times for the back-gate to reduce possible current transient decays, the fluctuations were still too large.

Limited by the precision of the measurements, we decided to study the origins of the strong fluctuations observed in the MoS₂ channels at low-doping regimes.

4.2 Low-frequency noise in MoS₂ transistors under photodoping

At the ultimate thinness level, electrons in 2D vdW FETs are particularly vulnerable to interactions with the surrounding environment [64]–[68], [70], [71]. The induced trap states in the band gap of semiconducting material and the ionized impurities lead to fluctuations in the current output. These apparently random oscillations can be decomposed in a frequency spectrum using fast-Fourier transform (FFT) procedures. Studying the dependence of the power spectral density (PSD) with frequency can provide additional insight about the microscopic mechanisms driving the oscillations. In 2D materials in particular, the PSD of the current oscillations, $S_I(f)$, has been reported to follow an inverse dependence with frequency f of $1/f^\beta$ -type, where β is a characteristic exponent [65]–[68], [70], [72]. The impact of the low-frequency noise (LFN) in the performance of electronic devices becomes more relevant for downscaled devices, where interfaces dominate transport. LFN is the main contributor to the phase noise of sensors and high-frequency operating systems, where the non-linear nature of most of the electronic circuits leads to strong upconversion of LFN to higher-frequencies [67].

In this section, we study the current fluctuations in MoS₂ FETs to address three questions. First, how current output transient decays affect low-frequency noise (LFN). Second, if photodoping, by strongly modulating the carrier density, can modify the LFN mechanisms. And third, if LFN mechanisms in MoS₂ FETs undergo a significant change with incremental channel layer number. This work was done in collaboration with the group of Prof. Farkhad Aliev, in the Universidad Autónoma de Madrid.

4.2.1 Structural and preliminary characterization

We studied four MoS₂ FET devices with monolayer, bilayer, trilayer and bulk channels. Along this work, we will report mainly on the bilayer as a representative of the monolayer and bilayer devices, and on the trilayer as a representative of trilayer and bulk devices, since the main significant change in LFN was observed between these two groups of devices.

For the fabrication of the samples we used deterministic transfer techniques and Ti (5 nm)/Au (40 nm) metal electrodes defined by standard EBL (see chapter 3 for

details of the recipes). Figure 4.6 shows the structural and preliminary electrical characterization done to the as-fabricated FETs.

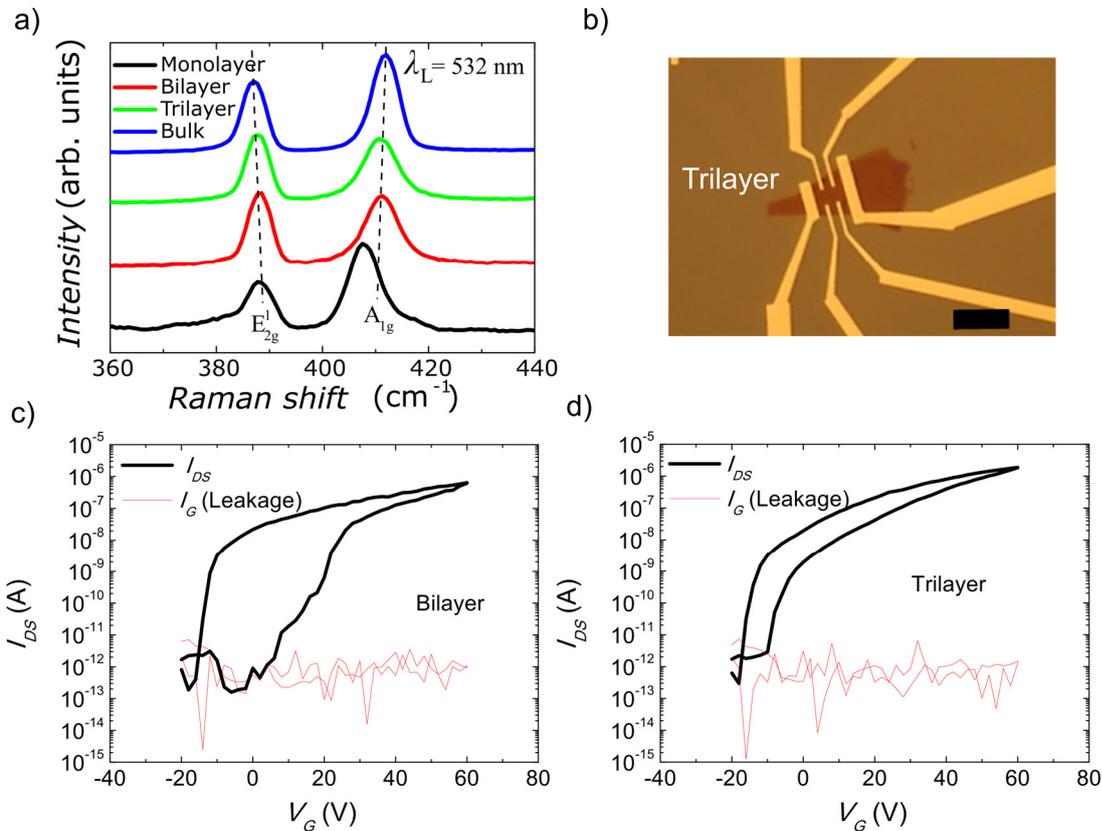


Figure 4.6 a) Raman shift of the monolayer to bulk devices using a laser line of 532 nm. The channel thicknesses were determined by Raman spectroscopy, with $\Delta(A_{1g} - E_{2g}^1)$ of 20.2, 22.8, 23.1, and 24.8 cm^{-1} for the monolayer, bilayer, trilayer, and bulk channels, respectively. b) Optical microscope image of the trilayer MoS_2 Hall bar with Ti/Au contacts. Scale bar: 10 μm . c), d) Trace and re-trace transfer curves of the bilayer and trilayer device to monitor the hysteretic behavior while gating, using the Lakeshore probe station system at base pressures of 10^{-6} mbar. Measurements at room temperature and under a V_{DS} of 1 V.

The number of layers of the flakes used for the MoS_2 FETs was determined using Raman spectroscopy, with resulting $\Delta(A_{1g} - E_{2g}^1)$ of 20.2, 22.8, 23.1, 24.8 cm^{-1} , corresponding to monolayer, bilayer, trilayer and bulk device channel, respectively, in accordance to literature [158] (Figure 4.6 a)). Figure 4.6 b) shows an optical microscope image of the trilayer device contacted with Ti/Au contacts, and Figure 4.6 c) and d) show the two-point transfer curves measured at room temperature and at high-vacuum conditions (using the Lakeshore probe station to better monitor the leakage currents) for the bilayer and trilayer device, respectively. The gate voltage sweeps were

done at a rate of $\sim 0.05 \text{ Vs}^{-1}$, starting at $V_G = -20 \text{ V}$, with 60 seconds to set the first measurement. The maximum field-effect carrier mobility was calculated using the expression $\mu_{FE} = \frac{Lg_{mt}}{WC_GV_{DS}}$, where C_G is the oxide capacitance per unit area, determined from a parallel plate model as $C_G = \epsilon_r \epsilon_0 / d$, and g_{mt} the terminal transconductance, given as $\frac{\partial I_{DS}}{\partial V_G}$. For a 250 nm-thick SiO₂ dielectric, with $\epsilon_r = 3.9$, and ϵ_0 being the vacuum permittivity, the determined C_G was $1.38 \times 10^{-4} \text{ Fm}^{-2}$. The field-effect mobility of the devices was determined to be roughly 20, 9, 14, and 25 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the monolayer, bilayer, trilayer and bulk-like device, respectively (lateral dimensions of the devices: $L^{mono} = 3.7 \text{ }\mu\text{m}$, $W^{mono} = 2.8 \text{ }\mu\text{m}$, $L^{bi} = 3.6 \text{ }\mu\text{m}$, $W^{bi} = 4.3 \text{ }\mu\text{m}$, $L^{tri} = 5.6 \text{ }\mu\text{m}$, $W^{tri} = 5.5 \text{ }\mu\text{m}$, and $L^{bulk} = 53 \text{ }\mu\text{m}$, $W^{bulk} = 12 \text{ }\mu\text{m}$). The trace and re-trace shown in Figure 4.6 c) and d) indicate the presence of strong trapping effects affecting the forth and back sweep. Although in these specific set of devices there is an apparent correlation between the layer thickness and the width of the trace and re-trace curves, such relation seem to have no causality, since in other devices fabricated there was no such direct connection.

4.2.2 Electron transport with and without photodoping

Before proceeding into the characterization of low-frequency noise with and without photodoping, we evaluated the direct-current (DC) transport with and without illumination to establish a foot-ground for the LFN studies. The imposition of an optically accessible chamber to measure the effects of photodoping in the LFN of the MoS₂ FETs lead to the use of a setup without the possibility of applying an external magnetic field and at ambient conditions. The current was measured with a Keithley 6485 picoammeter, using two-point strategies, and the drain-source voltage was supplied with a home-made ultra-low noise voltage source with output of 1 V. The gate voltage was applied up to 80 V using a Keithley 228A source. The optical excitation was driven by a TOPTICA-iBeam Smart diode laser with emission line at 487 nm and with up to 1 mW of nominal output power. The effective light intensity was estimated to be substantially below $1 \text{ }\mu\text{W } \mu\text{m}^{-2}$. The size of the laser spot of tens of μm in diameter covered the surface of the MoS₂ channels. Figure 4.7 shows the performance of the FETs with and without laser illumination at room temperature and ambient conditions.

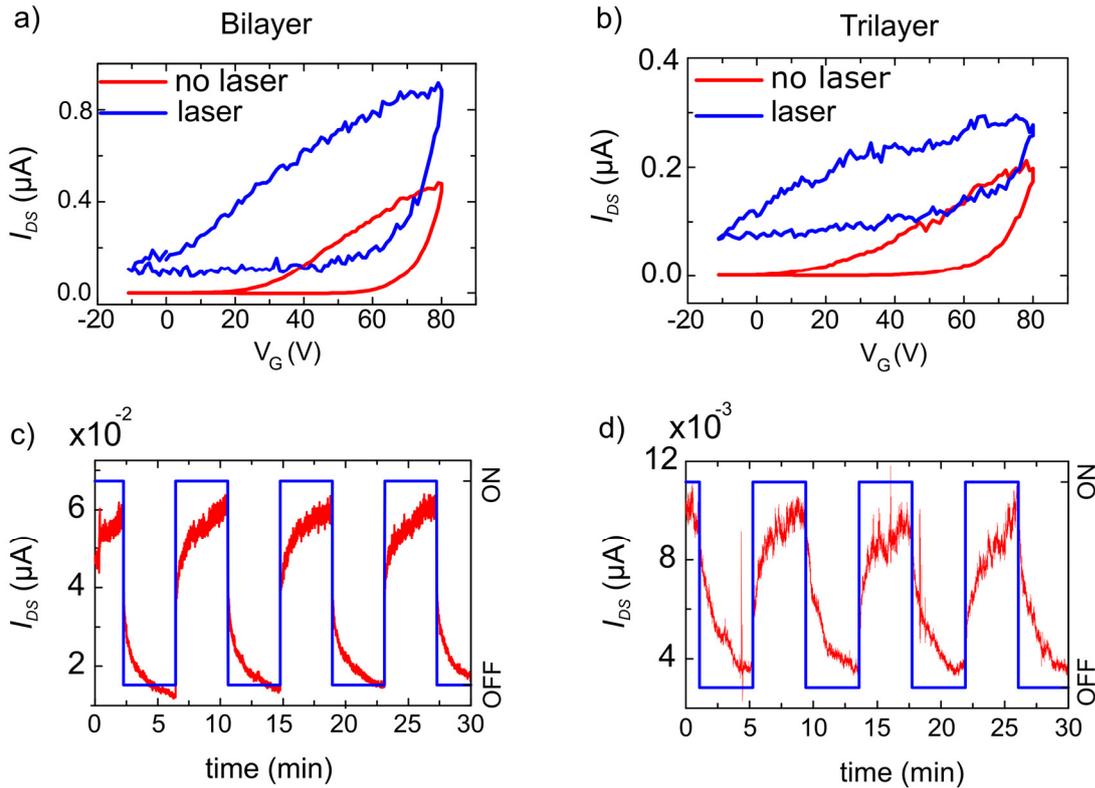


Figure 4.7 I_{DS} as a function of the gate voltage V_G with and without laser illumination of a) bilayer and b) trilayer devices. c) and d) Photocurrent response to laser pulses for the bilayer and trilayer device, respectively. $V_G = 0$ V, $V_{DS} = 1$ V. Blue solid line represents the time dependence of the ON/OFF incidence of illumination with laser output power of 0.1 mW. Period $t = 500$ s.

Compared to the transfer curves obtained under vacuum conditions, under ambient conditions I_{DS} decreases by one order of magnitude for the bilayer and trilayer devices, in-line with previous reports on the influence of environment conditions in the electrical characteristics of TMD-based FETs [165]. In all cases, with laser illumination, the transistor leakage current greatly increases from 10^{-12} to 10^{-8} A, while the ON state the current output increases by a factor of 2. It is also visible an increase of the hysteretic behavior, in-line with previous studies [74]. With the periodic ON-OFF laser incidence (denominated “under illumination”, and “under dark conditions”, respectively) it was visible a strong time dependence of the photocurrent. Using an exponential decay fitting we determined a time constant of 180 s for the relaxation. These time scales of photocurrent relaxation have been reported for MoS₂ FETs, and were attributed to the presence of defects [73]. For this reason, we decided to perform a preliminary study of the LFN in three periods, $P1$, $P2$, $P3$, along the current time series

(both in dark conditions and under illumination), each lasting for about 60 s, with $P3$ being the closest to equilibrium.

4.2.3 Low-frequency noise in MoS₂

4.2.3.1 Noise without photodoping

To perform the LFN experiments, we recorded the current relaxation time series for 180 s at a fixed gate voltage after steeply sweeping it up by 2 V for two different laser illumination conditions. When no laser illumination was applied, the condition was referred to as “under dark condition”. When under laser illumination, it was referred to simply as “under illumination”.

In order to evaluate the mechanisms driving the LFN, we evaluated the current time series by studying the power spectral density of the current and analyzed it using the empirical Hooge relation, $S_I = \alpha I^2 / f^\beta$, where S_I is the square of the module of the fast Fourier transform of the current time series expressed as a function of the frequency f (*i.e.* power spectral density of the current time series), I the average current, and α and β characteristic Hooge parameters obtained from fits in the 0.05-5 Hz frequency range. When β is close to one, or roughly in between 0.7 and 1.5, the fluctuations are called $1/f$ noise.

The dependence of the channel resistivity with gate bias (ON/OFF ratio of 10^6), makes it more convenient that we apply a continuous V_{DS} and record the I_{DS} output of the device for consecutively increasing gate voltages, with steps of 2 V, with fluctuations recorded for 180 s at each step. At room temperature, the Schottky barrier of 0.05 eV between the Ti work function and MoS₂ results in Ohmic-like contacts, ensuring that S_I is proportional to I_{DS}^2 .

Figure 4.8 a) shows the particular case of the current time series dependence of the trilayer device under dark conditions after a V_G steep sweep of 2 V, from $V_G = 0$ V, with an applied bias of 1 V. The current intensity time series was measured with a resolution of 67 ms. The current intensity exponentially decays with time, and at $P3$ seems to be in a stable steady state.

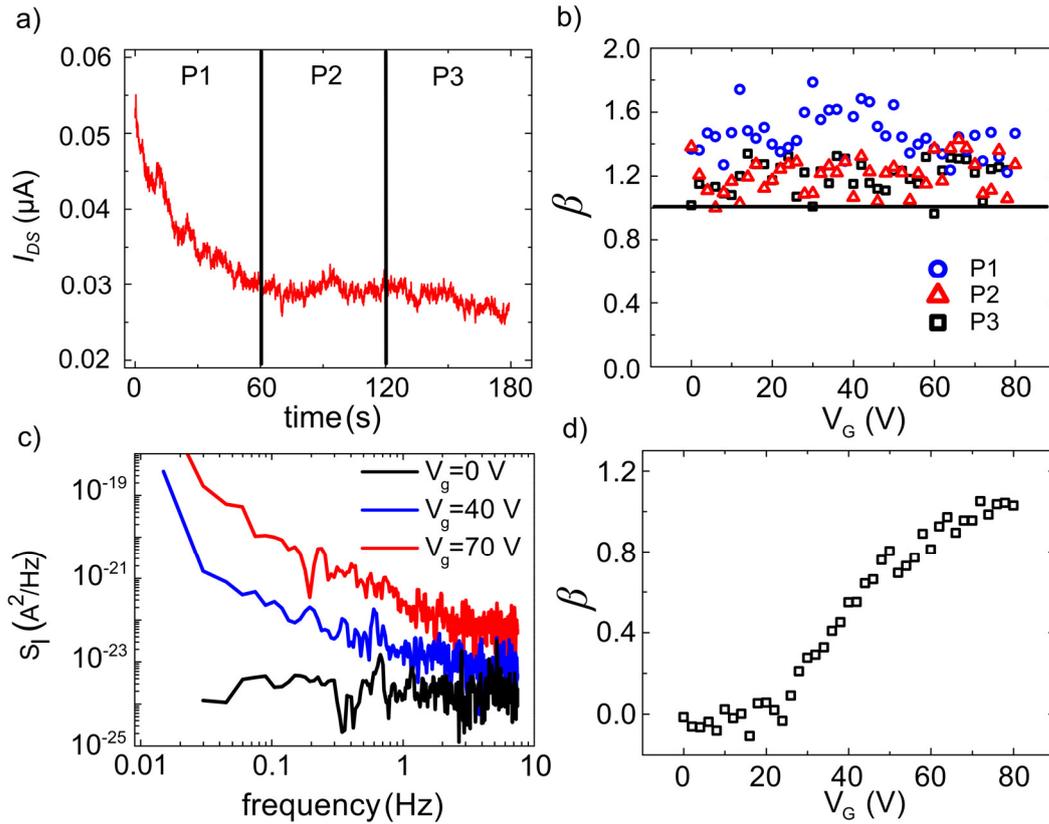


Figure 4.8 a) Transient decay of I_{DS} for the trilayer device after the gate voltage V_G is steeply swept up by 2 V from $V_G = 0$ V. $V_{DS} = 1$ V. Periods $P1$, $P2$, $P3$, of 60 s each. (b) β as a function of gate voltage for $P1$, $P2$, and $P3$. Trilayer device. Solid line represents the ideal β value for $1/f$ -type LFN. (c) Power spectral density of the bilayer device at $P3$ for different gate voltages. (d) β as a function of gate voltage for the bilayer device at $P3$. All measurements are under dark conditions.

In order to evaluate the effects of the transient decay in the LFN, in Figure 4.8 b) we plot the gate dependence of the determined β at $P1$, $P2$, $P3$, for the trilayer device. β decreases from above 1.5 to 1 as the time series goes through $P1$ to $P2$ and to $P3$. The dependence of the LFN with the period of the current time series was observed in all samples. The dependence of β with the considered period is not unique for this system, as it was also observed in off-equilibrium magnetic tunnel junctions near the switching to the antiparallel state [166]. Using only the data for the situations where the system was closer to equilibrium ($P3$), and using the bilayer as a representative sample, we can see a clear dependence of the $S_I(f)$ with gate voltage (Figure 4.8 c)), where the power spectrum density slope increases with increasing gate voltage. Taking a closer look at the gate dependence of β for the bilayer sample (Figure 4.8 d)), we can see that for $V_G < 20$ V β is close to 0, undergoing a crossover to $1/f$ noise when $V_G > 40$ V. Comparing

Figure 4.8 b) and d), the data suggests a dependence of LFN with layer thickness. Regardless, in equilibrium ($P3$), and at $V_G \gg V_{TH}$, $\beta \sim 1$. However, for the monolayer and bilayer devices at low gate voltages, $\beta \sim 0$, suggesting that a strong random-telegraph noise (RTN) was overcoming the $1/f$ -type noise. RTN emerges from dominating generation-recombination processes that lead to a Lorentzian spectrum, where the PSD tends to constant values at low frequencies. Since MoS₂ exhibits a strong decrease of defect-assisted recombination times with decreasing number of layers [161], [167], the observed behavior of β with layer number and electrostatic gating is then related to the competition between the strongly dependent recombination time scales with number of layers [161], [167], and the intrinsic electron doping of each flake, known to vary strongly with ambient conditions [165].

4.2.3.2 Noise crossover with photodoping

In order to understand the microscopic mechanisms driving the LFN in the $1/f$ regime, there are two models based on the Hooge relation that can be employed (see section 2.1.3.3). These are the Hooge-mobility fluctuation (HMF) and carrier-number fluctuation (CNF) models [168]. In the CNF model, the inverse Hooge parameter α^{-1} depends quadratically with the gate voltage. In the HMF model, α^{-1} depends linearly with gate voltage. The observed low conductivity of MoS₂ FETs should place them in the limiting case of weakly conducting regimes, and therefore the CNF model should suit the LFN. The HMF model is commonly valid for conducting regimes [114].

For the analysis of the gate dependence of the Hooge inverse noise parameter, α^{-1} , and β we follow the work of Ref. [65]. Since for $V_G - V_{TH} < 0$ the device is in the OFF state, the analysis of the noise parameters was done only when $V_G - V_{TH} > 0$, where the carrier density n can be approximated as $n \propto (V_G - V_{TH})$. Additionally, the study of the parameters must be done in the cases where the power spectrum density is approximately of $1/f$ -type ($0.7 < \beta < 1.5$).

Figure 4.9 shows the gate dependence of the α^{-1} and β parameters for the bilayer and trilayer devices for several laser powers.

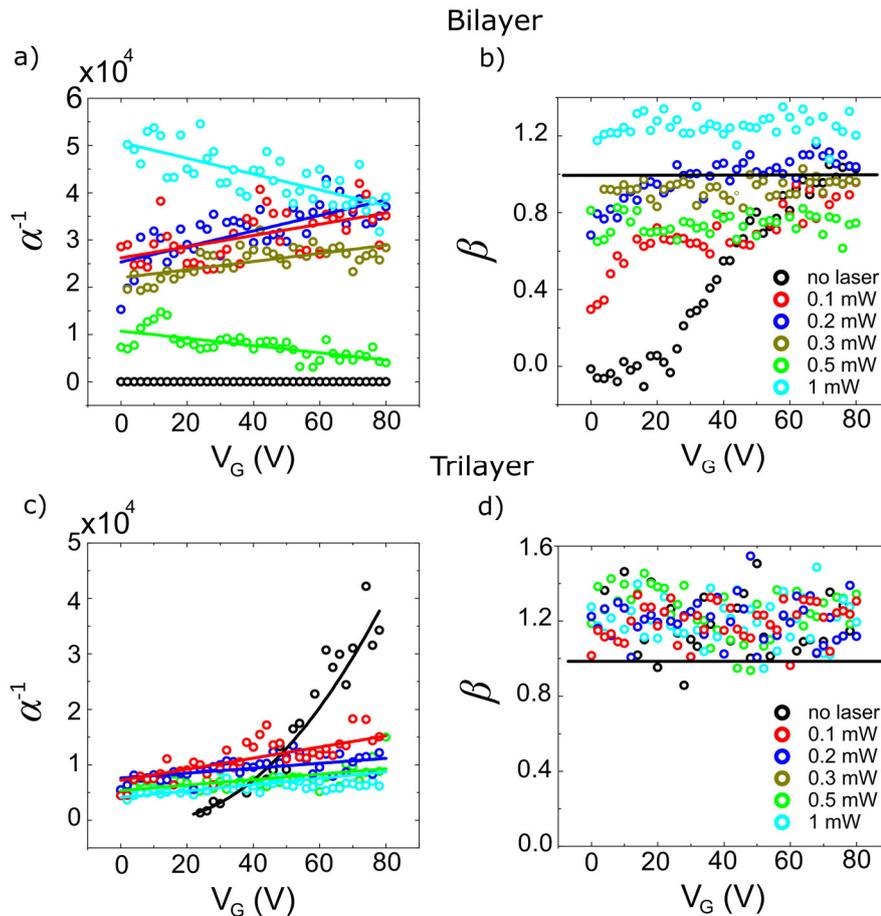


Figure 4.9 LFN in MoS₂ with and without photodoping. a), b) α^{-1} and β dependence with gate voltage for different laser illumination conditions for the bilayer device. c), d) α^{-1} and β dependence with gate voltage for different laser illumination conditions for the trilayer device. In α^{-1} plots, the solid lines are fittings to the gate voltage dependence. In β plots, the solid line represents the ideal β value for $1/f$ -type LFN.

Evaluating the results without laser illumination (under dark conditions), the bilayer device (Figures 4.9 a) and b)) suggests that the crossover to a sufficiently conducting regime with $1/f$ -type noise occurs only at gate voltages above 30 – 40 V. The absence of the $1/f$ at lower gates was already discussed, originating from dominating generation-recombination processes for lower channel thicknesses. The analysis of the dependence of α^{-1} with V_G must then be applied only for the data between gate voltages of 40 to 80 V. In this window of data, α^{-1} depends linearly with V_G indicating Hooge-mobility fluctuations as the driving mechanism for LFN. The trilayer device (Figures 4.9 c) and d)), on the other hand, exhibits a quadratic dependence of α^{-1} as a function of the gate voltage. Together with the fact that in the

explored gate voltage range the devices show $1/f$ -type noise (from the β parameter analysis), we can pinpoint carrier-number fluctuations as the underlying physical mechanism driving the LFN. With this information we can identify two different LFN noise behaviors without laser illumination in the monolayer-to-bulk devices: the monolayer and bilayer showed $1/f$ -type HMFs at gate voltages above 40 V for the bilayer device (60 V for the monolayer), while the trilayer and bulk device show $1/f$ noise driven by CNFs for the all applied gate voltages.

With laser illumination, the bilayer device (Figures 4.9 a) and b)) shows a linear dependence of α^{-1} with the gate voltage, but a not so clear dependence of the β parameter. While under dark conditions, and for gate voltages lower than 40 V, the LFN is of RTN-type, with increasing laser power, the β dependence changes to $1/f$ -type across the full gate range. This observation suggests that the additional photoconducting channels contribute to LFN dominated by HMFs. For the highest laser powers, the device shows a strong reduction of the normalized noise power. This effect can be explained by an increase in the recombination rate of the charge carriers that ultimately leads to a decrease in conductance and increase in LFN. For the trilayer, its visible a crossover from a quadratic dependence of the α^{-1} with the back-gate voltage to a linear dependence. This change indicates a crossover of the LFN mechanisms driving the fluctuations from fluctuations in the carrier number to fluctuations in the carrier mobility, respectively. In order to clarify all the information, Table 4-1 summarizes the findings from the analysis of Figure 4.9.

Table 4-1 Summary of the dependence of LFN mechanisms with the electrostatic gating and photodoping conditions for the four different devices: monolayer, bilayer, trilayer and bulk.

	Photodoping			
	No		Yes	
	Gate voltage		Gate voltage	
Thickness	$V_G \geq V_{TH}$	$V_G \gg V_{TH}$	$V_G \geq V_{TH}$	$V_G \gg V_{TH}$
Monolayer	RTN	HMF	HMF	HMF
Bilayer	RTN	HMF	HMF	HMF
Trilayer	CNF	CNF	HMF	HMF
Bulk	CNF	CNF	HMF	HMF

The analysis of table 4.1 allows us to extract several observations and conclusions. We see that the monolayer and bilayer devices without laser illumination and gate voltage just above the threshold voltage show RTN, while under the same conditions, the trilayer and bulk-like devices show CNF. As discussed before, the RTN originates from the strong dependence of the recombination time-scales with layer number. For gate voltages just above the threshold voltage, by shining the monolayer and the bilayer, the increase in the carrier density is enough to drive $1/f$ noise of HMF character.

An additional observation is that there is a crossover from CNF to HMF of the trilayer and bulk devices with laser illumination. In order to understand this effect, we refer to one work that has already explored LFN in semiconducting transition metal dichalcogenides using a random resistor network model [169], where according to the reference, this effect could be understood as a consequence of the percolative nature of the conductance in TMD FETs [169]. The crossover in the LFN microscopic mechanism from CNF to HMF originates then from the change of charge transport in MoS₂ from a regime where electrons hop or tunnel between disconnected metallic puddles at the Fermi level to a regime of continuum percolation, where instead of a random network of disconnected metallic puddles there is a continuum electron sea at the Fermi level. This transport picture is referred to as an island-and-sea representation of the carrier distribution in the MoS₂ flakes [169].

One important additional observation can be extracted from the analysis of Table 4-1. With the combined effects of photodoping and high electrostatic gating, all devices show HMF. This observation suggests that the intrinsic doping levels of the thinner devices are higher than of the devices with thicker channels since electrostatic gating on dark conditions is not enough to drive the trilayer and bulk-like devices to HMF LFN, while the monolayer and bilayer show HMF. This case is not unique to our samples, with other reports observing a higher carrier density with decreasing layer count [160].

Although in our study we observe a wide range of LFN mechanisms using just a single material, the conditions tested here allows us to combine the several elements for the dependence of β and α^{-1} with the layer thickness, gating, and laser illumination, to conclude over an overall picture for the LFN in MoS₂. The observed effects arise from a

complex interplay between the several electron-doping sources, namely the intrinsic doping of the flakes, the photodoping, the electrostatic doping, the strong decrease of the recombination time scales with decreasing layer number, and the percolative nature of electron transport in MoS₂. RTN changes to $1/f$ -type HMF noise in the thinner devices (monolayer and bilayer) under strong enough electron-doping, while the thicker devices (trilayer and bulk) exhibit mainly $1/f$ -type CNFs for overdrive conditions. In the $1/f$ -type noise regime, we observe a crossover from CNF to HMF driven by photodoping, where by illuminating the surface of the FETs the discontinuous random resistive network percolates to a continuum electron sea at the Fermi level.

4.3 Conclusions

In this chapter, we first explored the magnetoconductance of MoS₂ Hall bars under low-doping regimes. The transfer curves and output characteristics of the device shown are in-line with previous reports on high quality MoS₂ FETs, but the Hall measurements show a lower intrinsic carrier density, and maximum doping achieved by gating. The observed stability during the magnetotransport measurements has been reported to be a strong limiting factor, with works reporting only magnetotransport studies for doping values higher than $8 \times 10^{12} \text{ cm}^{-2}$. We then moved to study the origin of the strong fluctuations by analyzing the LFN of four MoS₂ devices, composed of monolayer, bilayer, trilayer, and bulk channels. Studying LFN under photodoping, for different layer thickness, and using electrostatic gating allowed us to identify the mechanism by which a wide-range of LFN effects are reported in MoS₂ transistors. LFN in MoS₂ is the result of a complex interplay between the several electron-doping sources (the intrinsic doping of the flakes, the photodoping, and the electrostatic doping), the strong decrease of the recombination time scales with decreasing layer number, and the percolation from a discontinuous random resistive network to a continuum electron sea at the Fermi level.

Chapter 5

Engineering WSe₂ transistors using vdW heterostructures

Within the family of semiconducting vdW TMDs, WSe₂ is another promising material for electronic and optoelectronic applications. The smaller band gap and the *p*-type doping makes WSe₂-based transistors a strong alternative to MoS₂-based electronics. Its use has been demonstrated in electrically tunable light emitting diodes [170], field-effect transistors (FETs) [59], [171], [172], electrically switchable chiral light-emitting transistors [173], among others. Field-effect hole mobility up to 180 cm² V⁻¹ s⁻¹ and electron mobility up to 142 cm² V⁻¹ s⁻¹ at room temperature have been reported in single-layered WSe₂, although these figures of merit for device performance are commonly taken under high induced carrier densities, and involve the use of high-*k* dielectrics, dual gating, ionic liquid gating techniques, as well as four-probe measurements [174].

Alongside the applications, a great effort has been put in optimizing device performance of WSe₂-based devices in an attempt to understand the role of metal contacts, doping, and passivation, both on the CVD and exfoliated counterparts of WSe₂, mainly using planar FETs as a device template [57], [58], [127], [171], [172], [175]. Depending on the metal contacts used and/or the production method of the channel (CVD or exfoliated), WSe₂ field-effect transistors may exhibit unipolar *n*-type, *p*-type, or ambipolar characteristics [58], [171], [174].

A main component of the work for electrically tunable applications comes then as an improvement of the channel mobility and of the metal contacts. Complementarily, here we report on the WSe₂ FET characteristics dependence on the ability to drive an unscreened inversion layer in the device channel. The operation of WSe₂ field-effect transistors (FETs) at room temperature and under low doping regimes is dominated by

hysteretic affects arising from trap states. Device concepts relying on WSe₂ channels will greatly depend on the optimization of the device transport characteristics. In this chapter, we first optimize the fabrication conditions of ambipolar WSe₂ FETs on SiO₂, and then compare the transport in three different device configurations: SiO₂/WSe₂, SiO₂/WSe₂/BN, and SiO₂/BN/WSe₂.

5.1 Optimization of ambipolar WSe₂ transistors on SiO₂

To optimize the ambipolar WSe₂ FETs on SiO₂ we first considered three different conditions that could influence the device performance: we acquired bulk crystals from two different available suppliers, we tried two types of metallic contacts, and tested the benefits of using or not annealing conditions. Ti and Pd were the two metal contacts initially considered for contacting WSe₂. From a rigid band analysis, the Pd work function (5.22 eV) stays close to the valence band of WSe₂ (5.15 eV), while Ti (4.33 eV) stays in between the valence band and conduction band (3.53 eV). An initial guess would lean towards Ti as the best contact for an ambipolar FET. The WSe₂ bulk crystals were acquired from HQGraphene [133], and from a group with expertise in the CVD growth of TMDs, from Valencia, Spain. The thermal treatment condition considered was an annealing in a thermal oven at 300 °C for three hours, high-vacuum (10⁻³ mbar), and in a 100:5 sccm Ar:H₂ atmosphere.

The devices were prepared following blue tape exfoliation approaches, and the electrical characterization was done on the Lakeshore probe station using two-point measurements. Figure 5.1 shows a monolayer WSe₂ FET on SiO₂, with respective AFM scan, and optical microscope images of the two different bulk crystal sources of WSe₂.

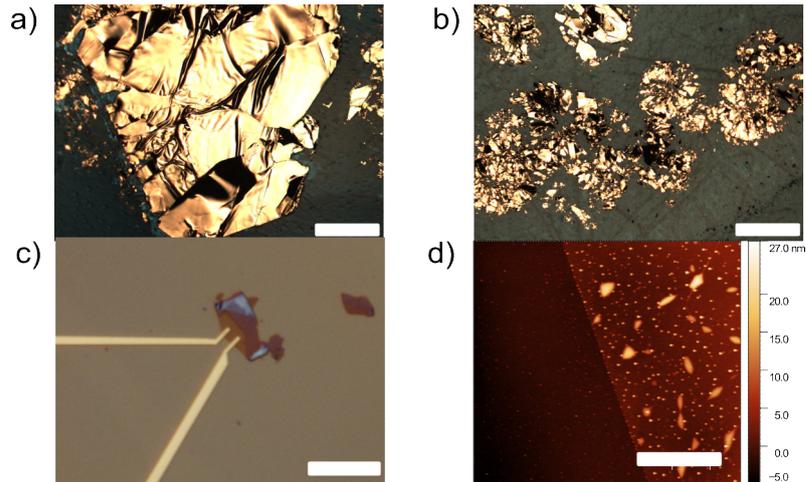


Figure 5.1 a) and b) Optical microscope images of the WSe₂ bulk crystals as received from HQGraphene and from Valencia, respectively. Scale bar: 500 μm . c) Optical microscope image of one of the monolayer WSe₂ FET on SiO₂ (250 nm-thick) fabricated to assess the role of supplier, metal contacts, and annealing conditions. Scale bar: 10 μm . d) High resolution AFM imaging of one WSe₂ flake on SiO₂ for the determination of the layer thickness. The brightest spots are bubbles of accumulated material below the flake. Scale bar: 1 μm .

We fabricated three monolayer WSe₂ FETs for each of the four combinations of two metal contacts with two materials sources, making up for a total of 12 devices fabricated. The devices would then be characterized electrically before and after annealing. Figure 5.2 shows a comparison between the transfer curves at RT of monolayer WSe₂ FETs using Ti and Pd contacts, before and after annealing, for HQGraphene crystals.

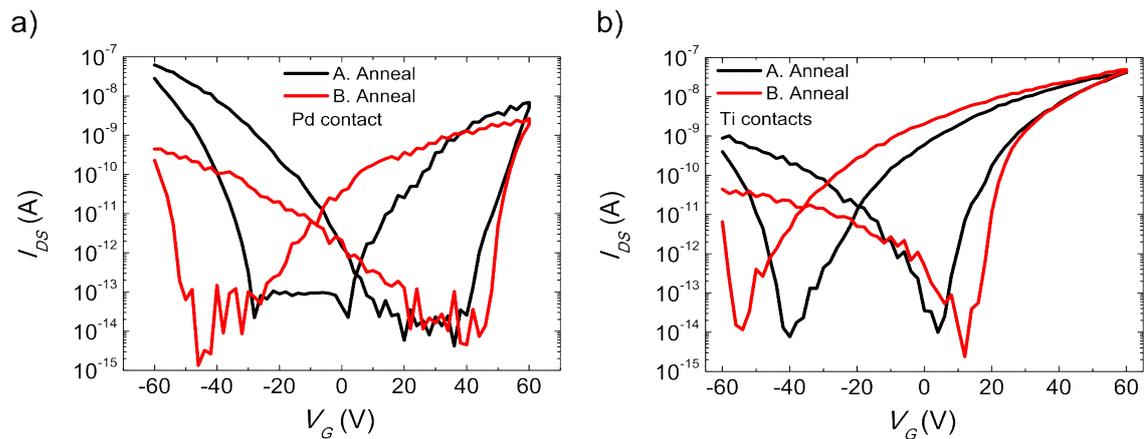


Figure 5.2 Drain-source current, I_{DS} , as a function of back gate voltage, V_G , for WSe₂ FETs made of HQGraphene crystals, at RT. $V_{DS} = 1$ V. a) Transfer curve for the FET using Pd contacts before and after annealing. b) Transfer curve for the FET using Ti contacts before and after annealing. Leakage currents at the 10^{-13} A level.

The gate voltage, V_G , sweeps were done at a rate of $\sim 0.05 \text{ V s}^{-1}$, starting at -60 V , with 60 seconds to set the first measurement. Comparing Figure 5.2 a) and b) one can see that the transfer curves of WSe_2 on SiO_2 exhibit wide hysteretic behavior for both Pd and Ti contacted WSe_2 , and that the annealing condition narrows it. Whereas before the annealing the hole-onset for the trace and the hole-onset for the re-trace are $\sim 70 \text{ V}$ apart, after the annealing this value decreases to $\sim 50 \text{ V}$ for both cases. The hysteretic behavior arises from trap states between the substrate and the channel, and from impurities on top of the channel, although at this point we cannot state about their relative contributions. Although for proof of principle devices one sweep direction might be enough to claim an ambipolar device operation, considering both sweep directions the device performance is not in a suitable position for reliable applications. The Pd contacted FETs show similar current levels for electron conduction and hole conduction, while Ti contacted FETs show a more asymmetric transfer curve, with electron transport dominating. Since the effective mass of holes and electrons in monolayer WSe_2 has been determined to be similar ($0.45 m_0$) [176], the observed symmetric ambipolarity for Pd, and less so for Ti suggests that the surface states of WSe_2 pin the work function of the metals at lower values. The field-effect mobility for both holes and electrons, μ_{FE} , was calculated employing the relationship $\mu_{FE} = \frac{L}{C_G V_{DS} W} \left(\frac{dI_{DS}}{dV_G} \right)$, where L is the channel length, W the channel width, C_G gate capacitance per unit area, and $\frac{\partial I_{DS}}{\partial V_G}$ the rate of change of I_{DS} with V_G . Since the transfer curves exhibited large hysteresis, we did the calculation of the hole and electron mobility for trace and re-trace conditions. Table 5-1 summarizes the field-effect mobility determined for the palladium contacted device, using a 250 nm-thick SiO_2 dielectric, with capacitance per unit area of $1.38 \times 10^{-4} \text{ F m}^{-2}$.

Table 5-1 Field-effect mobility for the Pd contacted device, using HQgraphene flakes (Fig. 5.2 a)).

	μ_{FE} , holes ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)		μ_{FE} , electrons ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	
	Trace	Re-trace	Trace	Re-trace
No annealing	1×10^{-3}	2.1×10^{-3}	1.6×10^{-3}	2.8×10^{-2}
Annealing	4×10^{-1}	4×10^{-2}	3×10^{-1}	7×10^{-2}

The annealing condition increases the field-effect mobility by roughly one order of magnitude, with both holes and electrons exhibiting similar values.

Due to the strong hysteretic effects, we will henceforth take the maximum value from the trace and re-trace as the mobility value for each carrier type. Figure 5.3 summarizes the average (3 devices for each condition) μ_{FE} obtained for electrons and holes for Pd and Ti contacted monolayer WSe₂ FETs, from both suppliers, before and after annealing.

With the intention of maximizing the performance of the hole transport in the WSe₂, Figure 5.3 allows us to conclude that the optimum combination was obtained for the annealed HQgraphene WSe₂ FETs with Pd contacts. At the same time, it was also the combination that showed more symmetrical ambipolarity. For this reason, the devices fabricated for the rest of this work consider these three conditions.

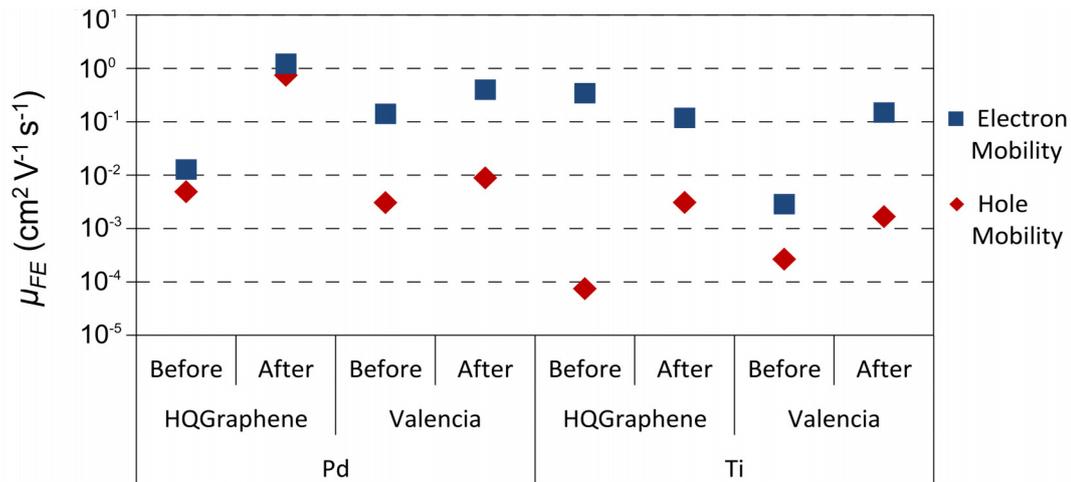


Figure 5.3 Summary plot of the average μ_{FE} for the WSe₂ devices fabricated on 250 nm-thick SiO₂ substrates. Conditions tested: metal contact (Pd, Ti); material source (HQgraphene, Valencia); and before/after annealing.

5.2 vdW heterostructures

In TMDs and other 2D vdW materials, water trapped between the substrate and the channel has been pointed as one of the significant sources of hysteretic effects [74]. Several approaches have been developed to encapsulate 2D vdW channels with insulating layers to reduce the presence of trapping sources using water-free fabrication

processes, as plasma enhanced chemical vapour deposition and atomic layer deposition. Alternative routes using encapsulation with other 2D materials has also been demonstrated to lead to a strong decrease of such effects [23], where the strong vdW repulsions between adjacent 2D layers ensure an interface clean of impurities [177]. In this regard, BN was first proposed as a substrate dielectric for high-quality graphene applications [23] and has been already explored in several device architectures for WSe₂ [59]. Engineering devices by stacking 2D materials vertically or laterally with other 2D materials comes then as a natural step towards heterostructures free from disorder and impurity induced trap states.

Trap states arising at the interface between the dielectric and the channel, at the bulk of the material, and at the top surface screen the field-effect, slowly driving drain-source currents away from its maximum value, resulting in large current decays and wide hysteresis in the trace and retrace of the transfer characteristics. For device applications at room temperature this feature is highly undesirable. In this section, we study how the performance of Pd contacted WSe₂ FETs improves changing the dielectric/WSe₂/top interfaces. We do so comparing three device architectures: I) SiO₂/WSe₂, II) SiO₂/WSe₂/BN, and III) SiO₂/BN/WSe₂. Note that in these devices we used HQgraphene WSe₂ crystals, and annealed according to the conditions stated in the previous section.

Figure 5.4 a), c) and e) show an optical microscope image of the devices explored, with corresponding transfer curves, Figures 5.4 b), d), f), measured at room temperature for a drain-source voltage of 1 V. All the measurements were taken starting at a $V_G = -60$ V, sweeping up to 60 V and back to -60 V, with a 60 second gate charging delay for the first measurement at $V_G = -60$ V. As before, the transfer curve for the Pd contacted annealed WSe₂ bilayer on SiO₂ (Figure 5.4 b)) exhibits wide hysteresis and similar levels of current of holes and electrons. The electron and hole mobility achieved are in line with the $1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ obtained in the previous section. The SiO₂/WSe₂ device, before and after placing the BN top layer show, for a channel length $L = 4 \text{ }\mu\text{m}$ and width $W = 9 \text{ }\mu\text{m}$, clear ambipolar behavior, with mobility for holes and electrons of approximately, 0.02 and 0.4, 2 and 0.1 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. With BN as a substrate, device III shows a one order of magnitude increase to 3 and 14 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

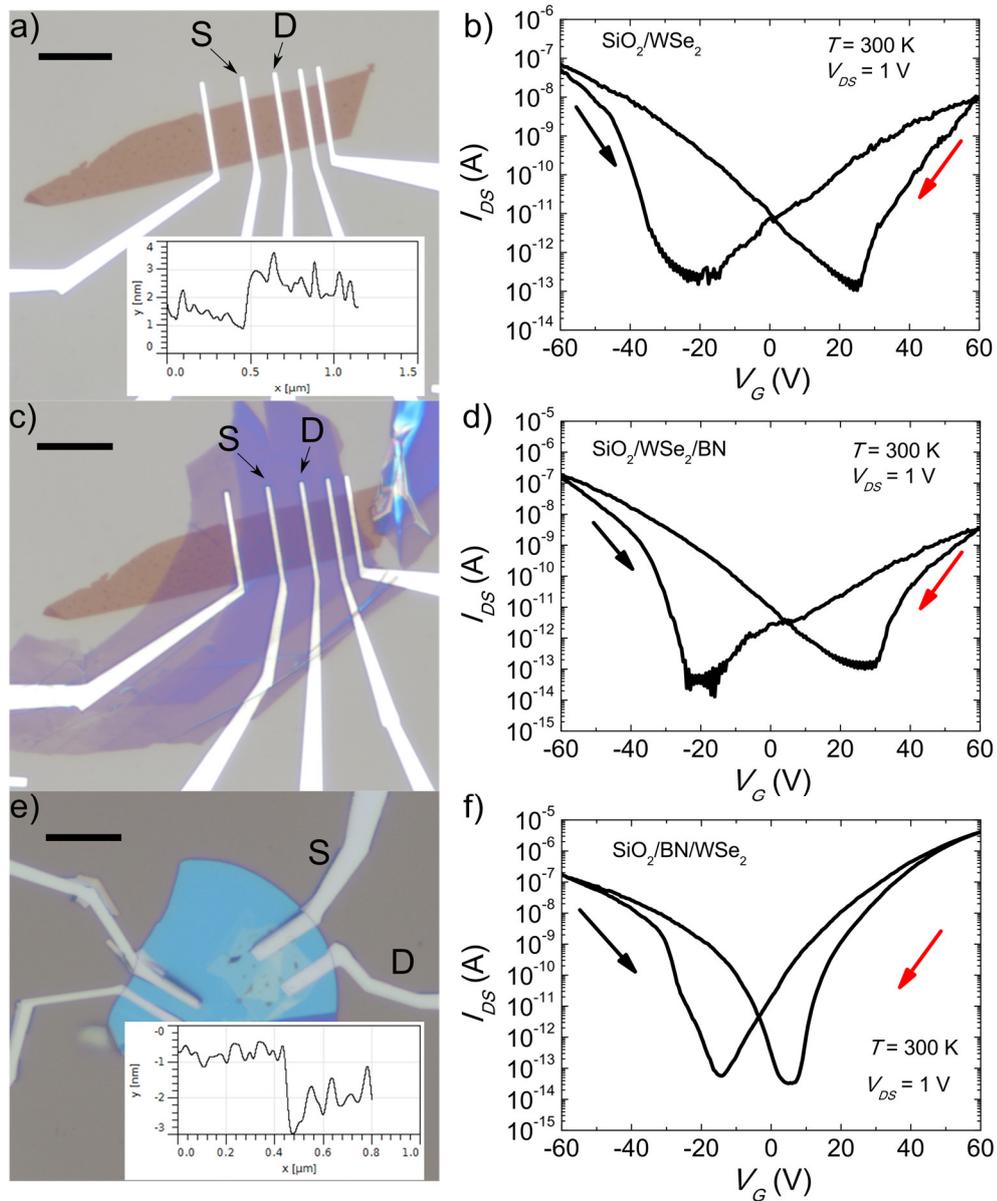


Figure 5.4 Bilayer WSe₂ flakes on SiO₂ and on BN substrates, with respective determination of the bilayer thickness using AFM. Pd (50 nm-thick contacts). a) and c) refer to the same flake, with c) showing the result of placing a 15 nm-thick BN top layer using deterministic transfer. Inset: AFM of the WSe₂ bilayer. Scale bar: 10 μm . e) Bilayer WSe₂ flake placed on top of a 60-nm thick BN flake, using deterministic transfer procedures. Inset: AFM of the WSe₂ bilayer. Scale bar: 10 μm . b), d), f) Respective transfer curves. Black and red arrows indicated the trace and re-trace directions. S, D refer to the source and drain electrodes used for the two-point measurements.

For the calculation of μ_{FE} for the device using the 60 nm-thick BN substrate, the effective capacitance per unit area was determined using an in-series model of the capacitance, according to the expression $C_T = C_{SiO_2} C_{BN} / (C_{SiO_2} + C_{BN})$, where C_T is the

total capacitance per unit area, and C_{SiO_2} and C_{BN} the individual capacitance per unit area of the SiO₂ and BN dielectrics, calculated as $\epsilon_0\epsilon_r/d$, where ϵ_0 is the vacuum permittivity, ϵ_r the dielectric constant, d the dielectric thickness, and e is the elementary charge. The mobility values are largely underestimated due to the nature of the two-probe measurement method and for the low doping regime in which the study is being employed.

The ON/OFF ratios at best are of the order of 10^6 , 10^7 , and 10^8 , for device I, II, and III, respectively, with corresponding SS of 3.3 V/dec, 2.5 V/dec, and 2.9 V/dec, respectively. Comparing device I and II, it can be seen that placing the BN on top lead to an increase of 2 times in current magnitude for the hole side, and a decrease of 3 times in current magnitude for the electron side, most likely due to the small doping shift of 10 V. Device III shows a substantially lower hysteresis, with the different between the trace and re-trace hole-onset (ΔV_{G_h}) only 20 V apart, although the current levels are only significantly higher in the electron side. Table 5-2 summarizes the performance of the three devices.

Table 5-2 Figures of merit for the performance of the SiO₂/WSe₂, SiO₂/WSe₂/BN, and SiO₂/BN/WSe₂ devices.

		SiO ₂ /WSe ₂	SiO ₂ /WSe ₂ /BN	SiO ₂ /BN/WSe ₂
Mobility (cm ² V ⁻¹ s ⁻¹)	Holes	0.02	2	3
	Electrons	0.4	0.1	14
ON/OFF		10^6	10^7	10^8
SS (V/dec)		3.3	2.5	2.9
ΔV_{G_h} (V)		60	50	20

5.2.1 Transient decay and hysteretic effects

The presence of trap states in a FET using a semiconducting channel manifests via hysteresis effects in the transfer curves, or in the transient decay of the electrical current driven by a drain-source bias. Due to the fabrication processes and the thinness of the channel, 2D vdW materials on oxide substrates are known to exhibit wide hysteretic effects [74], [177], [178]. Figure 5.5 compares the trace and re-trace of the

transfer characteristics starting from a gate voltage of -60 V up to 60 V at an average rate of 0.05 V s⁻¹, at room temperature and at cryogenic temperatures, of device III.

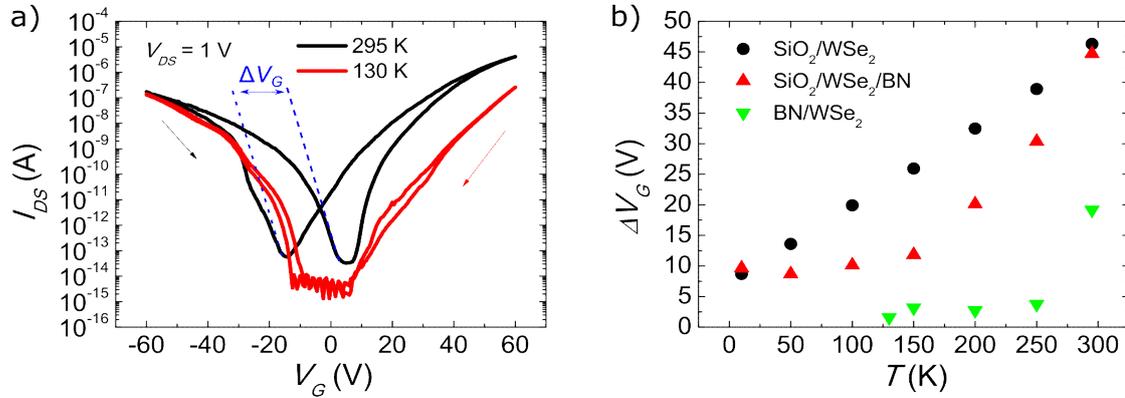


Figure 5.5 Hysteresis in WSe₂ FETs. a) Trace and re-trace transfer curve of the BN/WSe₂ device at 295 K and 130 K. b) Difference of the hole on-set for the trace and retrace curve as a function of temperature, for the three devices explored.

Trapped charge lifetimes and population have a strong dependence with temperature. Electrons gain energy from thermal excitations, increasing the probability of leaping into the trap states induced by the substrate or other sources. Lower temperatures should therefore decrease the probability of electrons getting into the trap states, effectively increasing the characteristic time scales of the current decays. For the qualitative analysis of the thermal activation of the trap states, we defined the width of the transfer curve as the difference between the onset gate voltage of the hole current for the trace and re-trace curves, ($\Delta V_{G_h} = V_{TH_h}^{Re-trace} - V_{TH_h}^{Trace}$). We could estimate with a 5% error margin the onset thresholds based on a linear fitting of the slope. Figure 5.5 b) shows the dependence with temperature of ΔV_{G_h} for the three studied devices. All devices exhibit a strong decrease with temperature, with the WSe₂ device on SiO₂ showing a linear dependence with temperature. When covered with BN, the device exhibit a stronger dependence with temperature, but still exhibits strong hysteretic effects. Changing the substrate from SiO₂ to BN seems to be the most efficient way to reduce the trap states, showing already at 250 K a strongly suppressed hysteresis width of 4 V.

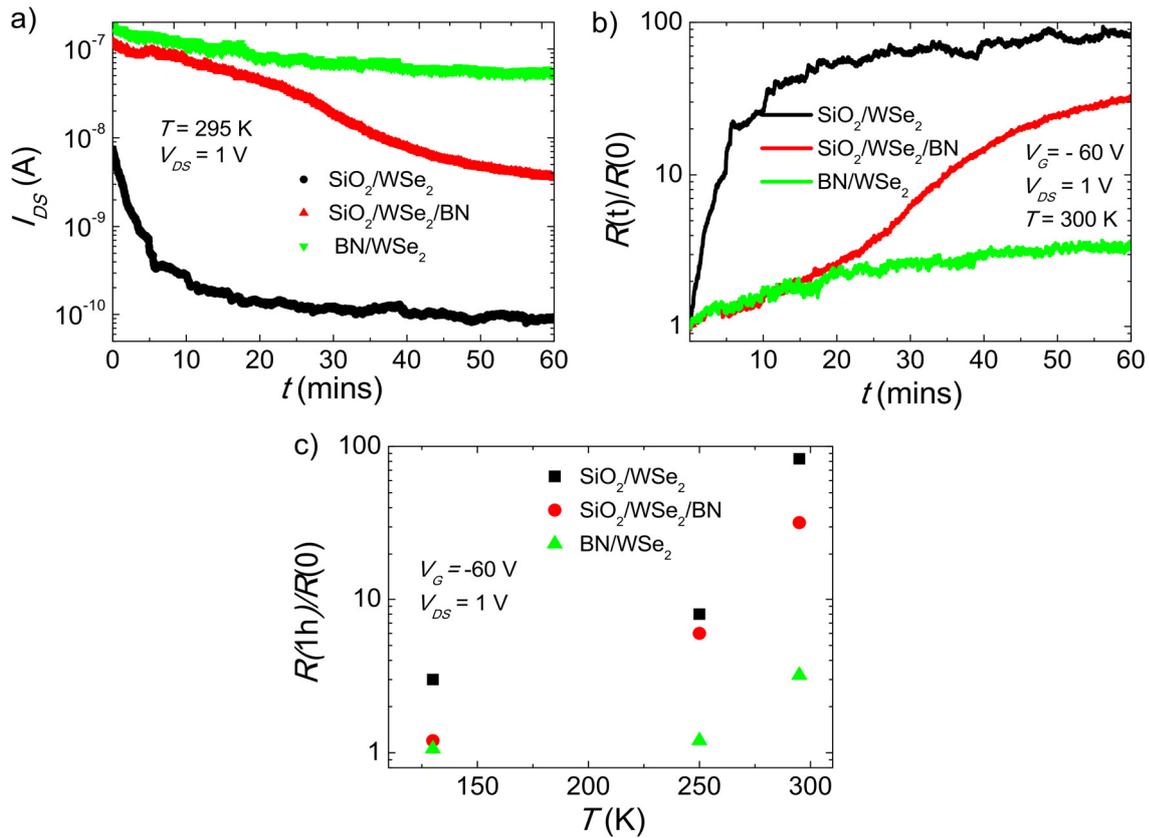


Figure 5.6 a) Dependence of the drain-source current with time at a gate voltage of -60 V, at room temperature for the three devices. b) Normalized time dependence of the resistance. c) Dependence of the normalized resistance after 1 hour with temperature for the different devices.

If instead of sweeping the gate voltage we fix it and record the current driven in the channel, the charging of the trap states will lead to a decay of the current. The time dependence of the driven I_{DS} across a channel under constant V_{DS} and V_G is related to the decrease of the carrier density in the TMD channel. This reduction is proportional to the trapped population. Due to the different sources of trap states, the fitting of the trapping process to a transient decay exponential should consider the contribution of different lifetimes. For this reason, the time dependence of the drain-source current should be expressed as a series of exponential decays, expressing quicker and slower trapping processes. The exponential time dependence of the current is characterized with a time constant connected with the RC constant of the capacitor modelling the trap states. In recent works in TMDs, the transient decay of currents has been explored using bi-exponential relationships, where the current, I , is given as, $I = I_0 + I_1 \exp(-t/\tau_1) + I_2 \exp(-t/\tau_2)$ [74], [178]. Typical time constants of strongly hysteretic MoS₂

transistors on SiO₂ were reported in the range of 500 to 1000 s [74]. Larger time constant are associated with slower population and de-population of trap states, and ideally should be as long as possible. Figure 5.6 a) shows the time dependence of the current driven for the three devices at $V_G = -60$ V, and $V_{DS} = 1$ V, at room temperature.

In our devices, we found that in most cases a single exponential curve would fit the data, indicating a dominating single-type trap source driving the hysteretic effects. Table 5-3 summarizes the time constants extracted. Although there was no clear dependence with the temperature for each individual device, comparing between devices allows us to see lower time constants for the SiO₂/WSe₂ device, with the BN/WSe₂ device being the one with the longer relaxation constants, across all temperatures. By placing the BN top layer, the relaxation time constants are significantly increased.

Table 5-3 Time constants extracted fitting the current transient decays with a bi-exponential function for the three devices at different temperatures.

	295 K		250 K		130 K	
	τ_1 (s)	τ_2 (s)	τ_1 (s)	τ_2 (s)	τ_1 (s)	τ_2 (s)
SiO₂/WSe₂	72 ± 0.3	382 ± 5	445 ± 10	-	218 ± 2	-
SiO₂/WSe₂/BN	1035 ± 7	-	1093 ± 64	-	816 ± 24	-
BN/WSe₂	1026 ± 6	-	1451 ± 47	-	956 ± 59	-

The temperature dependence of the transient decays become more apparent if we evaluate the ratio between the resistance after 1 hour, $R(1h)$, and the resistance at $t = 0$, $R(0)$. Figure 5.6 b) and c) show the resulting plot as a function of time and temperature, respectively. While the device on SiO₂ show a large change in resistance, almost of 2 orders of magnitude, placing the BN top lowers this effect to 20 times the initial resistance. The BN device clearly shows the highest stability by exhibit an increment of resistance by a factor of 2. Compiling this information together with the exponential time constants determined we can see that the trend is for more stable devices to have larger time constants. Comparing the relative impact of the different placement of the BN layer either as a substrate or as a capping layer, allow us to conclude the larger contribution for a device operation free from disorder and trap states by using the BN as a substrate.

5.3 Conclusions

In this chapter, we optimized the fabrication of WSe₂ devices on SiO₂ and studied its characteristics engineering the top and bottom interfaces with BN. First, we tested the devices fabricated on SiO₂ for two metal contacts, two material suppliers, and two annealing conditions. We concluded the Pd contacted and annealed devices to be the highest performing devices, with hole mobility reaching 0.3 cm² V⁻¹ s⁻¹, ON/OFF ratios of 10⁶, and subthreshold swings of 3.3 V/dec. The devices fabricated on the oxide substrate exhibited wide trace and re-trace hysteresis that were not addressed by annealing the device.

We then studied the impact of having BN layers on top and on the bottom interface of the WSe₂ channel. By using BN as a substrate, the maximum hole mobility increased to 3 cm² V⁻¹ s⁻¹, the electron mobility to 14 cm² V⁻¹ s⁻¹, the ON/OFF ratio to 10⁸, while the subthreshold swing kept in similar values. This increase of the figures of merit of the device was accompanied by a strong decrease in the trapping effects at RT. The lifetimes of the trap states exhibited a strong dependence with temperature, with the placement of the BN top and bottom layer greatly affecting the transient decay of the current.

Overall, the best performing devices were fabricated on BN, with RT characteristics greatly improved when compared to those on SiO₂.

Chapter 6

Nonlocality in CVD graphene macro-to-microscale devices

In recent years, the pursuit for the full-electrical generation, manipulation, and detection of the various charge carrier degrees of freedom in the context of post complementary metal oxide semiconductor technologies (post-CMOS) lead to the development of non-local geometries [94], [98], [99], [101], [102], [179]. Non-local measurements have become an attractively simple and powerful spin transport characterization tool in non-magnetic materials. In graphene, the strong enhancement of non-local signals at the charge neutrality point (CNP) has been associated to several demonstrations of magnetic-element-free generation, transport, and detection of spin currents. The detection of spin signals in graphene using H-bar non-local approaches free of magnetic elements has been demonstrated by using extrinsic sources of spin-orbit coupling [98], [99], [101], strong exchange coupling via proximity effect to ferromagnetic insulators [179], and by applying an external magnetic fields [102], although the demonstrations via extrinsic sources of SOC have been contested by Wang, and Kaverzin [180], [181]. The prediction of spin transport in such conditions has been mainly exploring spin diffusion in the spin Hall regime. In the spin Hall regime, the spin Hall effect (SHE) and inverse spin Hall effect (ISHE) are used to generate and detect, respectively, the spin currents. So far, the considered mechanisms capable of driving the enhancements of non-local signals close to the Dirac point in graphene are the extrinsic sources of SOC, Zeeman spin Hall interaction, and proximity-induced strong-exchange bias, explored in Ref. [96], [182]–[184],[185], [186].

The experimental realizations rely on microscale Hall bars of pristine or CVD graphene channels with sizes easily ranging several micrometers, limited by the

microscale spin relaxation lengths. In order to demonstrate that mechanisms other-than-charge are responsible for the nonlocality, these techniques rely on comparing the exceeding non-local signal to the classical charge diffusive background, and studying its dependence with channel geometry.

In this chapter, we demonstrate that external magnetic fields applied to CVD graphene Hall bars lead to large non-local signals that persist for devices at the millimeter and micrometer scale, and that they closely follow the same dependence with the device aspect ratio (L/W) for geometries that differ by two orders in magnitude. We exclude possible sources of spin or valley transport due to the length scales involved, and propose that the same mechanisms present in the macroscale devices is driving the signal in the microscale samples. Considering the strong asymmetry of the non-local magnetoresistance, and the microscopic details of the fabricated samples, we suggest the large non-local signals to be driven by dissipative, shunted counterpropagating edge states, mediated by grain boundaries. These results imply that additional care should be taken when attributing non-local signals in solid state devices to the diffusive transport of spin or valley currents.

6.1 Fabrication, device scheme, and measurement.

Both millimeter and micrometer scale devices were fabricated following the same procedures, with recipes described in detail in chapter 3. The devices were fabricated on $1 \times 1 \text{ cm}^2$ Si (n⁺⁺ doped)/SiO₂ (300 nm) substrates with monolayer CVD graphene film wet transferred on top, acquired from Graphenea S.A.. The devices were then spincoated with DL PMMA. The Hall bar shape of the samples was defined exposing the surrounding area with EBL, and etching with Ar:O₂ RIE. The remaining resist leftovers were striped in a cold acetone bath for 4 hours, immersed in IPA, and dried with a nitrogen gun. The sample was again spin coated with DL PMMA, and the metal pads defined on the Hall bar. The metallization was done on a UHV system for the deposition of Ti (5 nm)/Au (40 nm) contacts. The lift-off was performed in cold acetone.

Figure 6.1 shows a sketch of the macroscale and microscale devices studied in this chapter with respective dimensions and measurement schemes.

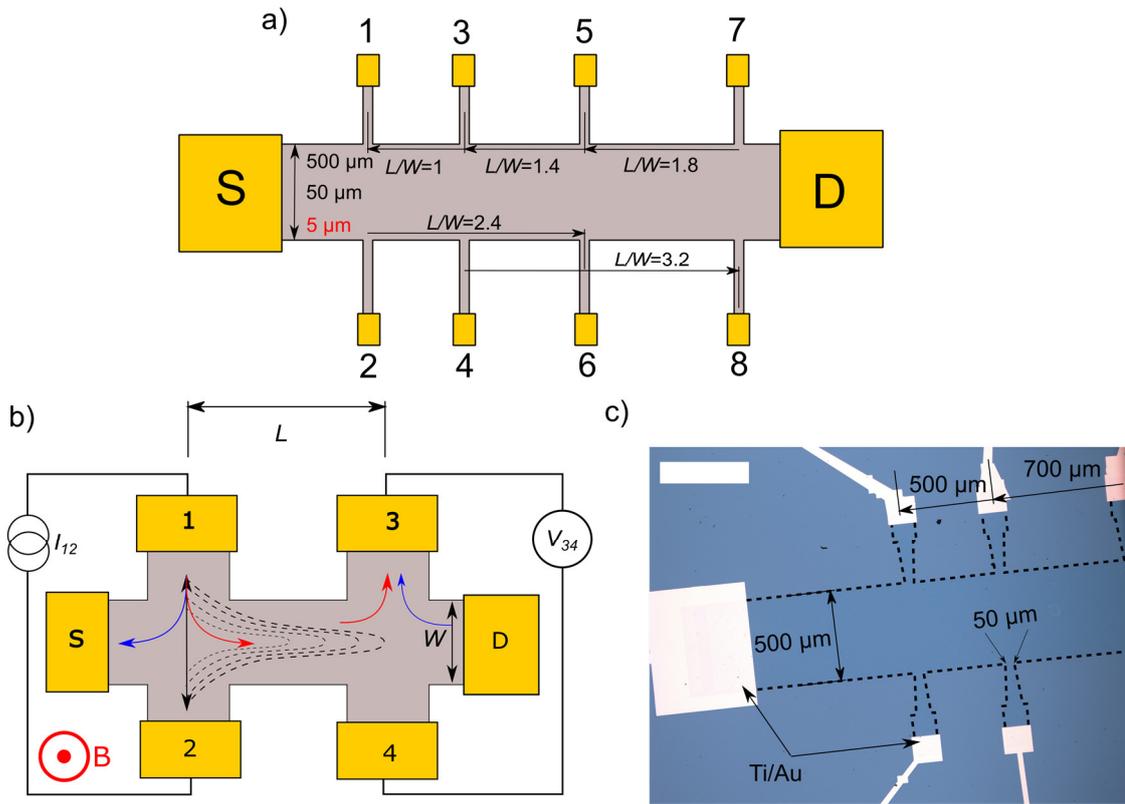


Figure 6.1 a) Sketch of the macroscale and microscale devices. b) Measurement scheme for $L/W = 1$. The non-local resistance, R_{NL} , for the set of electrodes shown is defined as $R_{NL} = V_{34}/I_{12}$. The blue and red arrow represent spin “up” and “down” transport in the spin Hall regime. The black dashed lines represent the van der Pauw contribution to the non-local signal detected between probes 3 and 4. c) Optical microscope image of the macroscale CVD graphene device. White scale bar: 500 μm .

In our work, we explored CVD graphene devices 5, 50, and 500 μm -wide, with center-to-center distance between terminals maintaining similar aspect ratios (L/W) of typically 1, 1.4, 1.8, 2.4 and 3.2. The width of the terminals was kept at $1/10^{\text{th}}$ or less of the channel width. The data shown in this chapter has been confirmed for a total of six devices.

The measurement of non-local signals in the spin Hall regime consists of injecting a current in one arm of a H-bar shaped channel with the voltage detection being made at the other arm (see Figure 6.1 b)). Using the terminals shown in Figure 6.1 b), the non-local resistance for this electrode combination is determined as $R_{NL} = V_{34}/I_{12}$. In one arm of the H-bar a transverse spin current will be generated from the charge current via spin Hall effects, and will diffuse across the channel to be converted into a charge current via inverse spin Hall effect. The magnitude of the non-local signals

will depend on how efficient is the spin-to-charge conversion, and on the spin relaxation length. Following a transmission line method measurement of the non-local signal [187] both the spin Hall angle and spin relaxation length can be determined. The non-local signal dependence with channel length is given as $R_{NL} = \frac{1}{2} \theta_{SH}^2 \rho_{xx} \frac{W}{\lambda_s} \exp\left(-L/\lambda_s\right)$, where θ_{SH} is the spin Hall angle, ρ_{xx} the sheet resistance, and λ_s the spin diffusion length. Since the strong nonlocality of graphene is observed around the Dirac point, one has to use electrostatic gating to modulate the Fermi level of graphene to the charge neutrality point.

There are other sources of non-local signals not related to spin transport, these effects must be excluded as origin. The classical charge-related source of nonlocality that contributes to the signal being detected between terminals 3 and 4 (see Fig. 1a) is the van der Pauw current spreading from the injecting terminals. By injecting a current on the left-arm a net current will reach the detection terminals, with magnitude decreasing exponentially with the distance to the injecting terminals. This Ohmic contribution in the device scheme presented is determined using the expression, $R_{NL,Ohmic} = \frac{\rho_{xx}}{\pi} \ln \left[\frac{\cosh(\pi L/W)+1}{\cosh(\pi L/W)-1} \right]$, which for cases where $L > W$ is usually approximated as $R_{NL,Ohmic} \approx \frac{4}{\pi} \rho_{xx} \exp\left(-\pi \frac{L}{W}\right)$. The sheet resistance is determined by performing a four-probe measurement of the respective channel, injecting a current between electrodes S and D, and measuring the voltage drop between electrodes 2 and 4, or 1 and 3. The terminals 1/10th or less width requirement comes from a straightforward analysis of the van der Pauw expression for charge diffusive backgrounds, where if the width of the contact is on the same order of the channel width it can lead to edge-to-edge signals ~ 20 times in magnitude larger than the center-to-center signal. By comparing the detected non-local signals versus the expected non-local Ohmic contribution we can evaluate the emergence of signals not related to this classical source of nonlocality.

In our study, we have therefore to evaluate the non-local signals versus the expected Ohmic contribution under the same conditions for all samples. Throughout the manuscript, we keep the same relative orientation of the perpendicular external magnetic field applied and of the arm injecting and the arm detecting the voltage signal. Unless stated otherwise, the current excitation is of 10 μ A. We report mainly on the

results obtained for the extreme cases of 5 and 500 μm -wide devices, using the data of the 50 μm -wide devices to extend the discussion.

6.2 Macroscale devices

6.2.1 Electrical characterization

The electrical measurements were made using Keithley 2636 dual channel for the two-point output characteristic.

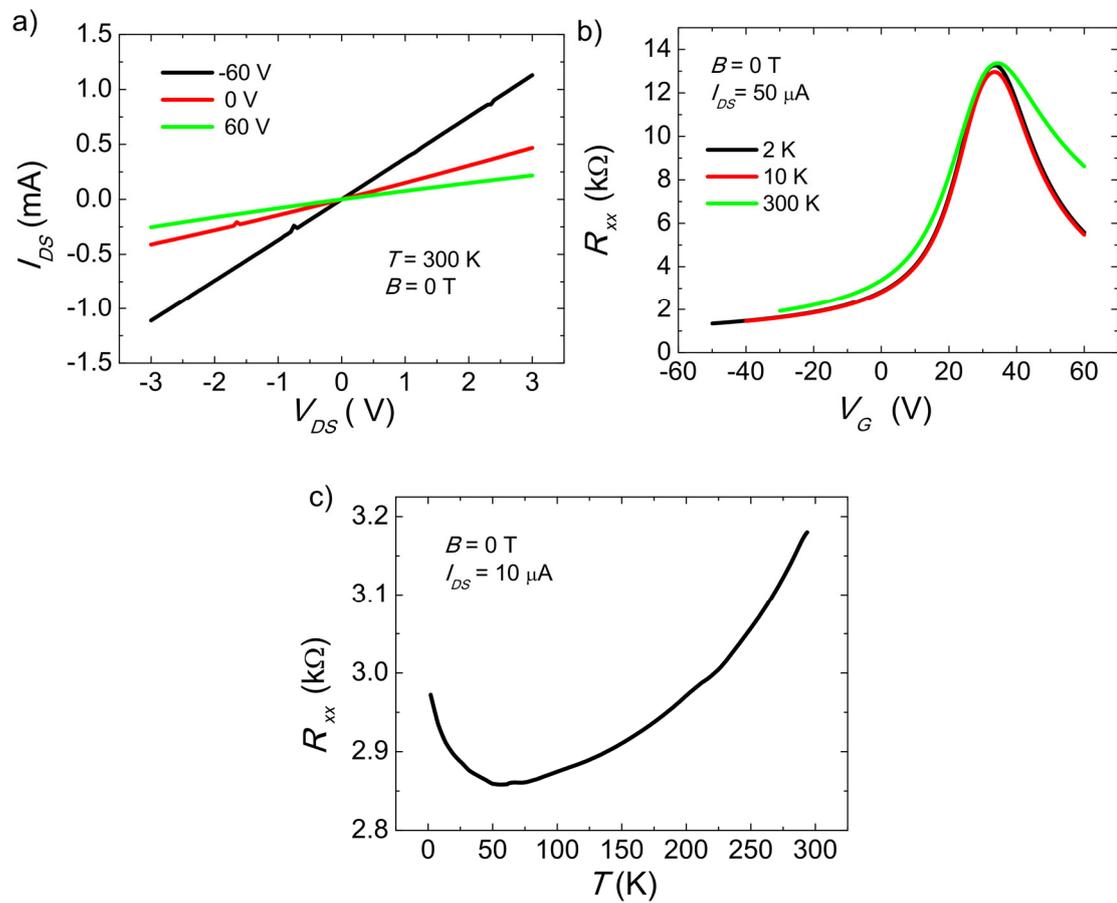


Figure 6.2 500 μm -wide sample. a) Two-point output characteristics at different gate voltages between the drain and source contacts at room temperature, showing Ohmic contacts. b) Four-point transfer curves ($L/W = 3$) at different temperatures. c) Temperature dependence of the four-point resistance at $V_G = 0\text{ V}$.

Due to the high conductivity of the graphene channels, the transfer characteristics were measured using the Keithley 6221/2182 current source and nanovoltmeter setup both in two-point measurements and four-point measurements,

with the gate voltage being applied by the Keithley 2636. Figure 6.2 shows the electrical characterization of the 500 μm -wide macroscale device. Before measuring the devices, we performed an in-situ annealing at 400 K, with helium purging cycles to release the sample chamber of evaporated water. After 3 hours, we would seal the chamber and cool down the sample. This procedure would impact the doping levels of the CVD graphene samples, decreasing the gate voltage required to reach the CNP by 25-40 V. Figure 6.2 b) shows the two-point output characteristics of the drain and source contacts, defined as the two outmost contacts, as a function of the gate voltage at room temperature. The linear relationship between I_{DS} and V_{DS} indicates an Ohmic contact for all gate voltages.

Figure 6.2 c) shows the four-point transfer curve of CVD graphene ($L/W = 3$) at several temperatures, with charge neutrality point (CNP) at $V_G = 32$ V, ambipolar operation, and ON/OFF ratio of 7. For the determination of the field-effect mobility, we used the relationship $\mu_{FE} = \frac{1}{C_G} \frac{L}{W} \frac{\partial G}{\partial V_G}$, where $G = 1/R_{xx}$ is the conductance, C_{ox} is the gate geometrical capacitance per unit area, $C_{ox} = \epsilon_0 \epsilon_r / d$, with ϵ_0 , ϵ_r being the vacuum and relative permittivity, and d the dielectric thickness. For $d = 300$ nm and $\epsilon_r = 3.9$, the gate capacitance was determined to be 1.2×10^{-4} F m^{-2} . At room temperature, the CVD graphene Hall bar had a mobility of 2325 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, increasing to 2875 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ at 2 K. The sheet resistance at the CNP for $L/W = 3$ and room temperature was $R_{\square} = 4410$ Ω . Figure 6.2 d) shows the temperature dependence at $V_G = 0$ V, with the sample showing metallic behavior down to 50 K, down from which an upturn would be visible due to weak-localization effects [188].

To determine the intrinsic carrier density and its dependence with temperature we performed Hall measurements to the CVD graphene Hall bar at $V_G = 0$ V.

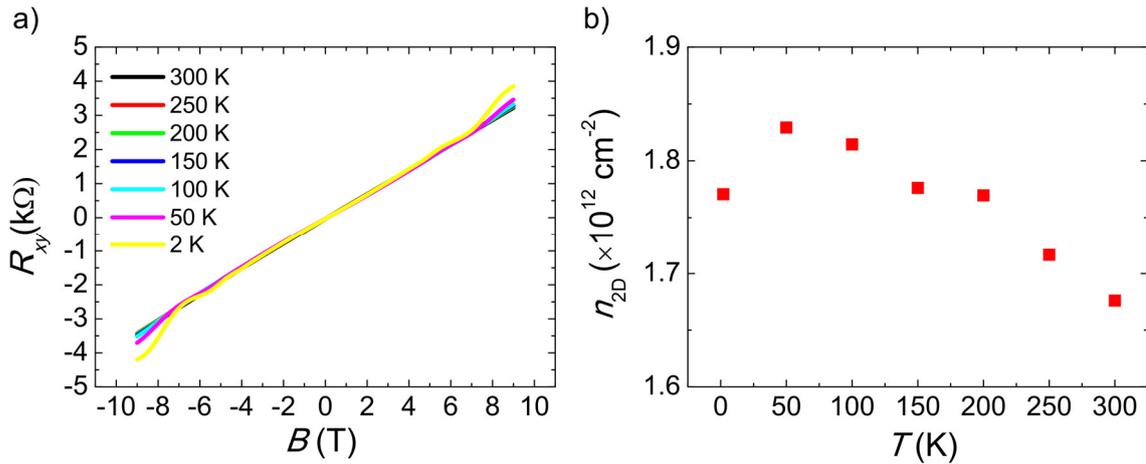


Figure 6.3 Hall measurements of the CVD graphene macroscale Hall bar. a) Transversal resistance, R_{xy} , as a function of magnetic field applied perpendicular to the surface of the channel for different temperatures. b) Determined intrinsic carrier concentration at $V_G = 0$ V, as a function of temperature.

Figure 6.3 shows the transverse resistance, R_{xy} , measured as a function of magnetic field. From 300 K to 100 K, the measurements are mainly linear for the whole -9 to 9 T range of magnetic fields explored, nearly superimposing on each other, with a small continuous decrease of the slope. At 50 K and below, the Hall measurements show anti-symmetric oscillations of the transverse resistance at the highest fields. Extracting the slope of the curves within a range of -1 to 1 T, we plotted in Figure 6.3 b) the dependence with temperature of the carrier density determined. The carrier density was determined from the expression $n = I / R_{HE}$, where R_H is the slope of the $R_{xy}(B)$ plot in the referred ranged. The Hall mobility at 2 K was determined to be $\mu_H = R_H / R_{\square} = 875 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $V_G = 0$. Unlike in chapter 4, the intrinsic doping can be directly determined at $V_G = 0$ V due to the high conductivity and doping. With the charge neutrality point standing at $V_G = 32$ V, we can estimate the effective gate capacitance to be 80% of the geometrical capacitance, in-line with the results obtained in Chapter 4 for MoS_2 transistors.

6.2.2 Magnetotransport properties

When a perpendicular magnetic field is applied to a channel of graphene, the electrons will undergo cyclotron orbits. For sufficiently large magnetic fields, the bulk will become insulating and the transport will be occurring mainly through the edges,

where the skipping orbits lead to a net circulation. These edge states survive in graphene devices up to large scales, and together with the quantization of the cyclotron orbits (Landau levels), lead to the QHE.

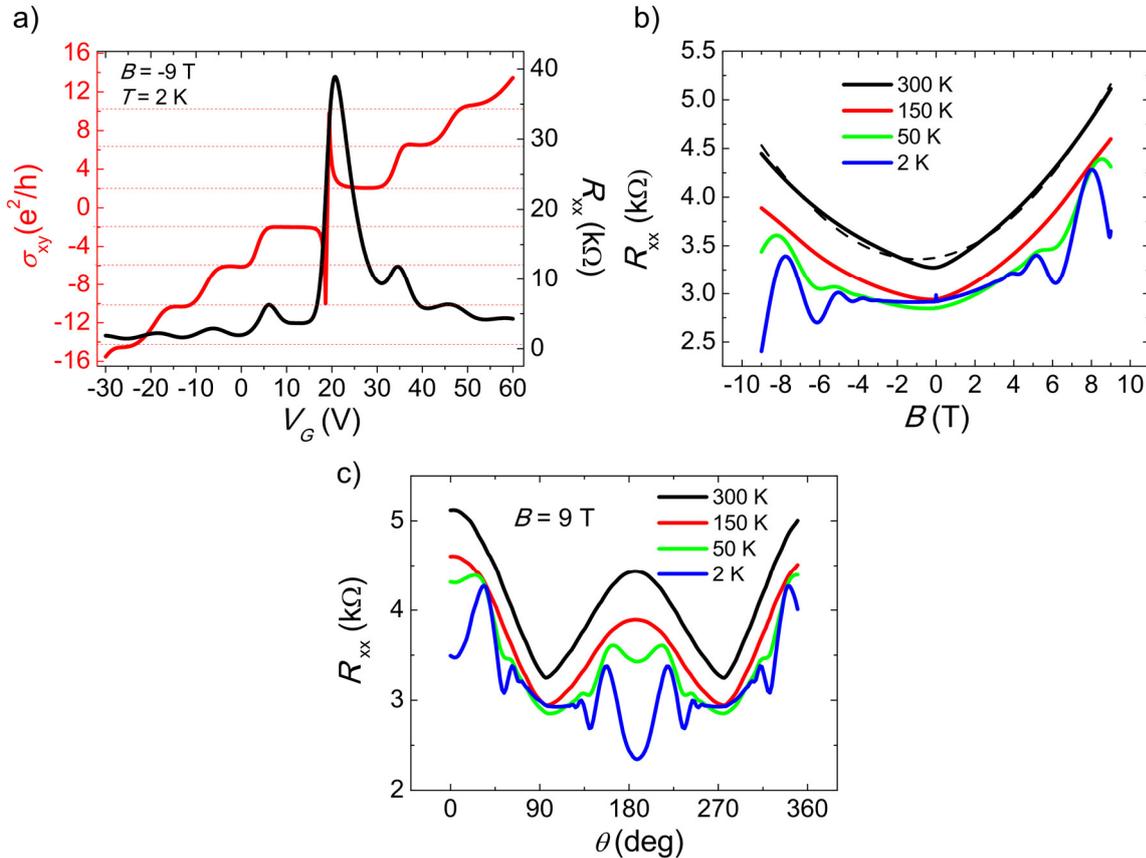


Figure 6.4 a) Transversal conductivity and longitudinal resistance as a function of the gate voltage, for an external magnetic field of -9 T applied perpendicular to the sample surface, at a temperature of 2 K ($L/W = 3$). b) Longitudinal resistance with $V_G = 0$ V as a function of the magnetic field, for different temperatures. Dashed-line: fit to B^2 with slope considered. c) Angular dependence of the magnetoresistance for different temperatures at a fixed external magnetic field of 9 T and $V_G = 0$ V.

Figure 6.4 a) shows the transversal sheet conductance, σ_{xy} , and the longitudinal four-point resistance, R_{xx} , as a function of the magnetic field applied perpendicular to the surface of the sample for the case $L/W = 3$. In Figure 6.4 a) σ_{xy} is determined directly from the transversal resistance measurements, $\sigma_{xy} = 1/R_{xy}$, and exhibits conductance plateaus at $\pm 2, \pm 6$, and ± 10 e^2/h . These plateaus correspond to the half-integer Quantum Hall Effect of graphene, namely to $i = 0, 1$, and 2 , according to $\sigma_{xy} = \pm 4(i + 1/2) \frac{e^2}{h}$. The longitudinal magnetoresistance shows a main resistance peak at the CNP of 37 $k\Omega$, with consecutive peaks aligned with the change between conductivity plateaus,

corresponding to the location of the Landau levels. While the chemical potential (controlled via the gate voltage) is in between the Landau levels, the longitudinal resistance is not 0, showing that the bulk is not truly insulating and exhibits finite conductivity, likely due to the low-mobility of the CVD graphene samples.

Figure 6.4 b) shows the temperature dependence of the four-point longitudinal magnetoresistance of the graphene channel. At room temperature, the graphene shows a large maximum magnetoresistance, $MR = \frac{R_{xx}(B) - R_{xx}(0)}{R_{xx}(0)}$, of 71%, with a slightly asymmetric B^2 dependence of the longitudinal resistance, down to 150 K.

Although the CNP is at $V_G = 32$ V, both branches of the magnetic dependence show some linearity that can be attributed to the two-type carrier OMR [189]. Below that temperature, the magnetic dependence exhibits slight oscillations of the magnetoresistance, superimposed with the quadratic background. At 2 K, this signature has fully developed into Shubnikov de Haas oscillations, with a narrow weak-localization peak showing up between -30 mT and +30 mT. The angular dependence shows in a different way the same observations, with the OMR contribution at high-temperatures leading to a $\cos^2(\theta)$ angular dependence of the resistance. The slight magnetoresistance asymmetry observed in Figure 6.4 b) leads to the angular dependence showing a peak at 180 degrees with magnitude smaller than at 0 and 360 degrees. For decreasing temperatures, the SdH oscillations superimpose the OMR at 50 K, fully developing at 2 K.

6.2.3 Non-local measurements

For the non-local measurements, we compare the measured non-local signals, $R_{NL} = \frac{V_{NL}}{I}$, with the signals of Ohmic origin by considering the expression, $R_{NL,Ohmic} = \frac{\rho_{xx}}{\pi} \ln \left[\frac{\cosh(\pi L/W) + 1}{\cosh(\pi L/W) - 1} \right]$. Figure 6.5 shows the main results regarding the detection of non-local signals in a CVD graphene Hall bar on SiO₂ under magnetic fields applied perpendicular to the surface of the sample for the $L/W = 3$. Figure 6.5 a) shows the dependence of the non-local resistance of the macroscale device with the gate voltage at a temperature of 2 K. For increasing magnetic fields, the non-local signal detected at the CNP greatly increases, when compared to the non-local signal far away from the CNP,

which remains roughly the same. Fixing the magnetic field at -6 T and changing the temperature (Figure 6.5 b)), we can see that the non-local signal decays between the temperature range of 2 and 12 K, and then saturates up to 100 K, surviving up to room temperature. Figure 6.5 c) summarizes the magnitude of the non-local signal at the CNP as a function of magnetic field for different temperatures, while showing the determined Ohmic contribution measured for the same conditions.

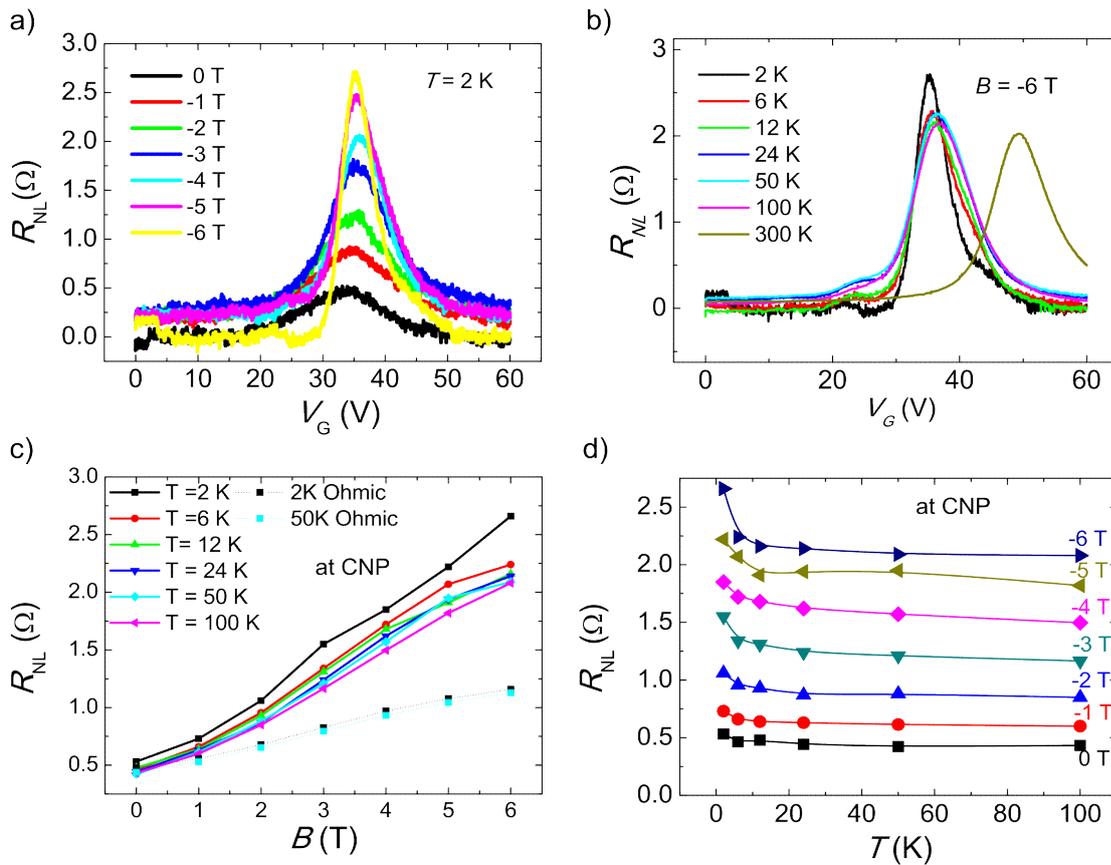


Figure 6.5 Non-local resistance of the macroscale device for $L/W = 3$. a) R_{NL} as function of the gate voltage for different magnetic fields at a fixed T of 2 K. b) R_{NL} as a function of gate voltage for different temperatures for a fixed magnetic field of -6 T. c) Dependence of R_{NL} at the CNP of graphene with the magnetic field B , with respective ohmic contribution, at several temperatures. d) R_{NL} at the CNP as a function of temperature for different magnetic fields.

With increasing magnetic field, the relative difference between the non-local signal and the Ohmic contribution increases, clearly indicating a magnetic field dependent generation of an exceeding contribution to the total non-local signal. Figure 6.5 d) shows for different magnetic fields the non-local signal at the CNP as a function

of temperature, with the sharp increase at the lowest temperatures, similar to what has been reported for high-mobility pristine microscale graphene samples.

To clarify the dependence of the exceeding non-local signals with the distance between injecting and detecting terminals, Figure 6.6 shows the resulting plot of the non-local signal at the CNP for a magnetic field of -6 T as a function of the distance between terminals, compared with the measured and determined Ohmic contribution for all cases.

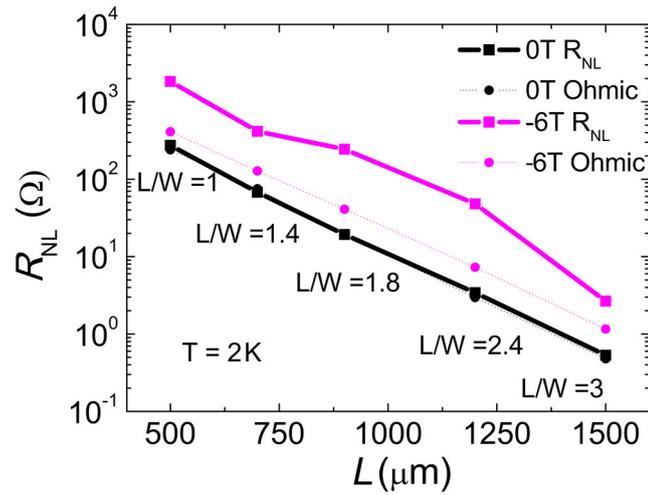


Figure 6.6 Non-local resistance of the macroscale device as a function of the distance between terminals at the CNP and 2 K, summarized for the magnetic fields of 0 T and -6 T. Ohmic contributions determined measuring the longitudinal resistance, R_{xx} , and employing the exact solution for each respective case and condition.

For all cases, at 0 T, the Ohmic contribution and non-local signal closely follow each other, indicating that in the absence of an external field, the detected non-local signals are due to the current spreading into the graphene channel. Once the magnetic field is turned on, reporting specifically for -6 T, and even though the system is still without a fully developed QHE, we can see that the Ohmic contribution is greatly overcome, in some cases by signals one order of magnitude higher. These signals can be extremely large for the shorter distances, as is the case for $L/W = 1$, where the expected Ohmic contribution (for a magnetic field of -6 T) is of $\sim 400 \Omega$ and the detected values are of 2000Ω . Following Ref. [97] and [102] for the Zeeman induced spin Hall effect in graphene, we can estimate the spin Hall coefficient at the CNP for $B = -6$ T from the non-local measurements following the expressions, $R_{NL} = \frac{1}{2} \theta_{SH}^2 \rho \frac{W}{\lambda_s} \exp(-L/\lambda_s)$ [190]. Fitting the data in Figure 6.6, we found a $\theta_{SH} = 1.6 \pm 0.4$,

with $\lambda_s = 163 \pm 19 \mu\text{m}$. The relaxation length is two orders of magnitude higher than what is usually reported for CVD graphene on SiO_2 lateral spin valves, where the non-local signals originate from the spin diffusion across the graphene channel. Also, the spin Hall angle overcomes that of Pt, which is the metal known to have the largest spin Hall angle of 0.2, and has a magnitude larger than 1, indicating that If we compare the characteristic length obtained with the equivalent characteristic decay from the Ohmic term $\propto \exp(-\pi L/W)$, where the prediction is $\lambda_{\text{theo}}^{\text{Ohmic}} = W/\pi \sim 159.2 \mu\text{m}$, and the result obtained was $\lambda_{\text{Exp.}}^{\text{Ohmic}} = 159.4 \pm 1.6 \mu\text{m}$. The anomalously large characteristic length suggests that the large non-local signals are associated with a source other than spin transport.

Although this plot is only shown for the specific temperature of 2 K, it holds true for the other tested temperatures. The origins of the non-local signal will be discussed further on, in section 6.4.

6.2.3.1 In-plane magnetoresistive effects.

In previous works, where exceeding non-local signals were induced by external sources of SOC, as hydrogen adatoms or proximity-induced via WS_2 , the spin origin of the signals has been tested at the microscale using Hanle measurements adapted to geometry of the devices. Hanle measurements in lateral non-local graphene spin valves consist in applying a magnetic field perpendicular to the sample to manipulate the spin orientation and modulate in this way the detected non-local signal, serving as a proof of the spin transport along the channel. In H-bar geometries free of magnetic elements, the applied magnetic field must be parallel to the direction of the injected current, and will therefore lay in plane with the samples surface, perpendicular to the channel orientation. For a flat graphene surface perfectly aligned with the external magnetic field, the magnetoresistance is predicted to show no dependence with the magnitude of the magnetic field, and therefore the Ohmic contribution to the non-local signal measured should also exhibit no dependence. By changing the direction of the applied magnetic field from perpendicular to the surface to parallel to the surface, the perpendicular contribution of the OMR should decay, leading to a characteristic $\cos^2(\theta)$ angular dependence. Figure 6.7 a) shows the angular dependence of the non-local signal of the

CVD graphene macroscale devices at the CNP for $L/W = 1.8$, applying a magnetic field of 0.5 and 1 T, well below the magnetic fields required for graphene to enter the QHE regime, where the angular dependence gets influenced by the SdH oscillations (as seen in Figure 6.4 c)). The data has been anti-symmetrized for the angular dependence following the relationship $R_{NL}(\theta)|_B = (R_{NL}(\theta)|_{+B} + R_{NL}(\theta)|_{-B})/2$.

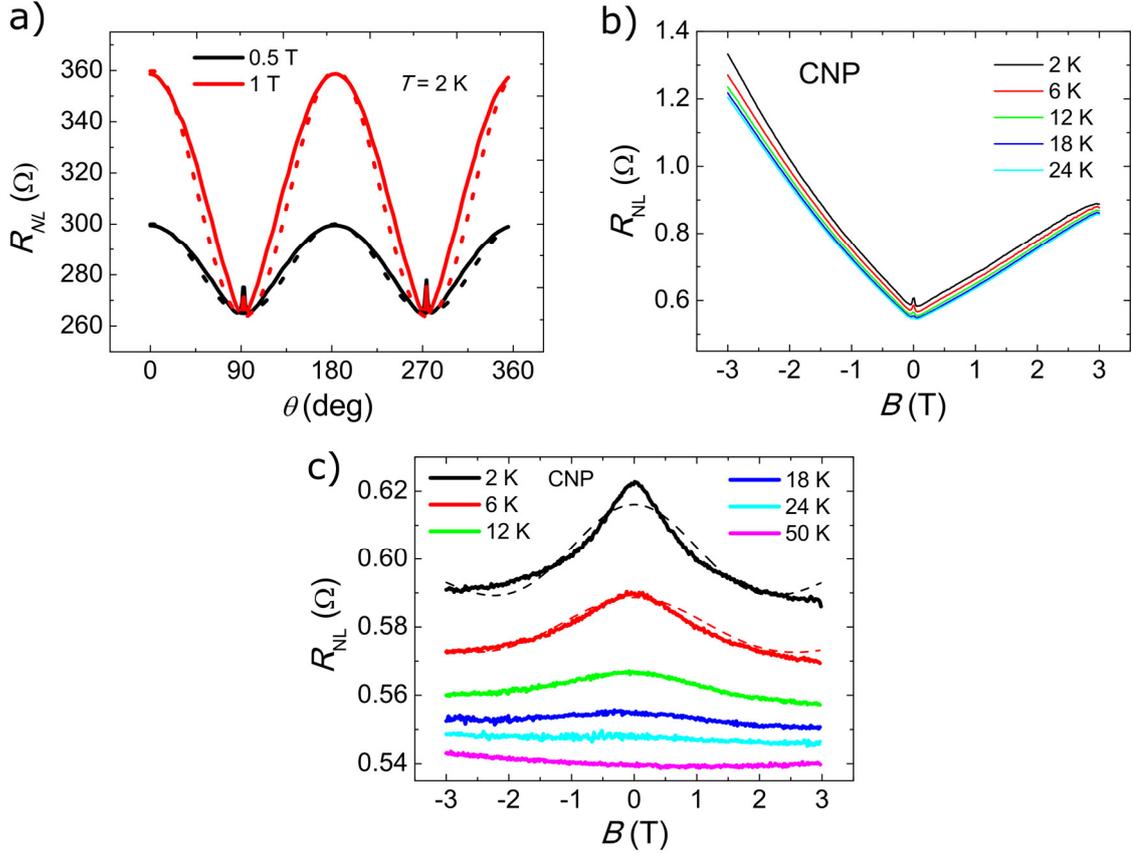


Figure 6.7 a) Angular dependence of the non-local resistance at CNP for $L/W = 1.8$, at 2 K, for $B = 0.5$ T and 1 T. Dotted lines are $\cos^2(\theta)$ fits. b) Dependence of the non-local signal at CNP for $L/W = 3$ with magnetic field perpendicular to the surface, where the weak localization feature is still detectable. c) Non-local resistance at CNP as a function of the in-plane magnetic field, exhibiting Hanle-like features. Dashed lines: fit to the non-local in-plane magnetoresistance model.

When the magnetic field is perpendicular to the normal of the surface, a peak shows up that we attribute to the weak-localization ohmic contribution. Testing it for $L/W = 3$, the weak-localization feature is still perfectly visible when we apply the magnetic field perpendicular to the sample and sweep the magnetic field, (Figure 6.4 b)). It is also confirmed in the local measurements with the temperature dependence (Figure 6.2 c)) emerging at temperatures below 50 K. Interestingly, for higher magnetic

fields, the weak-localization feature seemed to decrease with decreasing magnetic fields, suggesting a magnetic field dependence of the in-plane non-local magnetoresistance. In Figure 6.7 c) we plot the non-local signal as a function of the in-plane magnetic field for different temperatures (for $L/W = 3$), and see a Hanle-like signature at the lowest temperatures that quickly suppresses for increasing temperatures, in-line with the temperature dependence shown in Figure 6.2 c). According to what has been reported in other literature, the emergence of this signal, even if only at cryogenic temperatures, should be connected with spin transport. Fitting the data at 2 K to the expression [96] $R_{NL} = \frac{1}{2} \theta_{SH}^2 \rho W \operatorname{Re}[(\sqrt{1 + iw_B \tau_s / \lambda_s}) \exp(-\sqrt{1 + iw_B \tau_s / \lambda_s}) L]$, with θ_{SH} and λ_s as unknowns, the fitting outputs $\theta_{SH} = 0.28 \pm 0.08$ and $\lambda_s = 144 \pm 12 \mu\text{m}$. Although the model fits the data, suggesting this signal to be of spin origin would be accepting that spins generated at the injection terminals could cross a 1500 μm -long channel without decohering. Since for the out-of-plane measurements the weak-localization is extremely narrow, occurring between -30 mT to 30 mT, we suggest the possibility of the magnetoresistive effect emerging from small unavoidable sample misalignments, which allow for the ohmic contributions from the longitudinal resistance to emerge in the supposedly in-plane magnetoresistance effects. By considering a misalignment of 0.5 degrees, which is inside the experimental error of the rotator discrete steps together with the placement of the sample manually in the puck, the width of the weak localization dependence would go from the -30 to 30 mT to -3.5 to 3.5 T, which seems to fit well to our case. The emergence only at cryogenic temperatures and its quick decay with temperature are strongly correlated with the data we have for the weak localization effect, suggesting that the Hanle-like feature are caused by small unavoidable experimental inaccuracies that lead to a weak-localization contribution to the “in-plane” magnetoresistive measurements.

6.3 Microscale CVD graphene devices

6.3.1 Electrical characterization and magnetotransport

To further extend our study, we studied the non-local signals emerging in samples two orders of magnitude smaller, on pair with what has been reported in other works (with channels widths ranging 0.5 to 5 μm).

Figure 6.8 a) shows the optical microscopic picture of the etched graphene 40 μm -long Hall bar with 10 contacts, with associated dimensions, and corresponding preliminary electrical characterization.

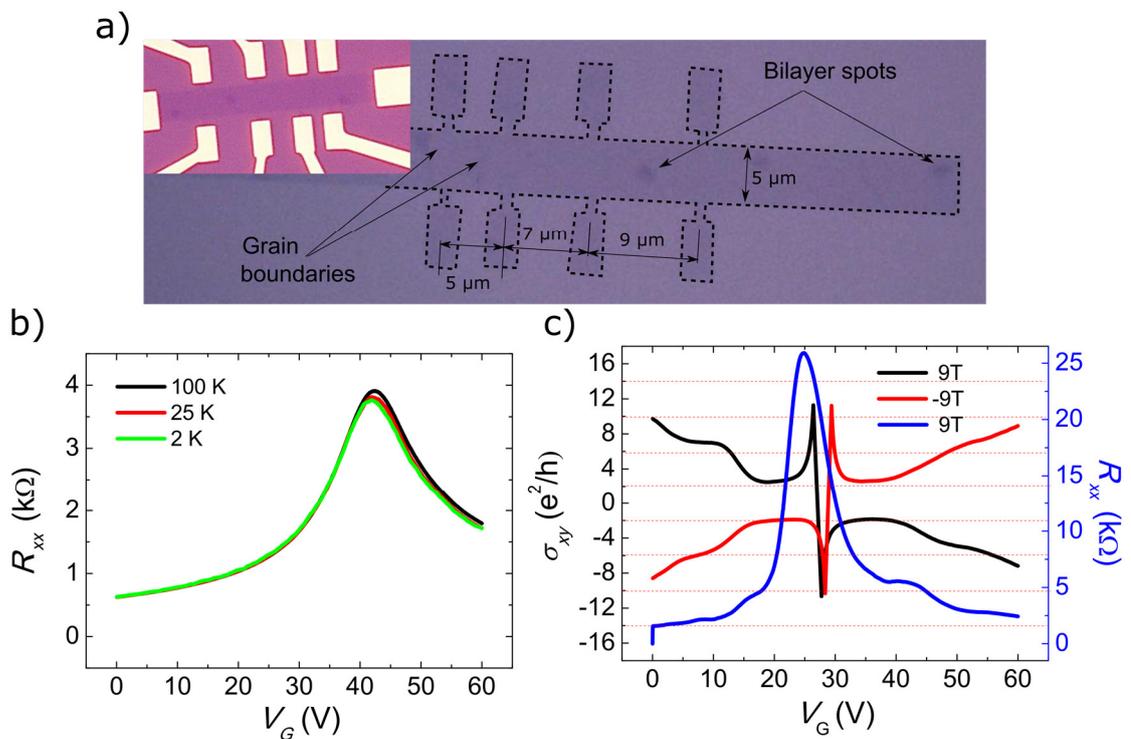


Figure 6.8 a) Microscale CVD graphene device on SiO_2 (300nm), after RIE with Ar/O_2 . Inset: with Ti/Au contacts. b) Transfer curve for $L/W = 1$ at different temperatures. c) Transversal and longitudinal resistivity as a function of gate voltage for a perpendicular magnetic field of 9 T.

Figure 6.8 b) shows the four-point transfer curves for $L/W = 1$ as a function of temperature, with CNP at 40 V. Due to the limitation of the number of contacts that can be attached to the puck, measurements between electrodes at different distances required the samples to be warmed up to room temperature and re-wired. Placing the

samples back in the chamber would require additional in-situ annealing, with the outcome of each annealing showing some variations. For this reason, the measurements of the transfer curves show a CNP at 40 V, and the QHE shown in Figure 6.8 c) shows the CNP at 27 V.

The microscale sample shows a maximum field-effect mobility of $5420 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at the lowest temperatures, two times in magnitude the field-effect mobility of the macroscale device, although the sheet resistance at the Dirac point and 0 T is quite similar, $R_{\square} = 3957 \text{ } \Omega$. The QHE does not exhibit as many plateaus as the CVD graphene large sample even for the highest magnetic field accessible (9 T), with σ_{xy} plateaus at ± 2 and $\pm 6 e^2/h$, corresponding to the half-integer levels $i = 0$, and 1, according to $\sigma_{xy} = \pm 4(i + 1/2) \frac{e^2}{h}$.

6.3.2 Non-local measurements

The non-local signals in the microscale devices were characterized in a similar way to the macroscale ones. Figure 6.9 shows the non-local resistance measurements for the $L/W = 3.2$ aspect ratio. In Figure 6.9 a), the magnitude of the non-local signals at the CNP stands out from the magnitude reported for the macroscale device. The macroscale devices exhibited a non-local resistance at the CNP of $3 \text{ } \Omega$ at 2 K for $L/W = 3$, while the microscale device signal increases to $50 \text{ } \Omega$. Interestingly, the temperature dependence is more pronounced than the one observed for the macroscale devices at $L/W = 3.2$, although at room temperature the signal is still of $5.5 \text{ } \Omega$ (25 times higher than the equivalent ohmic background).

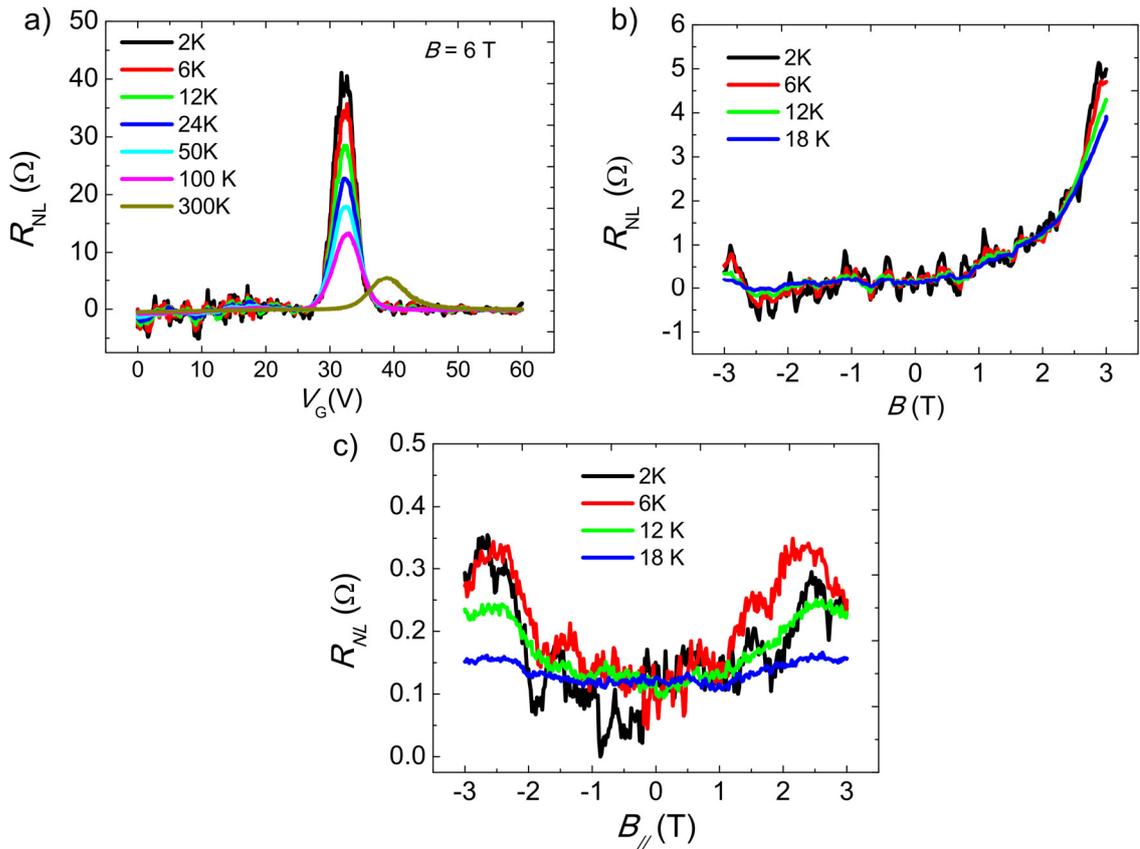


Figure 6.9 Non-local measurements for $L/W = 3.2$. a) Non-local resistance as a function of back-gate for different temperatures. b) Non-local resistance as a function of the perpendicular magnetic field at CNP for different temperatures. c) Non-local resistance as a function of the in-plane magnetic field for different temperatures at CNP.

In Figure 6.9 b) and c) we did not observe weak-localization effects in the non-local resistance dependence with magnetic field, both out-of-plane and in-plane. The absence of the weak localization in the out-of-plane magnetoresistance measurement and simultaneous absence of the Hanle-like in-plane signal, in the presence of non-local signals one order of magnitude higher than in the macroscale, supports even further our suspicions that the Hanle-like signal observed in the macroscale devices is related to the weak-localization and unavoidable experimental inaccuracies. One interesting feature of the microscale devices was the strong asymmetry of the non-local signal with the sign of the magnetic field, also observed in reference [102]. This observation will be further discussed in the next section.

Figure 6.10 summarizes the non-local resistance at the CNP as a function of the distance of the terminals for the microscale device.

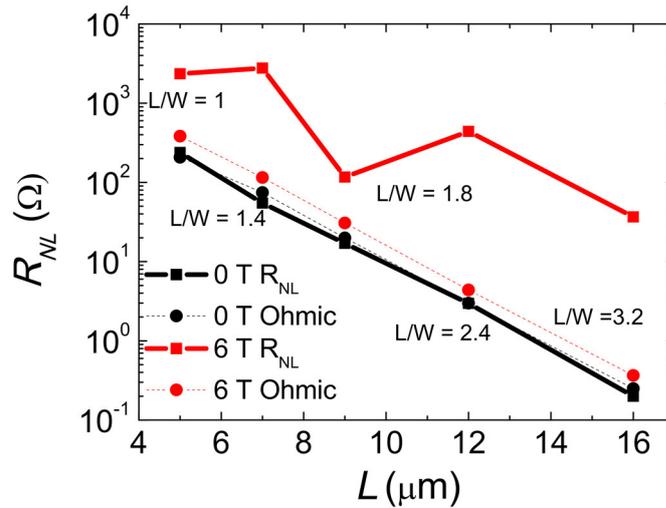


Figure 6.10 Dependence of the non-local resistance as a function of the distance between terminals for an external magnetic field of 0 T and 6 T, with the Ohmic contributions determined from the R_{xx} measurements under the same conditions.

The control measurements of the longitudinal resistance allowed us to extract the Ohmic contribution of the current spreading into the graphene channel. Even under a magnetic field of 6 T, the Ohmic contribution is orders of magnitude lower than the measured non-local resistance. In a similar way than done to the macroscale device, the exponential decay has characteristic length $\lambda = 2.7 \pm 1.2 \mu\text{m}$, while the ohmic contributions follows the expected decay for a $5 \mu\text{m}$ wide channel of $\lambda_{Theo}^{Ohmic} = W/\pi \sim 1.59 \mu\text{m}$, and experimental result $\lambda_{Exp}^{Ohmic} = 1.58 \pm 0.03 \mu\text{m}$. The discrepancy between λ and λ_{Exp}^{Ohmic} suggests an additional source to the non-local signal that emerges when the device dimensions get reduced, although it is not clear the origin. The spin Hall angle calculated for this case was $\theta_{SH} = 1.3 \pm 0.6$, smaller than the value obtained for the macroscale sample, but with higher uncertainty of determination.

6.4 Origins of the nonlocality

In a concluding manner, Figure 6.11 compares the results obtained between the macroscale device and the microscale device.

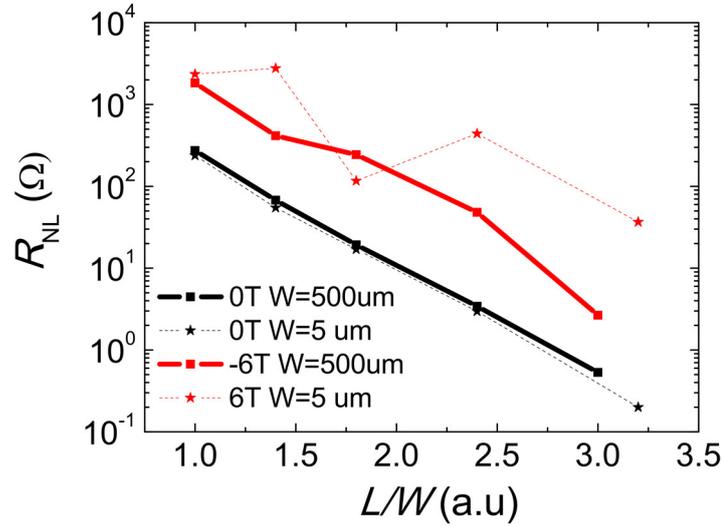


Figure 6.11 Summary plot of the dependence of the non-local signal with aspect ratio for the macro- and microscale device.

The semi-log plot shows that both devices have exponential decays with similar characteristic decays as a function of the aspect ratio, suggesting a connection between the non-local signal and the sample geometry. Scaling down the device increases the total signal, while the ohmic contribution strongly follows what's expected for both cases. After turning the magnetic field on, the interpretation of the data becomes less clear.

Regarding the origin of such signal, several works have proposed origins other than spin transport for the anomalously large non-local signals in microscale pristine graphene devices, namely Ref. [191]. In their work, they refer to a study of the non-local signal in samples 3 μm -long and 0.9 μm -wide where they explored the dependence of the ZSHE with the orbital (classical Hall effect) and total magnetic field dependence, expressed as $B_{tot} = \sqrt{B_{\perp}^2 + B_{\parallel}^2}$. While the ZSHE and inverse effect require an out-of-plane component to generate and detect the spin currents in the graphene channel, the Zeeman splitting does not have any orientation requirement, depending only on the magnitude of the applied magnetic field, B_{tot} . They show it by fixing the perpendicular

component of the magnetic field and sweeping the in-plane component, by which they could see a square dependence of the non-local signal with B_{tot} . Interestingly, they saw an additional offset term that could not be understood in the lines of the ZSHE. They introduced the Ettingshausen-Nerst and the Joule-Nerst effect as possible thermoelectric mechanisms for the generation and detection of non-local signals. While the non-local voltage generated via Joule-Nerst is a second order effect with the current, the Ettingshausen-Nerst is first order. In Ref. [191], the authors evaluated the first order and second order frequency response respective with a sinusoidal current excitation, and in this way they could separate each contribution. In our case, since we use a DC setup, we employed a delta-mode measurement technique that allows for non-local contributions from the Joule effects to be excluded from the measurements (described in chapter 3). Since the Ettingshausen–Nerst effect is linear with the injected current, Keithley’s delta-mode does not address it. In the Ettingshausen-Nerst effect a heat flow transverse to the injected current is generated via Ettingshausen effect ($\frac{dQ}{dt} \propto \frac{\partial T}{\partial x} = PB_z I_y$), where P is the Ettingshausen coefficient, dQ/dt is the heat flow and dT/dx is the thermal gradient generated at the injection terminal. The resulting non-local signal, R_{NL} , is generated from the Nerst effect, where a temperature gradient across the detection terminal and perpendicular to the magnetic field leads to $R_{NL} \propto \frac{dT}{dx} S_{xy} B_z$, where S_{xy} is the Nerst coefficient and dT/dx is the temperature gradient along the channel at the detection terminal. Previous studies have shown the thermoelectric properties of graphene to be relevant for the thermal generation of transverse voltages, with reported S_{xy} of $50 \mu\text{V K}^{-1}$ at the CNP for magnetic fields of 8 T [192]–[195]. Under high magnetic fields, S_{xy} also shows oscillating behavior with chemical potential, correlated with the QHE, and show a singularity at the CNP, where it is larger in magnitude. The dependence of the thermally induced non-local signal with distance between terminals is also not clear. While one could presume that the heat flow generated at the injecting terminal should be constant along the channel, which with homogeneous thermoelectric properties would generate a constant gradient throughout the channel and lead to a non-local signal invariant with channel length, the heat dissipation in nano and microstructures does not follow this most simple picture. Although the Ettingshausen and Nerst effect seems to be a strong contender for the origins of the signals observed in our samples, the dependence of the non-local resistance with the external magnetic field should be

quadratic, $R_{NL} \propto B^2$. This is clearly not the case in our samples, where the dependence of the non-local signal with magnetic field is strongly asymmetric.

In order to further clarify the data, we decide to repeat the experiment with a sample with dimensions in between 5 and 500 μm . With a 50 μm -wide channel, and equivalent aspect ratios between 1 and 3.2, the device is on the macroscale side, and should exclude spin-transport. Figure 6.12 a) summarizes the non-local signals at the CNP of graphene taken at $|B| = 6$ T, as a function of the channel aspect ratio, for all the device dimensions considered so far (5, 50 and 500 μm -wide channel). Figures

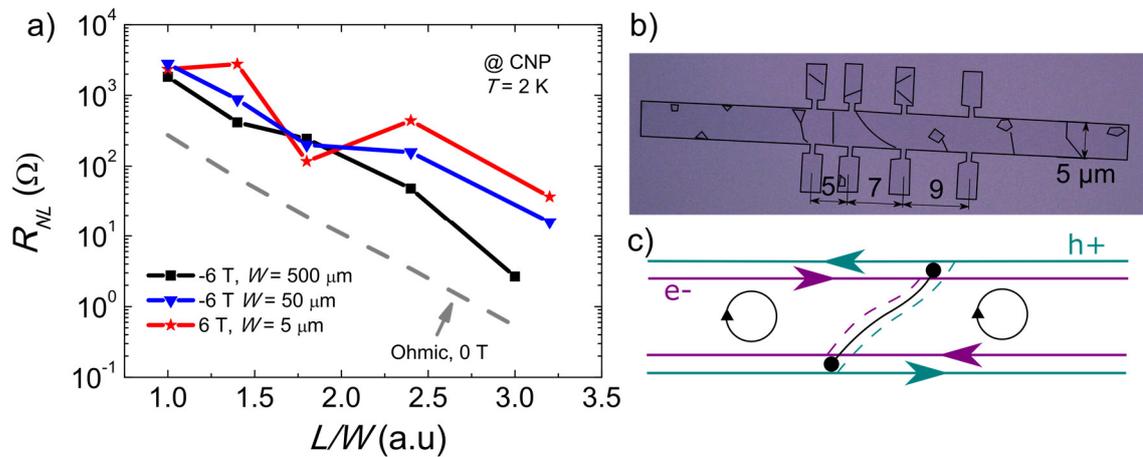


Figure 6.12 Non-local signal as a function of aspect ratio for the different devices. a) Non-local resistance as a function of aspect ratio for the Hall bars 5, 50, and 500 μm -wide. b) Optical microscope picture of the microscale Hall bar during the fabrication highlighting the visible grain boundaries and bilayer islands. c) At the CNP, and under an external field, the counterpropagating edge currents are coupled to the charge of the carrier via Zeeman interaction. The presence of the hole/electron asymmetric grain boundary shunting the edge states through the increasingly insulating bulk may lead to a decrease of the voltage drop at the detection electrodes.

The determined non-local signals for the 50 μm -wide sample are in between the results of the two other samples, with R_{NL} 1 to 2 orders of magnitude higher than what was expected from the Ohmic contribution. Importantly the magnitude of the non-local resistance is similar to the 5 μm -wide sample. For the 5 μm -wide sample, we still considered possible for spins to survive along the channel length. In this case, with a 160 μm -long channel, we exclude spin origins, but the magnitude of the signal is comparable.

The mechanism driving the non-local response must then be able to generate signals dependent with the magnitude of the external magnetic field, asymmetric with

B , seemingly invariant with scale, and that follow a dependence with channel length like a Ohmic background. While these conditions exclude the previous discussed sources (Zeeman spin Hall effect and Ettingshausen-Nerst effect), there is one source that qualitatively fits our description, which is the counterpropagating edge states shunted by grain boundaries.

Magnetic fields applied perpendicular to the surface of graphene will lead to a gradually more insulating bulk, with charge carriers flowing increasingly through the edges [18], [37], [196]. Strong external magnetic fields will result in a well-defined quantum Hall effect. At the Dirac point, the edge states develop into dissipative quantum Hall counterpropagating states [197]. The linear dispersion of graphene, at the CNP, and the Zeeman interaction result in the coupling of the charge type of the carriers and of the spin state, similarly to the Zeeman spin Hall effect [97]. Line defects, which in graphene can be seen as grain boundaries (inhomogeneous carrier distribution may also lead to similar effects), may shunt the opposite edges of the graphene channel, greatly changing the transport (Figure 6.12 b)) [198]–[200]. Not only so, but importantly, line defects in graphene show asymmetric electron/hole transmission [201]. In a non-local measurements scheme, and due to the fact that holes and electrons at the CNP and under a magnetic field are coupled to spin up and down states, respectively, the asymmetric hole and electron transmission through the line defect (grain boundary) will shunt the CVD graphene opposite edges only for one type of carrier (Figure 6.12 c)) [201], therefore leading to an asymmetric non-local signal with the external magnetic field. With transport happening mainly via the edge states, with (increasingly) insulating bulk, the non-local signal will follow a Ohmic like dependence with sample aspect ratio. These effects have been predicted using atomistic models in graphene nanoribbons, but the argument can be extended to larger scales [198], [199], [201]. Additionally, this feature would be independent of sample size, although the macroscale samples would average out the type of line defects, therefore showing more symmetric dependences with B , and even lower signals. Due to the random nature of the formation of inhomogeneities and grain boundaries during the growth of CVD graphene [198], [199], it would lead to cases of samples showing nonlocality for positive magnetic fields or for negative magnetic fields. This picture strongly fits to the plethora of effects exhibited by our samples, from the macro-scale to micro-scale. The

description excludes spin transport in the spin Hall regime, but relies on the topological nature of graphene transport to provide the reported signals.

6.4.1.1 Suppression of the Dirac point

In all the devices and measurements performed, one important feature checked was the Onsager reciprocity relationships, where inverting a magnetic field and changing the position of the electrodes lead to the similar results, summarized as $R_{12,34}(B) = R_{34,12}(-B)$, for example, using the terminal notation from Figure 6.1. Despite the fact that the relationship holds true, one observation in the microscale devices was the high magnetoresistance asymmetry (Figure 6.9 b)). The asymmetry was also observed in the macroscale device, but to a lower degree (Figure 6.7 b)). It was also reported before, namely in Ref. [102]. In our case, we observed an additional feature. Figure 6.13 shows the particular case.

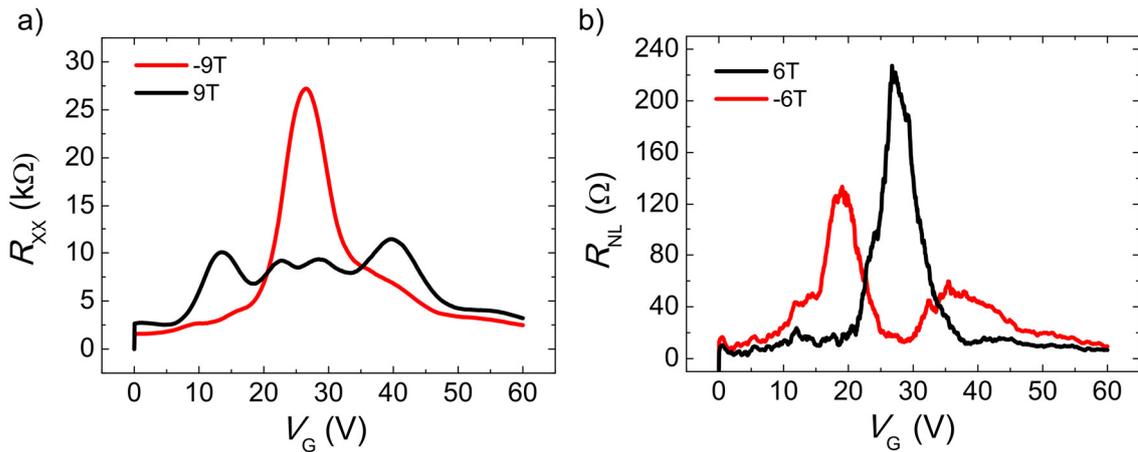


Figure 6.13 a) Longitudinal resistivity versus gate voltage for magnetic fields with same magnitude but opposite directions. b) Non-local signals for magnetic fields of with magnitude of 6 T, but for opposite directions. In both figures, $L/W = 1.8$.

Keeping the same electrodes, and performing the gate dependence of the non-local signal, the peak at the CNP would be suppressed, while the two peaks at $v \pm 2$ would show up enhanced when compared to the CNP. These features would also be visible in the longitudinal resistance (local measurements), although the DP would not be so strongly suppressed. Considering both the ZSHE and the Ettingshausen-Nerst effect in the context of the work presented in this chapter, we cannot explain this effect,

but counterpropagating edge states shunted by grain boundaries might be a reasonable mechanism to look for an answer.

6.5 Conclusions

In this chapter, we studied three types of CVD graphene Hall bars, two with dimensions superior to the ones usually employed in non-local studies of spin transport, referred to as macroscale devices, and one with dimensions similar to the spin relaxation length reported for CVD graphene devices, referred to as microscale. We detected at the millimeter scale robust non-local signals that greatly exceeded the Ohmic contribution from the channel, and that showed at most a characteristic decay length of $162\ \mu\text{m}$. At the microscale, this value decreased to $2.7\ \mu\text{m}$. The non-local signals observed depended with the magnitude of the external magnetic field, they were asymmetric with B , seemingly invariant with scale, and followed a dependence with channel length similar to the Ohmic background. We considered thermoelectric origins besides the ZSHE for the anomalously large non-local signals, namely the Joule-Nerst and Ettingshausen-Nerst effect. In our case, the strongly asymmetric non-local magnetoresistance suggests thermoelectric sources not to be at the root of the signal.

By considering the microscopic details of the transporting channel, we converged onto a picture that strongly fits to the plethora of effects exhibited by our samples, from the macroscale to microscale. We consider that counterpropagating edge states shunted by grain boundaries originate the signals observed. This model excludes spin diffusion transport, but relies on the topological nature of graphene transport to provide the reported signals.

Chapter 7

Organic transistors using CVD graphene as electrode material

Organic electronic devices have become key enablers in complex plastic electronics, owing their applicability to the versatility of organic field-effect transistors (OFETs) [202], [203]. OFETs rely on two fundamental elements: the organic material constituting the carrier channel and the contact electrodes. Recently, solution-processed polymers have been demonstrated to be suitable contenders for low-cost, and environmental friendly OFETs [204]–[206]. Meanwhile, noble metals remain the most commonly used electrode to inject and extract carriers from the organic layers. Noble metals are attractive for the role of contact electrodes due to their chemical stability and matching work function with orbital levels of the organic semiconducting materials.

With the development of OFETs aiming towards lower-cost, lower footprint, and performances on the same level as inorganic devices, contact electrodes based on noble metals are posing a strong limitation to the device operation. The large density of electronic states (DOS) makes modulating their work function extremely challenging, with the additional inconvenient of being quite expensive [207].

For the role of contact electrode, graphene has already been demonstrated to be a suitable candidate for highly performing semiconductor devices [208]–[214]. Its large-scale availability in the form of chemical vapor deposition (CVD) monolayer graphene makes it a strong contender to overcome the obstacles that noble metals face. Monolayer graphene can be sought for the role of contact electrode in organic transistors because of three properties: the gate tunable work function [215], the weak electrostatic screening [216], and its chemical stability. By electrostatically doping graphene, the work function can be modulated from 4.4 to 4.8 eV [215], in-line with the work function of many metallic electrode materials [217], [218]. Due to the low DOS of

graphene and ultimate thinness (in contrast to metals), graphene shows weak electrostatic screening. The weak electrostatic screening allows for the gate electric fields to reach the organic semiconductor on top of graphene and modulate its energy levels.

In this chapter, we propose a strategy to overcome common noble metal electrodes used in OFETs, integrating CVD graphene electrodes with *n*-type solution-processed electron-transporting polymers for high-performance lateral and vertical devices. We propose a specific design for both lateral and vertical transistors which allows us to monitor in-device the electrical properties of the graphene electrodes at each stage of the fabrication step, in particular the modulation of graphene's Fermi level and the weak-screening contributions with applied gate electric field.

We demonstrate the versatile operation of solution-processed organic transistors in lateral and vertical organic field-effect transistors (LOFET and VOFET, respectively) using CVD graphene electrodes. As electron-transporting channel material we use Poly{[N,N' -bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5' -(2,2' -bithiophene)} (P(NDI2OD-T2)), also known as Polyera ActiveInk™ N2200 [205], [206], [219], [220].

N2200 is an air stable polymer with band gap of ~ 1.45 eV, and lowest unoccupied molecular orbital, LUMO, and highest occupied molecular orbital, HOMO, energy levels ~ 4.0 eV and ~ 5.6 eV below the vacuum level, respectively [205]. OFETs using N2200 have been demonstrated to have field-effect electron mobility at room-temperature of $\sim 6 \times 10^{-3}$ cm² V⁻¹ s⁻¹ to ~ 0.85 cm² V⁻¹ s⁻¹, depending strongly with device configuration and substrate used [205], [221]. In our case, the devices are fabricated onto a 300 nm SiO₂ substrate.

This work was developed in collaboration with Subir Parui and Ainhoa Atxabal.

7.1 Fabrication of the devices

The fabrication of the devices was done in three steps for the LOFETs, and four steps for the VOFETs, following the recipes indicated in chapter 3. Figure 7.1 a) and b) show the sketch of each device.

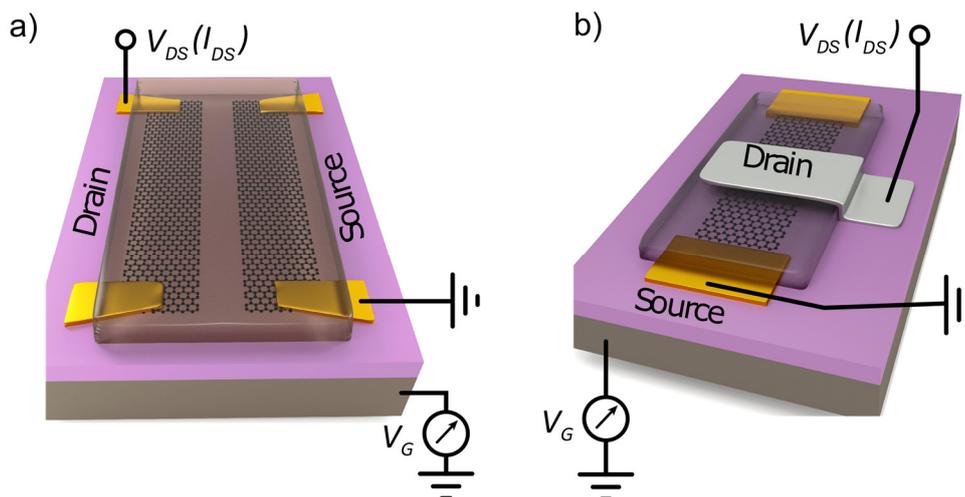


Figure 7.1 a) Sketch of the lateral organic field-effect transistor, with graphene drain (D) and source (S) electrodes, with spin coated N2200 on top. Each individual graphene electrode is contacted with Ti/Au contacts, which allow the electrical properties to be monitored. b) Vertical organic field-effect transistor, with a single graphene electrode, contacted with Ti/Au electrodes, N2200 channel, and Al top electrode.

First, the graphene electrodes were fabricated using large-area high-quality CVD-grown graphene transferred onto a $1 \times 1 \text{ cm}^2$ Si/SiO₂ (300 nm) substrate, acquired from a commercially available supplier (Graphenea S.A.). Using DL PMMA, the area surrounding the to-be graphene electrodes were exposed by e-beam lithography and etched with O₂/Ar plasma. Afterwards, a new layer of DL PMMA is again used to pattern the Ti/Au (5/40 nm) contacts pads at the end of each graphene stripe. At this stage the resulting FET was electrically characterized in a variable-temperature high vacuum probe station (Lakeshore) with a Keithley-4200 semiconductor analyzer. The graphene electrodes were 100- μm -wide, and were placed 15 μm apart from each other. The total length of each electrode was 1.5 mm, leading to an organic channel aspect ratio of $W/L = 100$ for the LOFET.

For the second step, we performed (hexamethyldisilazane) HMDS vapor priming of the oxide dielectric, with subsequent electrical characterization to understand its

impact on the graphene electrodes electrical properties. Afterwards, we would then spin coat the N2200 polymer. In addition to the evaporation of the solvent by hot-plate, we left the sample overnight in high-vacuum conditions. At this stage the fabrication, the LOFET is finished.

For the VOFETS, the fourth step was the deposition of 20 nm-thick and 300- μm -wide Al electrodes via shadow masking techniques to obtain the vertical transistor geometry. In the vertical geometry, there would be an overlapping area of $20 \times 300 \mu\text{m}^2$ between the graphene strip and the top electrode. In this vertical geometry, the 90-nm-thick N2200 layer would act as the channel between the asymmetric graphene and Al electrodes.

After fabrication, the devices were transferred to the variable-temperature probe station for electrical characterization.

The chemical structure of the N2200 polymer and the outcome of the spin coating process is illustrated in Figure 7.2.

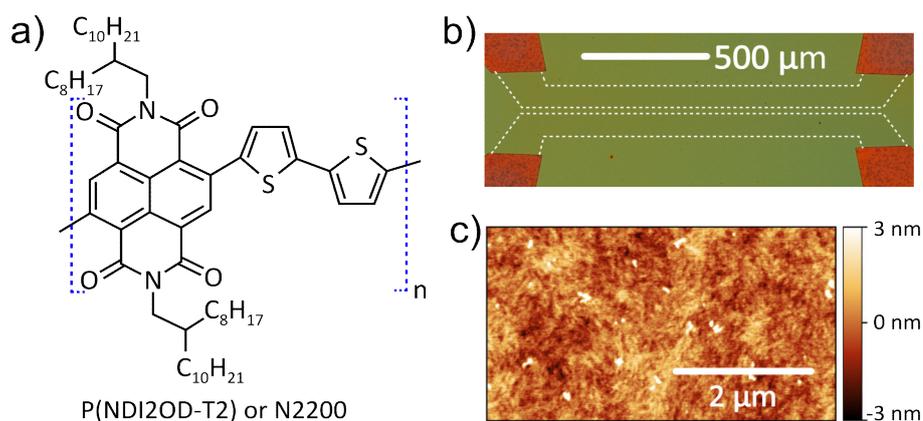


Figure 7.2 a) Molecular structure of N2200. b) Optical microscope image of the lateral devices covered with N2200, with graphene channel indicated with the dashed white lines. c) Atomic force microscopy image of the spin coated N2200, with surface roughness of 1 nm.

Figure 7.2 b) shows the optical microscopy image of a LOFET, with the graphene stripes indicated inside the dotted lines. The atomic force microscopy image of the surface topography of the spin-coated N2200 polymer on top of graphene (Figure 7.2 c)) shows a uniform N2200 film with surface roughness of ~ 1 nm.

7.2 Electrical characterization

7.2.1 Lateral organic field-effect transistor

For the electrical characterization of the N2200 LOFETs, we monitored the changes that the graphene electrodes underwent during the fabrication processes. We performed this analysis after the graphene electrodes were fabricated, after HMDS priming, and after spin coating N2200. Figure 7.3 a) and b) show the room temperature two-point transfer characteristics of the two graphene stripes used as source and drain (S, D) electrodes, respectively.

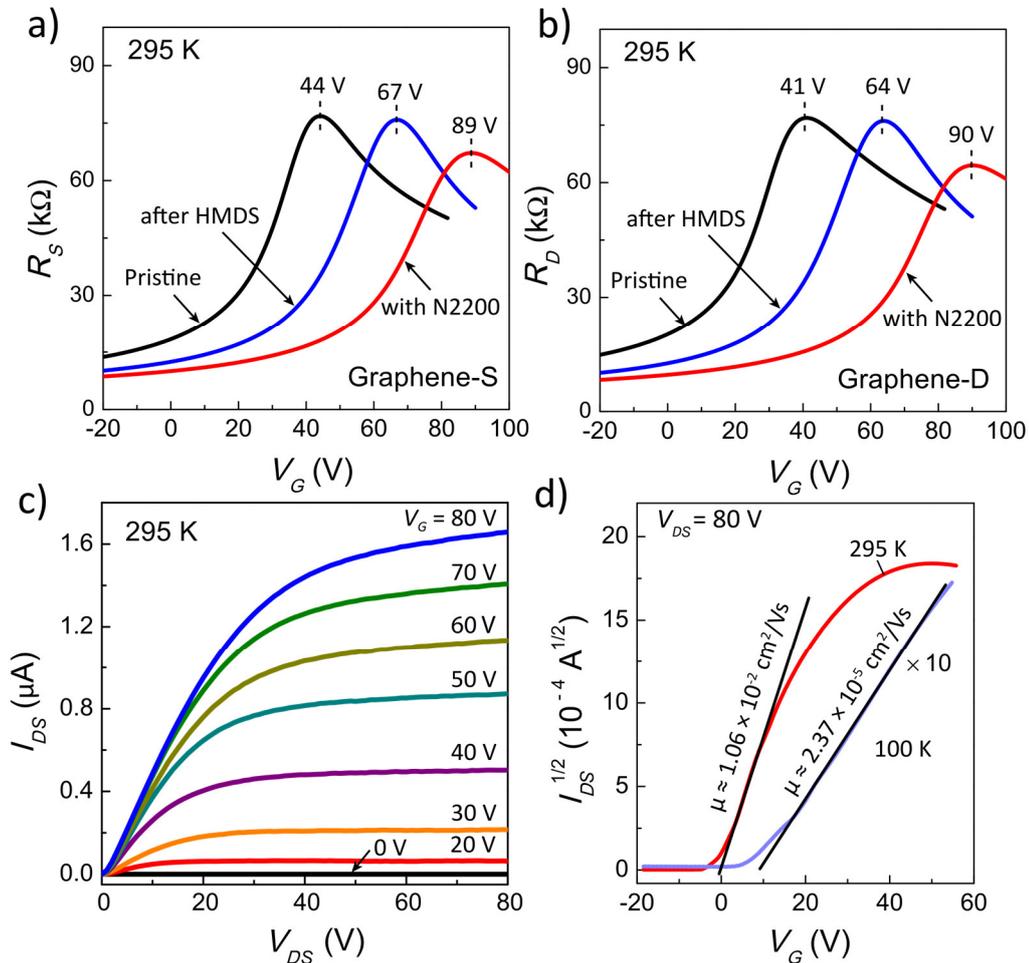


Figure 7.3 a) Transfer characteristics of the graphene source electrode at room temperature after etching, after HMDS vapor priming, and after N2200 spin coating. b) The same as a) but for the drain electrode. c) Output characteristics (I_{DS} - V_{DS}) of the LOFET for different gate voltages at RT. d) Transfer curves of the N2200 LOFET, plotted as the square root of I_{DS} as a function of V_G for $V_{DS} = 80$ V.

The transfer curves of the drain (D) and source (S) graphene electrodes show that both graphene electrodes are hole-doped, with charge neutrality point (CNP) at positive gate voltages of 44 V and 41 V, respectively. This doping level has been recurrently reported for CVD-grown graphene transferred onto Si/300-nm-thick SiO₂ substrates[213]. The purpose of using HMDS vapor priming is connected with previous demonstrations where by passivating the silanol groups of the SiO₂ surface the transport properties of n-channel OFETs were greatly improved [203], [221]. In our case, the HMDS priming lead the CNP of both drain and source stripes to shift up by more than 20 V, appearing at 67 and 64 V, respectively. Taking a close look at the shape of the transfer curves, we can see that the resistance at the CNP and curvature of the peak remain unchanged after HMDS vapor priming, indicating that other electrical properties of graphene apart from the doping shift remain consistent. Finally, with the spin coating of the 90-nm-thick layer of N2200 the CNP increases again to a higher V_G of 90 V. This occurs due to the formation of a dipole at the graphene/N2200 from the transfer of electrons from graphene to N2200. This time, the resistance at the CNP slightly decreases due to the additional conduction channel that the N2200 provides. The graphene mobility was determined using the expression $\mu = \frac{1}{R_{\square} n e}$, at a carrier density of 10^{12} cm^{-2} , resulting in $\mu \sim 3000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at RT.

Knowing now where the CNP is for each graphene stripe, we can move towards the transport across N2200. Figure 7.3 c) shows the output characteristics of the LOFET at RT for different gate voltages. We observe a nearly ideal output characteristics for the transistor operating at RT, with linear $I_{DS} - V_{DS}$ relationship in the low V_D region, and a saturation regime at higher bias, indicating a coupling between the drain electrode bias and the gate bias limiting the formation of the accumulation layer (gate pinch-off). Figure 7.3 d) shows the transfer characteristics of the N2200-graphene based LOFET measured both at room temperature and at 100 K in a square root plot of the I_D with V_G . The device exhibits typical n -type transistor behavior with RT ON/OFF current ratio over six orders of magnitude. In the saturation regime ($V_{DS} = 80 \text{ V}$), the electron mobility and gate voltage are related by the expression $\mu_{FE} = \frac{2L}{WC_{ox}} \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_G} \right)^2$. Using a C_{ox} of $1.2 \times 10^{-4} \text{ F m}^{-2}$ for a 300 nm-thick SiO₂, the determined μ_{FE} obtained were $1.06 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at RT and $2.37 \times 10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 100 K.

With the purpose of assessing if the devices fabricated with graphene electrodes were at the level of gold electrodes, we fabricated two bottom-gate, bottom-contact LOFETs using N2200 as organic channel.

Figure 7.4 shows the reference sample of N2200 and its electrical characteristics. Following the same analysis as for the devices with graphene electrodes, we found μ_{FE} to be $\sim (5.5 \pm 0.5) \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, in line with what has been reported in literature [221].

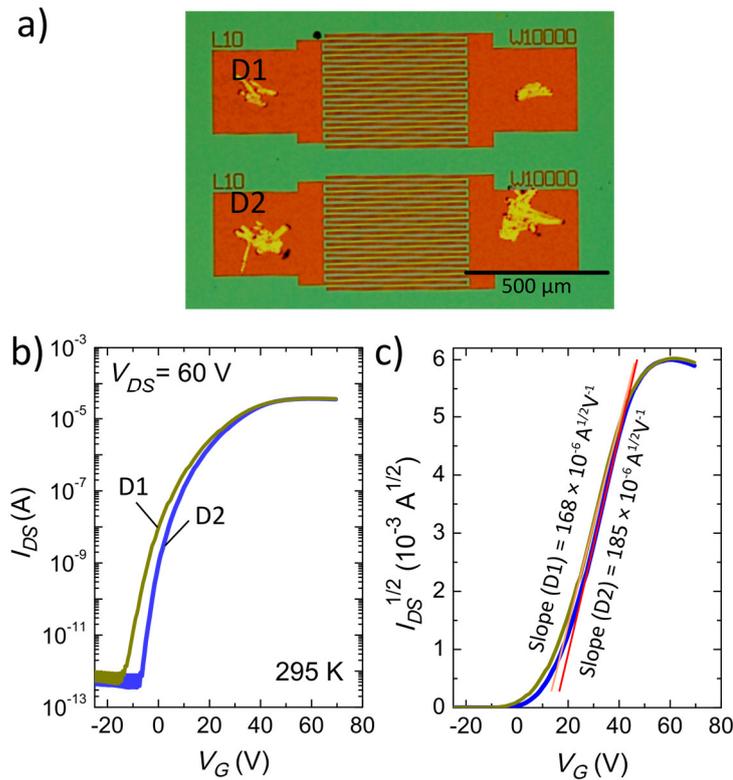


Figure 7.4 Reference samples with Au electrodes for the N2200 LOFETs. a) Optical microscope image of two devices with gold bottom electrodes patterned with optical lithography techniques following chapter 3 recipes. b) Transfer curve of the transistor for an applied drain-source bias of 60 V. c) Same as b) but re-plotted as $I_{DS}^{1/2}$ versus V_G for the extraction of the carrier's mobility.

Comparing the μ_{FE} of the LOFETs with graphene electrodes and gold electrodes, graphene contacted devices show a ~ 2 times of magnitude better performance than the devices using 30-nm thick Au electrodes, already demonstrating how a proof-of-concept device outperforms the state-of-art.

7.2.2 Vertical organic field-effect transistor

Compared to LOFETS, vertical architectures have been demonstrated to technologically enable a strong reduction in energy consumption while also allowing lower footprint devices. With the transporting occurring through a channel two orders of magnitude lower than the lateral configuration channel, the current density increases, and the overall aspect ratio decreases [222]–[227].

To study the VOFET, we again start by determining the impact of the different processes in the transfer curves of the graphene electrode.

Figure 7.5 a) shows the RT graphene field-effect characteristics of the graphene electrode that is used for the VOFET device.

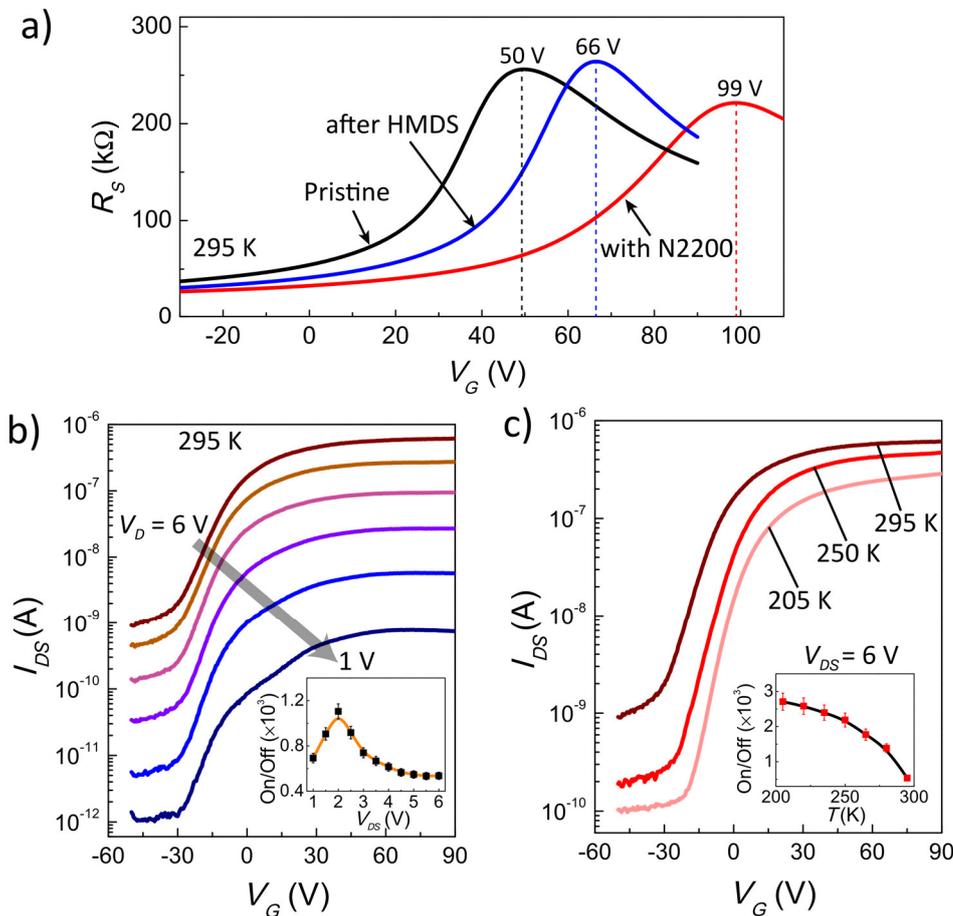


Figure 7.5 a) Gate dependence of the two-terminal resistance of the graphene used as electrode for the VOFET after fabricating etching, HMDS-vapor priming, and with N2200. b) Diode current versus V_G at several V_{DS} ranging from 6V to 1 V in steps of 1 V (graphene is grounded). Inset: ON/OFF ratio dependence with V_{DS} . c) I_{DS} versus V_G plots of the same diode at V_{DS} of 6 V and for different temperatures, ranging from 295 to 205 K. Inset: ON/OFF ratio dependence with temperature.

The narrower graphene stripe (20 μm -wide, instead of 100 μm -wide) leads to an increased resistance, with CNP remaining consistent with the LOFET graphene electrodes for the different processes. Figure 7.5 b) shows the transfer characteristics of the graphene/N2200/Al-based VOFET at RT for several V_{DS} . Applying a positive bias to the Al electrode with graphene to ground results in a reverse bias operation of the graphene/N2200 junction, with maximum modulation of the drain current with gate voltage. Sweeping the back-gate voltage from -50 V to 90 V, I_{DS} increases by 3 orders of magnitude, showing a maximum ON/OFF current ratio at $V_{DS} = 2$ V (inset of Figure 7.5 b)). Interestingly, for lower V_{DS} , the OFF-state current shows a current of $\sim 10^{-12}$ A, limited by the gate leakage. When the device is turned ON the transport across the devices gets limited by the channel conductivity, saturating at a given V_G . For increasing V_{DS} , the OFF-state leakage increases due to the leakage from the diode itself, surpassing the contribution from the gate, and leading to leakage values of 10^{-9} A. The same saturation occurs when the gate voltage is increased. In all cases, the device onset happens at $V_G \sim -30$ V.

One interesting feature to notice is the fact that the VOFET operates in the gate voltage range of ± 30 V, whereas the CNP of graphene appears at a much higher gate voltage of ~ 99 V.

This large difference between the VOFET gate voltage operation and the graphene electrodes CNP suggests that the main contributing mechanism to the vertical operation is the weak field screening of graphene [35]. In such case, the tunneling current at the graphene/N2200 interface should be enabling the transistor behavior. To further complemented the study, we performed a temperature dependence of the output characteristics from 295 K to 205 K at $V_{DS} = 6$ V. The OFF state current decreases with decreasing temperature and so does the ON state current, although to a minor degree. The resulting dependence of the ON/OFF ratio is visible in the inset of Figure 7.5 c). These features emerge from the competition between tunneling and thermionic transport at different V_{DS} and temperatures. In order to draw more quantitative conclusions regarding the nature of the energy barrier, and energy level bending, we studied the output characteristics as a function of temperature and gate voltage.

7.2.2.1 Transport mechanism

Figure 7.6 a), b), and c) show the interplay between the graphene electrode and the organic semiconductor for the formation of the energy barrier. Due to the weak screening and ultimate thinness of graphene, V_G modulates not only the work function of graphene but also the energy level bending in the semiconductor due to weak-screening effects of graphene.

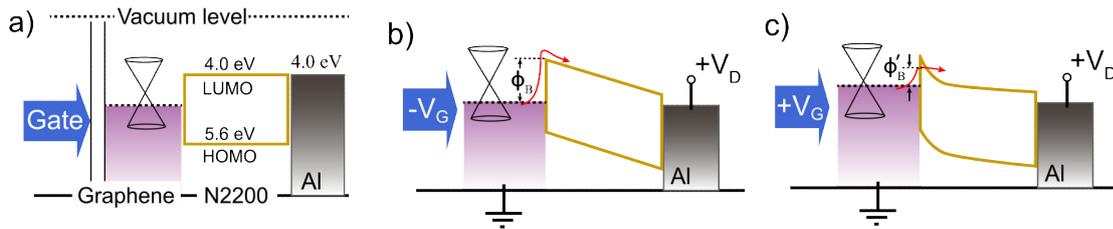


Figure 7.6 a) Rigid band energy diagram of the graphene/N2200/Al heterojunction. b) By applying a gate bias, the work function modulation changes the energy barrier, while c) weak screening of graphene leads to a change in the bending of the energy levels.

While the modulation of the work function of graphene is directly related with thermionic emission processes, where electrons being inject from the graphene into the semiconducting channel face an energy barrier that is overcome only with thermal energy, the bending of the energy levels in the semiconductor can lead to below the barrier transport, where the lower energy width makes it possible for electrons to tunnel from the graphene into the semiconducting channel.

Figure 7.7 a) shows the output-characteristics of the curve of the vertical junction diode in the semi-log scale at RT. In Figure 7.7 a), the larger modulation of I_{DS} with V_G for positive V_{DS} indicates a strong gate-modulation of the interface energy barrier height for n -type conduction, which is consistent with previous studies [213]. In a consistent manner, for positive gate voltages the increase of the Fermi energy level of graphene decreases the effective energy barrier of electrons injected from graphene to N2200, leading to a larger current at the junction. The determination of the energy barrier is done by plotting the saturation current normalized by the square of temperature, I_{SAT}/T^2 , as a function of, $q/k_B T$, and extracting the slope of the dependence in semi-log scale. The saturation current is determined at zero-bias from the slope of the

semi-log scale dependence of I_{DS} for the negative bias range where the semi-log dependence with V_{DS} becomes linear.

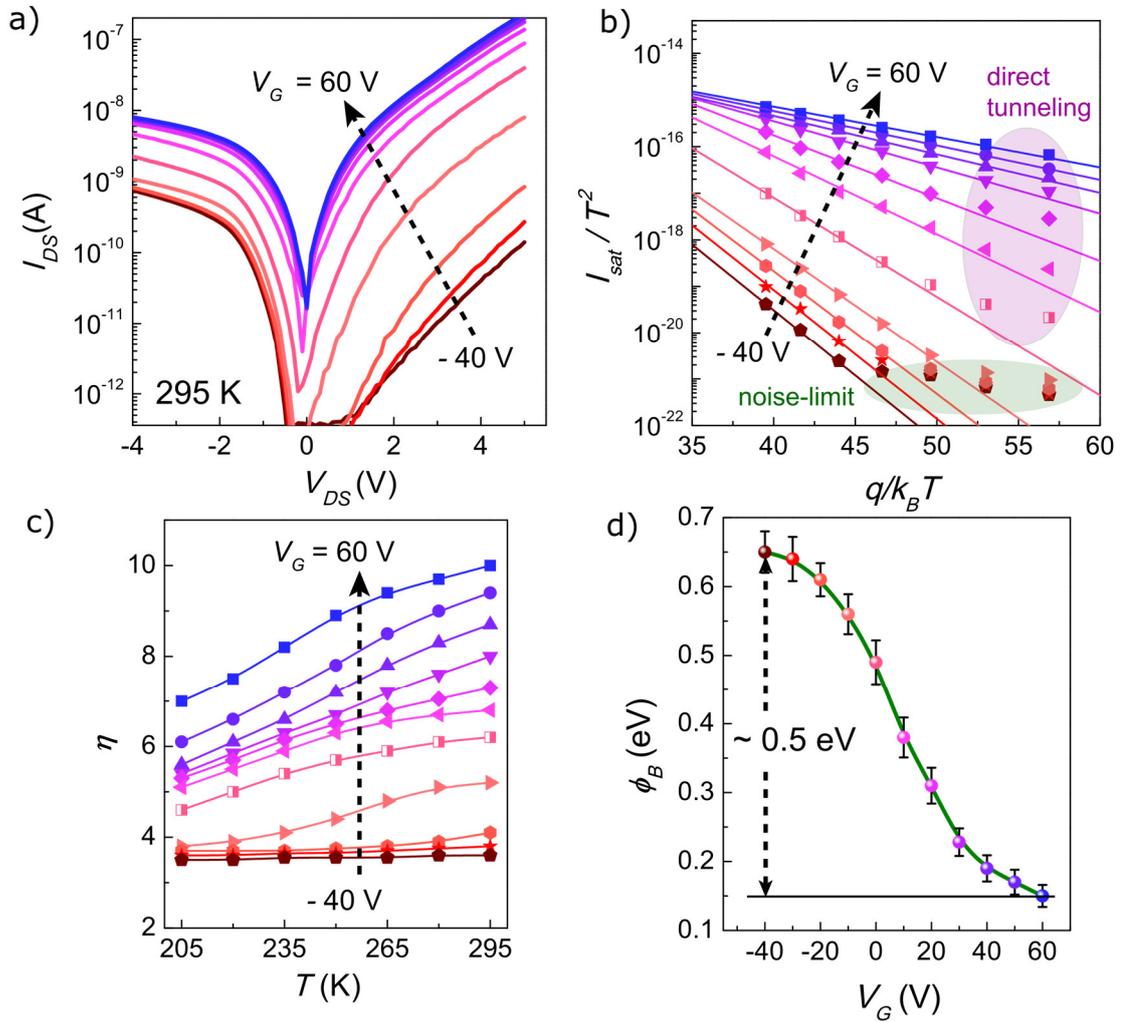


Figure 7.7 a) Output characteristics of the graphene/N2200/Al asymmetric device in semi-log scale, for gate voltages in steps of 10 V. Graphene is grounded. b) Semi-log scale plot of I_{SAT} normalized by T^2 as a function of $q/k_B T$. The barrier height is determined from the slope of the solid lines. c) The ideality factor η determined by fitting I_{DS} at negative V_{DS} (linear regime in semi-log scale) for different gate voltages and temperatures. d) Energy barrier height as a function of gate voltage.

Figure 7.7 b) shows the resulting plot. Extracting the effective energy barrier from the equation $I_{SAT} = A^* A T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right)$ [213], [228], we see in Figure 7.7 d) that for higher gate voltages the effective barrier height is lower than for lower barrier heights, facilitating the injection of electrons from graphene to the N2200 semiconducting layer. If we further evaluate the data in Figure 7.7 a) considering the non-ideality factor of the diode by fitting the drain current to $I_{DS} =$

$I_{SAT} \exp\left(\frac{qV_{DS}}{\eta k_B T}\right)$, we can determine how much the device operation deviates from a purely thermionic emission based diode ($\eta = 1$). It's clear from Figure 7.7 c) that for all operation regimes the device shows strong non-ideality, increasing for higher gate voltages and higher temperatures. This result allows us to discuss that the origin of the effective barrier height modulation is not due to the modulation of the graphene's work function but rather from an increased contribution of tunneling effects either through the energy barrier and via multi-step tunneling from graphene to Al through the ~ 90 nm thick N2200 channel.

One important observation from monitoring the graphene electrodes is that the CNP is at a $V_G \sim 99$ V, while the VOFET operates in a gate voltage range of ± 30 V. The dependence of the graphene Fermi level with the square roots of the carrier density leads to a significantly small modulation for electron-doping regimes far away from the CNP. The strong tunneling non-linearity, and the dependence of the barrier height with the gate voltage allows us to suggest that the weak screening of graphene dominates over the change in the work function of graphene for the vertical operation, confirming that the gate electric field reaches the N2200 polymer, enabling the associated VOFET operation.

7.3 Conclusion

In this chapter, we demonstrated how the integration of graphene electrodes in lateral and vertical organic transistors (in proof of concept devices) enables performances better than devices with noble metal electrodes. By monitoring the graphene electrodes, we can determine the position of the CNP and with this contribute to the most relevant conclusion in this work that the weak screening effect enables the vertical operation. In summary, the LOFETs show ON/OFF ratios of 10^6 , while the LOFET shows 10^3 . The maximum electron field-effect mobility of N2200 polymer in a lateral transistor was determined to be of $\sim 1.06 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at RT. In the vertical diode architecture, the effective energy barrier height modulation across graphene/N2200 interface was of ~ 500 meV. The different conclusions drawn from the energy barrier analysis and of the monitoring of the graphene electrodes allowed us to indicate the weak field screening of graphene to be the dominating mechanism

providing the vertical transistor operation. Combining both graphene electrodes and solution-processed polymers we obtained promising devices for future low-cost, easy fabrication and high production throughput plastic electronic applications.

Chapter 8

Metal/insulator/graphene lateral diodes

On par with field-effect transistors, diodes are fundamental building blocks for electronic circuits [6]. The applicability of diodes is based on the non-linear and strongly asymmetric output characteristics, which enables the rectification of time-varying excitations to direct-current (DC) signals or their upconversion to higher frequency. The built-in electric field characteristic of a junction between dissimilar material makes diodes composed of photosensitive materials attractive for optoelectronic applications [229].

Among the family of diodes, metal/insulator/metal (MIM) and metal/insulator/semiconductor (MIS) devices have recently attracted interest due to their applicability for high-frequency systems [230]–[237]. MIM and MIS diode-based systems are now considered to be the mainstream rectifiers for radio-frequency (RF) power detectors due to the high-efficiency in converting time-varying signals to DC signals. In this regard, MIM and MIS are seen as promising candidates for solar energy harvesting [238], [239], being predicted to surpass the conversion efficiency of semiconductor based solar cells [238], [239], for photodetectors [240]–[242], and for high-frequency mixers [243].

One of the limitations of MIM and MIS is the low conductivity levels due to the presence of the insulating tunnel barriers, which not only provides the rectifying and non-linear behavior but also greatly decrease the current output. When an antenna (acting as a voltage source) and a diode are brought together (rectenna), the impedance matching between both will define how efficiently the antenna delivers its power to the diode [244]. The input resistance of the antenna in series with the diode (modeled as a parallel capacitance and resistance) determines the RC time constant [245]. Large impedance mismatches will lead to an inefficient conversion, and large RC time constants to slow operation. Since the high-frequency operation of MIM and MIS

diodes are limited by the capacitance, it requires the strong downscaling of the device geometries to enable high-frequency operation [244].

One range of the electromagnetic spectrum that has been gaining significant applicability is the still relatively unexplored terahertz (THz) range [234]. THz radiation lies in the microwave and infrared range, typically between 300 GHz to 30 THz. Technologies exploring this range of frequencies have been shown to be promising for information and communications technology, biology and medical sciences, non-destructive characterization of material properties, security, quality control, environmental monitoring, and ultrafast computing [234]. Coupled to antennas, MIS diodes have been demonstrated as versatile tools to rectify infrared electromagnetic radiation to a DC signal [43].

In this context, graphene (Gr) has emerged as a strong contender for THz applications [233], [246]–[253] due to its high mobility [27], ultrafast carrier dynamics [248], intrinsically low quantum capacitance close to the Dirac point [42], and strong interband absorption at a wide range of frequencies [247]. MIS and MIM devices based on vertical architectures using graphene have been demonstrated to operate based on tunneling effects [232], [254], although exhibiting current densities on the order of the A cm^{-2} , and suffering from the large area capacitance inherent to the vertical construction.

In this chapter, we demonstrate the large-scale reliable fabrication of lateral $\text{Ti/TiO}_2(5.7 \text{ nm})/\text{Gr}$ diodes using contact photolithography techniques and chemical vapor deposition (CVD) monolayer graphene. The lateral construction of the devices benefits from the intrinsically low quantum capacitance of graphene and ultimately thin cross-section, while also benefiting from the fully in-plane injection and extraction of electrons through the graphene layer [147], known to exhibit highly anisotropic conductivities for out-of-plane and in-plane transport directions. Using this lateral approach, we demonstrate the rectifying and non-linear operation of the device, with current densities of the order of $5 \times 10^6 \text{ A cm}^{-2}$, while exhibiting strong figures of merit (FOM) for high-frequency applications. In our devices, we determine a RC time constant for an input impedance of $50 \ \Omega$ of $2.1 \times 10^{-14} \text{ s}$, placing our proposed device architecture in a suitable position for THz operation. This work was done in collaboration with the Graphene group in AMO GmbH, Aachen, Germany.

8.1 Fabrication of the devices

Figure 8.1 shows a sketch of the fabrication of the lateral metal/insulator/graphene diodes using scalable photolithography techniques and CVD graphene. The recipes followed during the fabrication steps described in this section are described in chapter 3. The fabrication of the devices goes through a total of 6 steps, using 1 mask and 4 different layers. All the reported oxide thicknesses have been measured using an M-2000 ellipsometer [141].

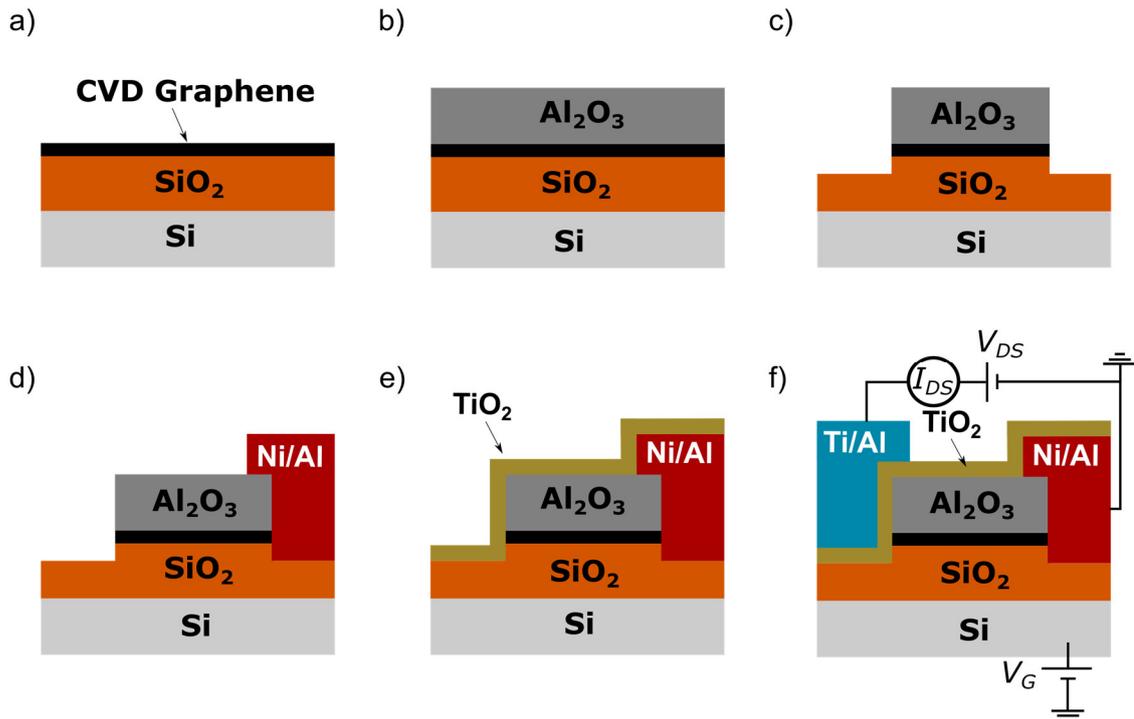


Figure 8.1 Fabrication steps of the lateral metal/insulator/graphene diodes. a) After wet transferring graphene on the Si/SiO₂ substrate. b) After encapsulation of graphene with 40 nm-thick Al₂O₃ grown by water-based atomic layer deposition. c) Etching of the graphene/Al₂O₃ layers into 70×20 μm² stripes using ICP RIE. d) Formation of the edge contact between Ni and graphene by sputtering of Ni (25 nm)/ Al (60 nm) metal electrodes. e) ALD of the insulating layer of TiO₂ (5.7 nm). f) Deposition of Ti (20 nm)/ Al(50 nm) electrodes, and two-point measurement setup.

The CVD graphene was acquired on a copper foil from a commercially available supplier (Graphenea S.A). For the fabrication of the devices, we wet transferred 1.5×1.5 cm² graphene sheets onto a 2×2 cm² Si/SiO₂ (300 nm) substrate. The encapsulation of graphene was done with a 40-nm layer of Al₂O₃ deposited by a water process of atomic layer deposition (ALD). Afterwards, we deposited Ni/Al alignment markers using AZ5214E positive tone resist. The critical step of the fabrication was the etching of the

SiO₂/Gr/Al₂O₃ stack by ICP RIE using SF₆:O₂ plasma chemistry. To guarantee clean edges, without resist leftovers or re-deposition, a layer of AZmir 701 was spin coated and patterned to define 70×20 μm² rectangular areas of graphene/Al₂O₃. The etching was optimized such that a portion of the SiO₂ substrate layer (~ 50 nm) was also etched, leaving the encapsulated graphene edges completely exposed. After etching, and without performing any stripping of the resist leftovers, the samples were quickly spin coated with a double layer of LOR and UVN30. The first metallization step was intended to establish a one-dimensional (1D) Ohmic contact with graphene. In this regard, Ni deposited with sputtering techniques has been demonstrated to be a good metal for the formation of edge contacts with graphene [255].

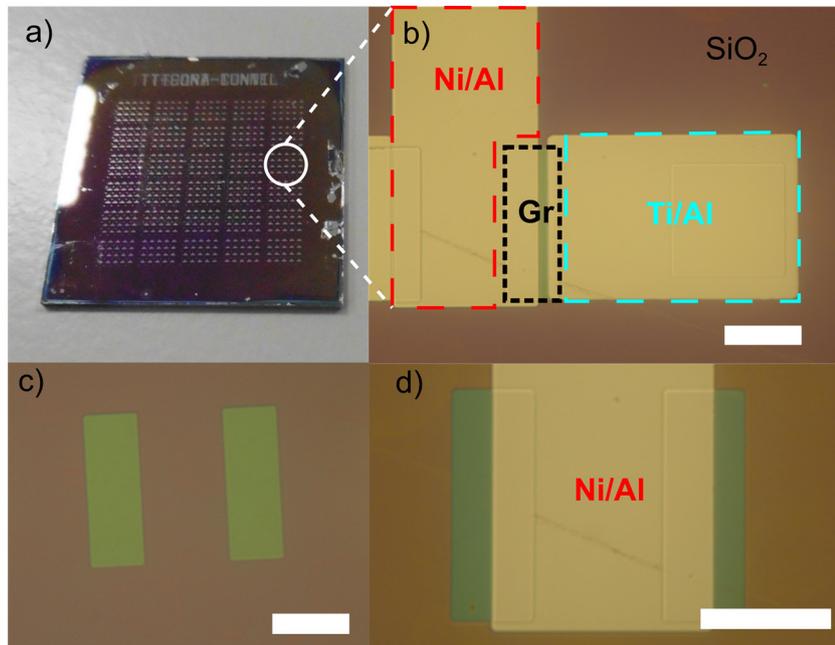


Figure 8.2 a) Photography of the 2×2 cm² chip with hundreds of devices fabricated on top of the transferred CVD graphene. b) Optical microscope picture of the Ti/TiO₂/Gr/Ni metal/insulator/semiconductor junction. White scale bar: 30 μm. c), d) Optical microscope pictures of two 70×20 μm² Gr/Al₂O₃ stacks after etching and after contacting with Ni, respectively. White scale bars: 30 μm.

The metallization was a sputtered double layer of Ni (25 nm)/ Al (60 nm). Since one of the graphene edges would still be exposed after the lift-off, the sample was immediately placed on the ALD chamber for the oxygen plasma assisted growth of the insulator layer of 5.7 nm of TiO₂ layer all over the sample. The last step was the metallization of the other side of the SiO₂/Gr/Al₂O₃ stack with Ti (20 nm)/Al (50 nm), this time using the negative tone of the AZ5214E. The final device is an asymmetric

metal/insulator/semi-metal junction composed of Ti/TiO₂/graphene, with an edge contact of Ni to graphene. The use of the mask aligner allowed us to fabricate 200 devices over the graphene area simultaneously. Figure 8.2 shows the resulting chip carrier, a microscopic picture of a Ti/TiO₂/Gr metal/insulator/semiconductor diode, and two detailed views of the etched Gr/Al₂O₃ stack, and of the Ni contact.

Additionally, two other types of devices were fabricated to confirm the Ohmic nature of the graphene/nickel contact, and the influence of the TiO₂ barrier.

8.2 Electrical characterization

Figure 8.3 shows the output characteristics of the Ti/TiO₂ (5.7 nm)/Gr device at RT and $V_G = 0$. With the Ni contact grounded, the features that immediately stand out of the output characteristic are the large current density and the rectifying behavior.

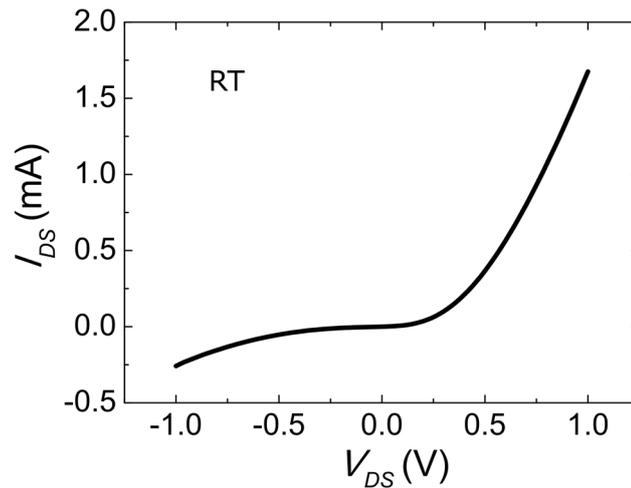


Figure 8.3 Trace and re-trace of the output characteristics of the Ti/ TiO₂ (5.7 nm)/Gr diode at RT and $V_G = 0$ V.

Comparing the performance with the current literature on metal/insulator/graphene diodes, the current density reported here for a 0.3 nm-thick and 70 μm -wide edge contact ($\sim 5 \times 10^6$ A cm⁻²) are 6 orders of magnitude larger than what has been reported in other graphene diodes based on vertical architectures of Ti/TiO₂/Gr diodes [254], vdW MIS heterostructures [232], or for state of the art Nb/Nb₂O₅/Pt MIM diodes [235], [236]. Additionally, the device exhibits negligible hysteresis.

To clarify if the rectifying behavior could emerge from a low-quality Ni/Gr contact, or not be related with TiO₂, we performed two control experiments. One symmetric device of Ni/Gr/Ni, and a second device with a thinner TiO₂ (1.7 nm) barrier between the Gr and the Ti. Figure 8.4 shows the output characteristics and the transfer curve done for both cases.

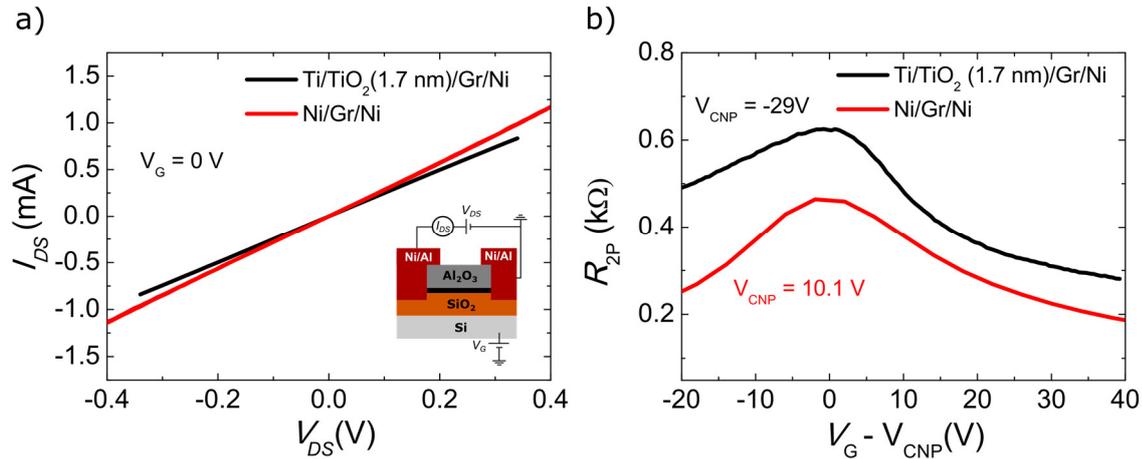


Figure 8.4 a) Linear output characteristics of the reference devices with thinner TiO₂ insulator (1.7 nm), and with Ni contacting both edges of graphene. Measurements at RT and at $V_G = 0$ V. b) Transfer curves of both devices, with the x -axis shifted according to the CNP. Measurements at RT.

Note that the reference devices have the same geometry and follow equivalent fabrication steps. The output characteristics show that the current levels increase, exhibiting a linear, symmetric Ohmic-like dependence. In the same way, testing the device for an even thinner insulating barrier between the Gr and the Ti of 1.7 nm-thick TiO₂ layer also shows a linear dependence, although with lower current density, indicating that at such thinness the TiO₂ acts only as an in series contact resistance. Note that adding the TiO₂ significantly shifts the doping of graphene from p-doped, commonly reported for CVD graphene on SiO₂ surfaces, to highly n -doped, in-line with previous works using vertical device structures of graphene encapsulated with TiO₂ [254]. For the 5.7 nm TiO₂ device, the n -doping further increased to lower gate voltages.

One of the advantages of a lateral construction for a metal/insulator/graphene diode is the low capacitance emerging from the 1D contact, limited in an ideal scenario only by the quantum capacitance of graphene, which has been demonstrated to be between 2 and 7 $\mu\text{F cm}^{-2}$ close to the charge neutrality point (CNP) in moderately

disordered samples. Assessing the RC time constant of our diode in series with an input impedance of 50Ω , with the capacitance limited by the quantum capacitance (quantified for lateral dimensions of a 0.3 nm-thick and $70 \mu\text{m}$ -wide edge contact), gives a time constant of 2.1×10^{-14} s, with cut-off frequency $f_{-3db} \approx 1/(2\pi R_{\text{input}} C_{\text{diode}})$ of 7.58 THz.

To evaluate the performance of the fabricated diode for high-frequency applications we evaluated three important figures of merit that can be determined from a DC analysis of the junction. They are the diode asymmetry, the non-linearity, and the responsivity [235], [236].

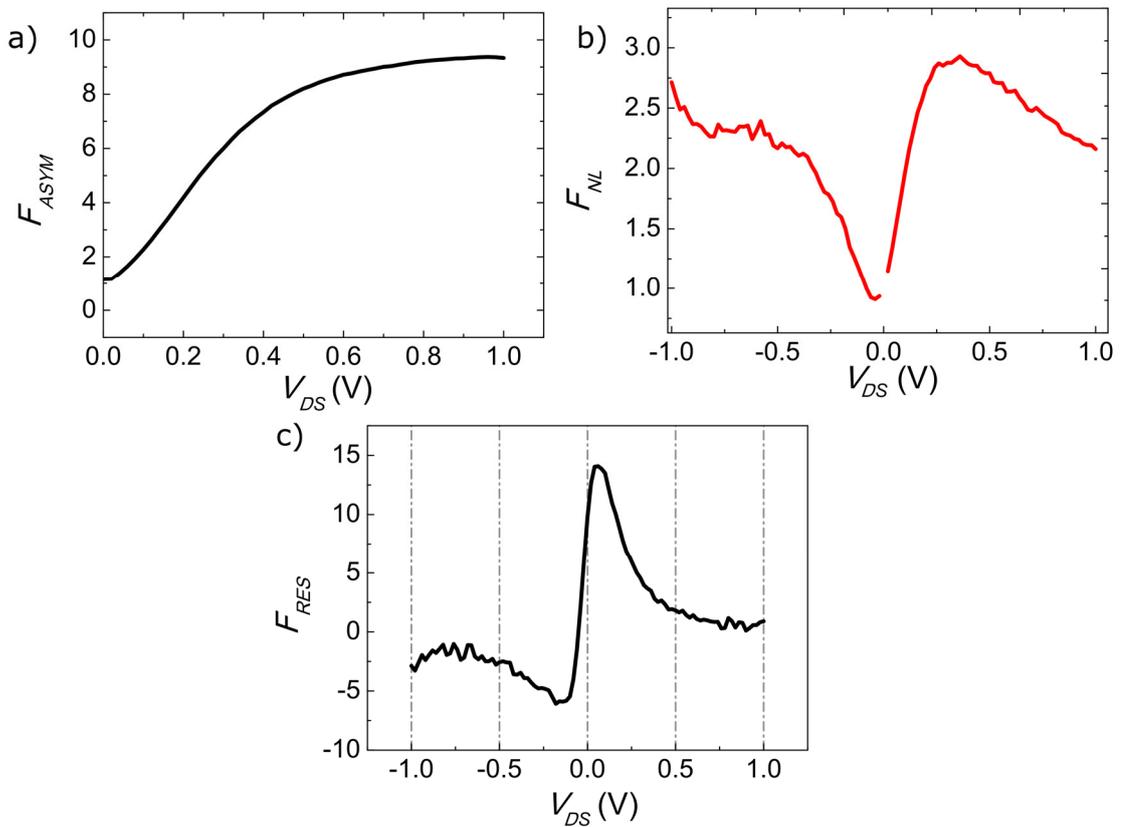


Figure 8.5 Figures of merit for high-frequency applications at room temperature. a) Asymmetry of the output-characteristics as a function of the drain-source voltage. b) Non-linearity as a function of V_{DS} . c) Responsivity as a function of V_{DS} .

The diode asymmetry is defined as the ratio between forward and reverse current density, $F_{ASYM} = \left| \frac{J_F}{J_R} \right|$, the non-linearity is the ratio between the first derivative of the current density with the applied bias and the resistance, $F_{NL} = \frac{\partial J}{\partial V} \left(\frac{J}{V} \right)^{-1}$, and the responsivity is the ratio between the second derivative and the first derivative of the

current density as a function of the bias, $F_{RES} = \frac{\partial^2 J}{\partial V^2} \left(\frac{\partial J}{\partial V} \right)^{-1}$. Ideal devices for high-frequency power conversion applications should exhibit $F_{ASYM} > 1$, $F_{NL} > 3$, and $F_{RES} > 7$, low turn-on voltages, low hysteresis, and high current densities [254].

Figure 8.5 shows the plots of the three figures of merit discussed as a function of the drain-source bias, V_D , for the Ti/TiO₂/Gr lateral stack.

For the reported device, the maximum diode asymmetry is ~ 10 for V_{DS} larger than 0.7 V, the non-linearity shows a maximum of 3 at 0.25 V, and the responsivity maximum is 15 V^{-1} . Importantly, the responsivity of the device at $V_{DS} = 0 \text{ V}$ is of 10 V^{-1} . These values are in-line with the required characteristics of an ideal junction for radio frequency applications. Compared to the state of the art MIM devices composed of Nb/Nb₂O₅/Pt, with asymmetry of 7800 and nonlinearity of 4.7 at $V_{DS} = 0.5 \text{ V}$, our devices show a substantially lower asymmetry, and equivalent non-linearity, although the current density reported in our device is 6 orders of magnitude higher than in the referred MIM diodes.

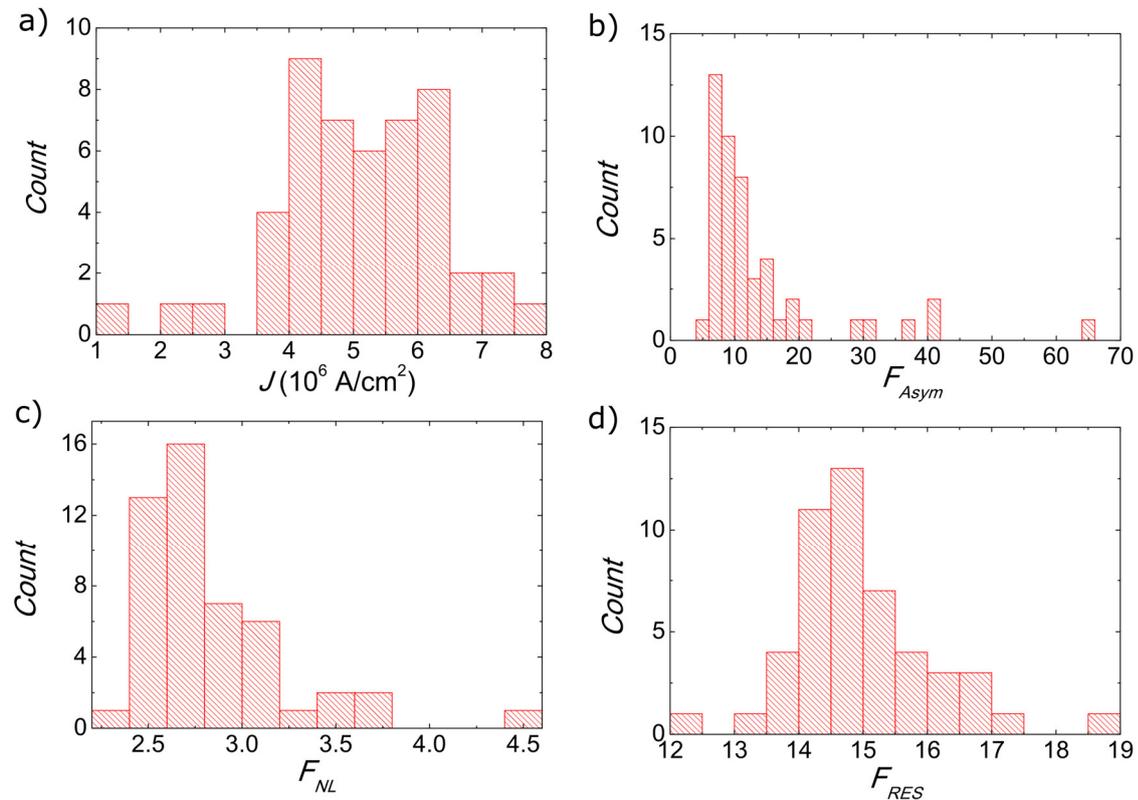


Figure 8.6 Histogram for 50 devices of a) current density, b) asymmetry, c) non-linearity, d) responsivity.

The large-scale production of the devices allows us to study the reproducibility of the fabrication procedures by studying the FOMs for many devices. Figure 8.6 shows the histograms of the FOM for 50 devices. For each one, we determined the maximum F_{ASYM} , maximum F_{NL} , F_{RES} at $V_{DS} = 0$ V, and maximum current density, J . We summarize in Table 8-1 the average and standard deviation of each FOM for the devices measured.

Table 8-1 Average and standard deviation determined for the FOM of 50 devices.

	Average	Std. Deviation
J (10^6 A cm^{-2})	5.08	1.29
F_{ASYM}	14.11	11.54
F_{NL}	2.84	0.39
F_{RES} (V^{-1})	14.97	1.08

Although these figures are important to understand how reliable the fabrication of the devices is, we should confirm the transport mechanism driving the device operation. The electron response to an external electromagnetic excitation source will significantly change based on the transport mechanism. In thermionic emission processes the transit time of electrons is known to be limited by the diffusion speed of the electrons, while tunneling relies on quantum processes to achieve significantly higher response times. With the predicted RC time constants of the level of 7.58 THz from a DC analysis, clarifying the transport mechanism becomes then quite important to further sustain the applicability.

In this regard, we performed a temperature dependence of the output characteristics and assessed it in light of thermionic emission processes, while also evaluating the output characteristics using the Simmons approximation for tunneling processes.

8.2.1 Transport mechanism

When Ti, TiO₂, and Gr are brought into contact, the energy level alignment will lead to an asymmetric trapezoidal TiO₂ energy barrier between the graphene and Ti electrode. Figure 8.7 a) and b) show the rigid band alignment and the tentative alignment under thermal equilibrium and under no external bias.

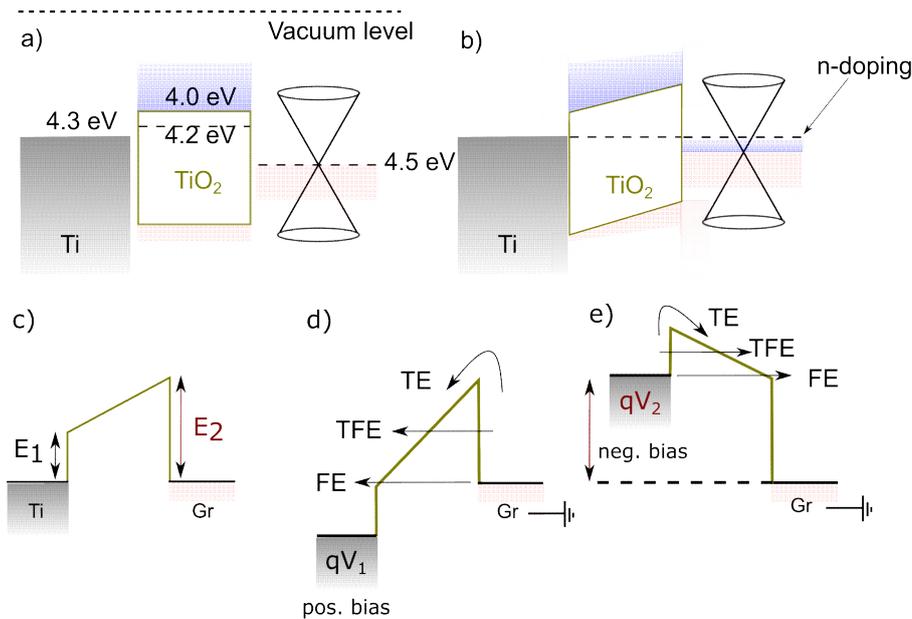


Figure 8.7 a) Energy level alignment of the Ti/TiO₂/Gr junction before placing the materials into contact. b) Energy level alignment in contact and under thermal equilibrium. c) Predicted energy barriers $E_1 = 0.3$ eV and $E_2 = 0.5$ eV at the junctions between Ti/TiO₂ and TiO₂/Gr. d), e) Representation of the transport mechanisms of the trapezoidal energy barrier under under positive bias larger than E_1/q , and negative bias larger than E_2/q , with graphene grounded.

Amorphous TiO₂ has an electron affinity of 4.0 eV and Fermi level at 4.2 eV. The two electrodes, graphene and Ti have work functions 4.5 eV and 4.3 eV below the vacuum level. When put into contact, the thermalization of the electron energy levels will lead to a constant Fermi level throughout the junction. With the requirement that at the Ti/TiO₂ and TiO₂/Gr junctions the difference between the insulator's electron affinity and the work functions of each electrode material remain the same, these conditions lead to the formation of energy barriers with different magnitude at the Ti/TiO₂ and TiO₂/Gr junctions, predicted to be 0.2 V and 0.5 V, respectively. Under bias, these junctions exhibit several transport mechanisms, namely direct tunneling (DT), field emission (FE), thermionic field emission (TFE), and thermionic emission

(TE). Figure 8.7 d) and e) represent how an asymmetric barrier under bias leads to an uneven transport for negative and positive bias with the graphene electrode grounded. At low bias, the transport is mainly mediated via direct tunneling and thermionic emission. When the Fermi level of the graphene electrode is higher than the energy barrier at the opposite junction ($qV_{DS} > 0.2$ eV), there will be a crossover from direct tunneling to field emission. With increasing bias, this contribution gets stronger and leads to an increase in the total current flowing through the device. The same will happen for a negative bias, but the crossover from direct tunneling to field emission will be happening at larger negative biases. The asymmetric output characteristics is then a consequence of the different barrier heights at the two junctions. Nevertheless, there will always be thermionic emission (TE) and thermionic field emission (TFE) components contributing to thermally activated transport.

To determine the transport mechanism behind the high-performance of the Ti/TiO₂/Gr junctions, we measured the output characteristics of the device for different temperatures. Figure 8.8 a) shows the temperature dependence of the output characteristic of the diode. Although there is a larger decrease in the reverse current than the forward current, the overall current levels do not strongly depend with temperature. At 100 K, the forward current levels are still above 100 μ A and the reverse bias current levels above 10 μ A.

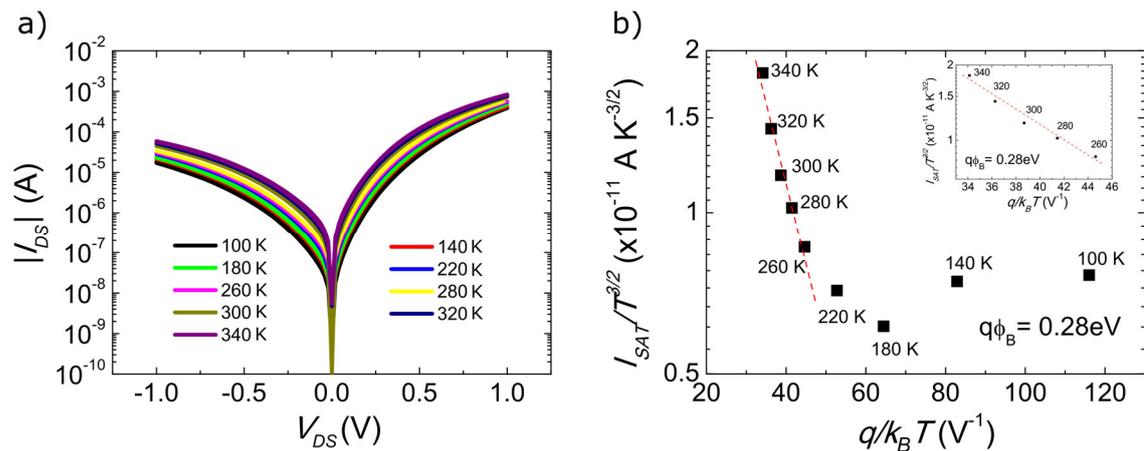


Figure 8.8 a) Semi-log scale of the output characteristics for different temperatures, b) Semi-log scale plot of I_{SAT} normalized by $T^{3/2}$ as a function of $q/k_B T$.

The determination of the energy barrier via thermionic emission is done by plotting the saturation current normalized by $T^{3/2}$ versus $q/k_B T$, following the

Richardson-Dushman expression adjusted for transport limited by a 2D semiconductor [147], $I_{SAT} = A^* A T^{3/2} \exp\left(-\frac{q\phi_B}{k_B T}\right)$. The saturation current, I_{SAT} , is determined from the linear extrapolation of the zero-bias current in semi-log scale for $qV_{DS} > 3k_B T$. In an ideal thermionic junction, the semi-log plot of the refereed quantities should result in the linear decrease of $I_{SAT}/T^{3/2}$ with increasing $q/k_B T$. Figure 8.8 b) shows that is the case only for the highest temperatures, with the device exhibiting activation-less charge transport for temperatures lower than 180 K. From the slope of the dependence at the highest temperatures, we obtained an energy barrier of 0.28 eV. Although this number is interesting to understand the energy that the electrons must overcome from a thermionic emission process, the evaluation of the output characteristic with the expression $I_{DS} = I_{SAT} \exp\left(\frac{qV_{DS}}{\eta k_B T}\right)$, which takes in account tunneling effect, shows non-linearity's, η , close to 80. This highly diverging performance from a thermionic based device shows that, although the device might have some contribution from thermally activated transport, there are strong contributions from tunneling processes. To evaluate the tunneling contribution to the output characteristics, we plot the output characteristics according to the Simmons plot for a field emission process, by expressing the dependence of the natural logarithm of I_{DS}/V_{DS}^2 with V_{DS}^{-1} .

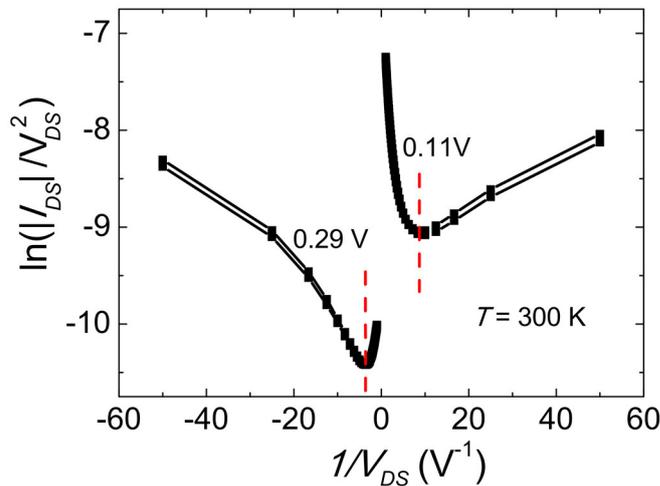


Figure 8.9 Field emission plot of the output characteristics at 300 K.

Via this plot, it is possible to detect the point at which the diode goes from a direct tunneling mechanism to a field emission dominated regime. In a direct tunneling regime, the dependence of $\ln(I_{DS}/V_{DS}^2)$ with V_{DS}^{-1} should be logarithmic ($\ln(V_{DS}^{-1})$), while the for field emission processes, the dependence is linear with V_{DS}^{-1} , increasing

with decreasing V_{DS}^{-1} . This process is visible in Figure 8.9, where for both forward and reverse bias, the transport mechanism changes from direct tunneling to field emission. The bias at which the crossover happens for forwards and reverse regimes identifies the energy barrier of the Ti/TiO₂ and TiO₂/Gr junctions, respectively. In our device, we identified a Ti/TiO₂ energy barrier of 0.14 eV and a TiO₂/Gr energy barrier of 0.36 eV, at 340 K. The discrepancy of the barrier heights with the predicted 0.2 eV and 0.5 eV might be related to the high n -doping of the graphene, which modulates the work function according to the expression $\Delta E_F = \pm \hbar v_F \sqrt{\pi n}$, where n is the carrier density, \hbar the reduced Planck constant, and v_F is the electron velocity at the Fermi level, $\sim 10^6$ ms⁻¹. ΔE_F is positive for hole-doping, and negative for electron-doping. For an electron doping of 3×10^{12} cm⁻², ($V_{CNP} \sim -40$ V), $\Delta E_F \approx -0.2$ eV, leading to a difference between the TiO₂ electron affinity and the graphene Fermi level of 0.3 eV, in agreement with the measured energy barrier via thermionic emission processes, 0.28 eV, and by evaluating the output characteristics with the field emission plot, 0.29 eV.

With this we can conclude that the transport in these devices is mainly via tunneling mechanisms, with the device asymmetry resulting from the inequivalent energy barriers at the Ti/TiO₂ and TiO₂/Gr junctions. At the highest temperatures, thermionic emission based processes contribute significantly to the total output current, with the determined energy barrier that the electrons need to overcome with thermal energy in-line with the values obtained with the Simmons equations for the maximum energy barrier, corresponding to the TiO₂/Gr junction.

8.3 Conclusions

In this chapter, we demonstrated the large-scale fabrication of lateral metal/insulator/graphene diodes using Ti as a metal and TiO₂ as the insulator, with RC time constants (for an input impedance of 50 Ω) that place its cut-off frequency in the 7.58 THz range. Benefiting from the edge contact structure and lateral stack of the Ti/TiO₂/Gr diode, the devices fabricated exhibit performance on par with state of the art MIM. The scalable approach using contact photolithography techniques shows high reproducibility, with average current density, asymmetry, non-linearity, and responsivity of 5.1×10^6 A cm⁻², 14.11, 2.84, and 14.97 V⁻¹, respectively. The study of

the energy alignment via thermionic emission and tunneling processes allowed us to confirm field emission to be the dominating transport mechanism, with the asymmetric energy barriers between the Ti/TiO₂ and TiO₂/Gr diverging slightly from the predicted 0.3 and 0.5 eV from a rigid band model, to the 0.11 and 0.29 eV, respectively, likely due to the electron transfer between the TiO₂ and respective metals contacts.

Chapter 9

Conclusions

In this thesis, we have studied the electrical transport properties of MoS₂, WSe₂, and chemical vapor deposition (CVD) graphene using field-effect transistors, Hall bars and diodes as device templates.

In chapter 4 we pin-point an electron doping limitation in the analysis of magnetoconductance in MoS₂ field-effect transistors (FETs), and by studying the source of low-frequency noise in the FETs we identify a complex interplay between the intrinsic electron doping of the flakes, the electron doping induced by external sources (the electrostatic gating and photodoping), and the strong dependence of defect-mediated recombination timescales with channel thickness as the reason for the wide variety of LFN observed in MoS₂. Additionally, using photodoping, we identify a crossover of the microscopic mechanism of the current fluctuations from carrier number fluctuations to mobility fluctuations driven by the percolative character of the conduction in MoS₂ transistors.

In chapter 5 we study the performance of ambipolar WSe₂ FETs, optimizing the fabrication conditions for maximum hole mobility on SiO₂ substrates, and study the impact of changing the top and bottom interfaces of the TMD channel with BN layers. The use of BN layers as a substrate results in an increase of the mobility by one order of magnitude up to mobilities as high as 14 cm² V⁻¹ s⁻¹, with a strong suppression of hysteretic effects, although not fully addressing the hysteretic effects.

In Chapter 6 we explore the origin of non-local signals in graphene macro-to-microscale devices, where by evaluating the enhancement at the charge neutrality point of graphene of the non-local signal with increasing out-of-plane magnetic-fields an apparently scale-invariant source of nonlocality emerged. Our experiment setup allowed us to exclude possible spin and valley related transport, while the observed asymmetry of the magnetoresistance of the non-local signals allowed us to argue in favor of

mechanisms not related with thermoelectric effects. By evaluating the microscopic details of the fabricated samples, our results strongly suggest the large non-local signals close to the Dirac point in graphene to be driven by dissipative, shunted counterpropagating edge states, mediated by grain boundaries.

In chapter 7 we explored graphene as an electrode material, and demonstrated lateral organic field-effect transistors (OFET) with performances on par with OFETs using noble metals as electrode material, using a solution-processed polymer (N2200) as channel (ON/OFF ratio 10^6 , $\mu_{FE} \sim 1.06 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). Additionally, we demonstrated that the low density of states of graphene allowed for the transistor operation of vertical organic field-effect transistors, via weak-screening effects (ON/OFF ratio of 10^3).

Finally, in chapter 8 we explored the large area availability of CVD graphene and ultimate thinness of the material to enable the large scale reliable fabrication of lateral Ti/TiO₂/Gr diodes. The lateral construction using edge contacts to graphene benefits from the small cross-section and the quantum capacitance of graphene to enable cut-off frequencies for input resistance of $50 \text{ } \Omega$ of 7.58 THz. Due to the energy alignment between the different materials, the devices exhibit current density of $5 \times 10^6 \text{ A cm}^{-2}$, orders of magnitude higher than of state of the art metal/insulator/metal devices, while exhibiting strong asymmetry (~ 14), non-linearity (~ 3), and responsivity ($\sim 15 \text{ V}^{-1}$).

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List of publications and patents

Related to the thesis:

- *Photodoping-driven crossover in the low-frequency noise in MoS₂ transistors*
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(Chapter 4)
- *Scale-invariant large nonlocality in CVD graphene*
Mário Ribeiro, Stephen Power, Stephan Roche, Luis E. Hueso, Fèlix Casanova
in preparation
(Chapter 6)
- *Graphene as an Electrode for Solution-Processed Electron-Transporting Organic Transistors*
Subir Parui, **Mário Ribeiro**, Ainhoa Atxabal, Roger Llopis, Fèlix Casanova, Luis E. Hueso, *Nanoscale*, accepted (2017), DOI: 10.1039/C7NR01007A
(Chapter 7)
- *Metall-Isolator-Graphen Diode*
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(Chapter 8)

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Other publications:

- *Spin doping using transition metal phthalocyanine molecules*
A. Atxabal*, **M. Ribeiro***, S. Parui, L. Urreta, E. Sagasta, X. Sun, R. Llopis, F. Casanova, L. E. Hueso. *Nat. Comm.* **7**, 13751 (2016)
- *Large room temperature spin-to-charge conversion signals in a few-layer graphene/Pt lateral heterostructure*
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- *Frequency driven inversion of tunnel magnetoimpedance and observation of positive tunnel magnetocapacitance in magnetic tunnel junctions*
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- *Reliable determination of the Cu/n-Si Schottky barrier height by using in-device hot-electron spectroscopy*
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Acknowledgements

There are countless people I have to thank for their support during these last 3 years.

First, I would like to thank to L. Hueso and F. Casanova for their patience and guidance, and for the opportunity given to work in a world-class research environment. I would like to thank to Joaquín Fernández-Rossier for leading the Spinograph project, and for all the students it brought together (Wenjing, Alvino, Lado, Sambricio, Noel, Denis, Luis Gonzalez, Josep, Francesca, Leutenantsmeyer, Mehrdad, Regina, Julian, and Sowmya). I would like to specially thank Wenjing and Christian Alvino, with whom I shared endless moments of joy, but also harder times where we helped each other go through them.

I would like to thank all my fellow co-workers in the Nanodevices team for listening my babbling about Portugal, Spain, and the Basque country (Estitxu, Pablo, Luca, Amilcar, Edurne, Sun, Mano, Juanma, Josu, Saul, Miren, Oihana, Elisabetta, Roger, Santiago). Thanks for all the help and time that you gave. Special thanks to Subir and Ainhoa who were always there regardless of the reason.

I would like to thank all my collaborators, namely the group of Farkhad Aliev, Stephan Roche, and Daniel Neumaier for all the nice work we did together, and again to Subir and Ainhoa, with whom I developed a wonderful team.

My greatest acknowledgement goes to my wife, without whom I would have not been able to face the many challenges that emerged during the course of this experience. Thanks for being a bastion of happiness and hope.

Cheers, everyone.

Mário Ribeiro, 2017.