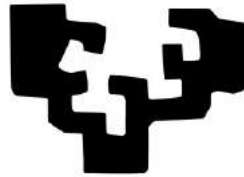eman ta zabal zazu

Universidad del País Vasco — Euskal Herriko Unibertsitatea

Resistive switching in Hafnium oxide

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-PhD Thesis-

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2014

II

Atardecer en Venecia – Claude Monet (1908)

A mi familia

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ABSTRACT

The upcoming reach of the CMOS technology physical limits in the near future has motivated the quest of the called "universal memory" and the associated development of potential candidates to become such forthcoming computing memory. The required properties of the future computing memory are exposed in the introduction together with the description of the currents potential candidates.

This thesis describes the fabrication and ulterior characterization of two types of HfO_2-based: metal/oxide/semiconductor (MIS) and metal/oxide/metal (MIM) devices in order to study its potential application as non-volatile memory device. The inherent memory properties are based on the resistive switching phenomenon, which will be described also at the first chapter of this thesis, and that is exhibited by many materials. The physical and electrical characterization of the memory devices is conducted by means of different experimental techniques described together with the device fabrication process at the second chapter of this thesis. The results obtained from morphologic and physical characterization are reported at the third chapter while along the chapters 4 and 5 we describe the results obtained from the MIS devices and MIM devices respectively. In the chapter 5 we also tackle the significant relevance of the metal electrodes on the resistive switching response as well as the interpretation of the particular non-crossing I-V hysteresis curve as well as the non-volatile memory properties analysis. In particular, the performance of hysteresis switching loops revealed the coexistence of two active interfaces which complementary switches, and whose interplay results in the mentioned non-crossing I-V curve. In addition, at the end of the chapter 5 we also includes and describes the effect of annealing treatments on the physical and electric properties. On the other hand ALD growing conditions effect on the resistive switching behaviour are described at chapter 6 together with the X-ray photoelectron spectroscopy analysis that provided us a physical correlation between the ALD deposition conditions and the resistive switching behaviour. Following, along chapter 7 we study the conduction mechanism which in conjunction with the results from previous chapters, drives to

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propose a picture for the description of the switching mechanism. Concretely there were strong evidences suggesting that the switching mechanism was based on local variations in the distribution of oxygen vacancies at the interfacial region driven by electric fields. Eventually, chapter 8 details the mathematical framework developed that allows us to rationalize the whole behaviour of our devices and reproduce the experimental I-V curves. This agreement with the experimental results verifies the switching mechanism suggested and permits the understanding of the resistive switching phenomenon observed at our HfO_2-based devices.

RESUMEN

Las tecnologías de la información y la comunicación han experimentado una evolución y un progreso sin precedentes desde mitad del pasado siglo XX. La fabricación del primer transistor, considerado uno de los más relevantes inventos de la pasada centuria, supuso la base de la denominada era de las comunicaciones. En base al transistor se desarrolló la electrónica y sus múltiples aplicaciones, así como el primer circuito integrado sobre una oblea de silicio. Precisamente la industria del silicio ha sido la dominadora de la industria de los semiconductores que gracias a los avances tecnológicos relacionados con la fabricación, pudo reducir los tamaños de los dispositivos electrónicos y duplicar el número de transistores por unidad de superficie en un circuito integrado cada año, lo que se denominó ley de Moore. Dicha ley ha ido cumpliéndose a lo largo de los años pero el ritmo se ha ralentizado durante los últimos años. Llegado el momento presente, los límites físicos de la actual industria de semiconductores se perciben no muy lejanos, impulsando la búsqueda y desarrollo de nuevas tecnologías para suplir la actual. De este modo, una serie de candidatos han surgido con el objetivo de convertirse en la base de la futura tecnología de la información y comunicación. Dicha futura tecnología debería de aunar una serie de características tales como ser robusta, no volátil, con elevadas velocidades de procesamiento y bajo costo de fabricación por bit.

Uno de los candidatos para esta futura tecnología es la denominada *Resistive Random Access Memory (ReRAM)*, basada en el fenómeno físico denominado *resisitive switching* (RS) mediante el cual, diferentes estados de resistencia eléctrica pueden ser inducidos en un material a través de la aplicación de un campo eléctrico. Además, los diferentes estados resistivos pueden ser alternados de manera estable y reproducible, lo que permite asociar a dos estados resistivos diferentes los valores típicos "0" y "1" de un bit (acrónimo de *binary digit*), que es la unidad mínima de memoria computacional. Gran cantidad de materiales exhiben este fenómeno, principalmente diferentes tipos de óxidos, que son depositados entre dos electrodos

metálicos formando la típica estructura sándwich *metal/insulating/metal (MIM)* de los dispositivos ReRAM.

Durante esta tesis se describe la fabricación y caracterización de diferentes dispositivos ReRAM basados en óxido de hafnio (HfO_2) orientados hacia una potencial aplicación como memoria computacional no volátil. En concreto se fabricaron y caracterizaron dos tipos de dispositivos: *metal/insulating/semiconductor (MIS)* y *metal/insulating/metal (MIM)*. El crecimiento de las capas delgadas de HfO_2 de 20 nanómetros de espesor se llevó a cabo mediante la técnica *atomic layer deposition (ALD)*. Los dispositivos MIS no mostraron las propiedades requeridas para un posible aplicación como memoria no volátil tales como curvas corriente-voltaje de histéresis estables y reproducibles lo que condujo a descartar estos dispositivos. Así pues el resto de la tesis se centra en el estudio y caracterización de los dispositivos MIM.

En relación a los mismos, uno de los puntos significativos de esta tesis estudia el efecto de variar las condiciones de crecimiento de las capas delgadas de HfO_2 sobre el *resisitive switching* exhibido por los dispositivos. Concretamente, en función de la temperatura de deposición y el tiempo de purga aplicados durante el proceso de ALD se fabricaron 26 dispositivos diferentes. Por su parte, los electrodos fueron fabricados mediante técnicas de *sputtering* y *electron beam evaporation* así como de litografía óptica, empleados para la definición de los electrodos superiores de 200x200 micras de tamaño.

En relación a los metales empleados como electrodos en las dispositivos MIM, diversos materiales fueron utilizados y caracterizados tanto física como eléctricamente, optándose finalmente por un dispositivo formado por Titanio como electrodo inferior y Cobalto como electrodo superior, al ser éste el que mejores propiedades de estabilidad y reproducibilidad exhibió. La caracterización física se realizó principalmente mediante diversas técnicas, tales como *atomic force microscopy (AFM)*, Rayos X y *X-ray photoelectron spectroscopy (XPS)*. En concreto, el análisis superficial realizado por AFM, tanto de los electrodos inferiores como de las capas delgadas de HfO_2, nos permitieron conocer los respectivos valores de

rugosidad. Por su parte, tanto la estructura y el grado cristalino del HfO_2 crecido en distintas condiciones, como el espesor de las mismas fueron determinados mediante diferentes mediciones de rayos X. Los resultados de la caracterización estructural mostraron un HfO_2 amorfo para temperaturas de crecimiento por debajo de 300ºC, mientras que en las muestras crecidas a 300 y 350ºC se observa una fase cristalina monoclínica dominante. Por otra parte, el análisis de capas delgadas de HfO_2 crecidas bajo diferentes condiciones fue llevado a cabo mediante *X-ray photoelectron spectroscopy*. Este análisis nos permitió establecer una correlación física entre las condiciones de crecimiento y la presencia o ausencia de *RS*. Los resultados obtenidos fueron de gran importancia para la elucidación del mecanismo físico en el que se basa el *RS* en nuestros dispositivos, posteriormente corroborado por un marco matemático.

En lo correspondiente a la caracterización eléctrica, ésta se realizó en diferentes *probe stations* y a través del instrumento de fuente-medida Keithley 2636A, mediante el cual se aplicaron diferentes protocolos de medición eléctrica. La aplicación de curvas corriente (I) – voltaje (V) nos reveló si los dispositivos mostraban un comportamiento de histéresis, y en su caso el grado de estabilidad y reproducibilidad. En este punto debemos incidir en una característica particular de las curvas I-V medidas, y es su naturaleza *non-crossing* cuando la polaridad del voltaje aplicado cambia. El estudio y análisis de esta característica revelará valiosa información acerca del comportamiento y propiedades de dispositivo.

Tras el análisis de los antes mencionados 26 dispositivos fabricados bajo diferentes condiciones de crecimiento, se obtuvo un diagrama en el cual se representa la ausencia o manifestación de *RS* en función tanto de la temperatura de crecimiento como del tiempo de purga aplicados. En este diagrama se observa una clara tendencia que muestra la manifestación de *RS* favorecida bajo ciertas condiciones de crecimiento (altas temperaturas de depósito y tiempos cortos de purga) e inhibida bajo las opuestas (bajas temperaturas de depósito y tiempos largos de purga).

RESUMEN

Protocolos de medición basados en la aplicación de pulsos eléctricos de diferente amplitud fueron utilizados para inducir las operaciones computacionales lógicas de escritura, lectura y borrado en los dispositivos, y determinar sus capacidades como unidad de memoria computacional. Del mismo modo, otros protocolos determinaron la capacidad de retención de un estado resistivo bajo un potencial constante, así como su estabilidad a través de la aplicación de un elevado número de procesos de lectura consecutivos. Los resultados señalaron unas características apropiadas para una potencial aplicación como memoria.

Con el fin de interpretar las características *non-crossing* I-V y extraer la información en ellas contenida empleamos distintos protocolos de medición tales como *minor loops* e *hysteresis switching loops*. Los resultados nos procuraron información fundamental acerca de las propiedades de los dispositivos. En concreto, mostraron la coexistencia de dos procesos de SET-RESET independientes y que indican procesos activos de *RS* en ambas interfaces del dispositivo: Ti/HfO_2 y Co/HfO_2. Además, dicho *RS* es de naturaleza bipolar, es decir los procesos de SET (cambio de estado de alta a baja resistencia) y RESET (paso del estado de baja resistencia al de alta) tienen lugar a polaridades de voltaje opuestas. A destacar, una característica reveladora para la comprensión de las curvas I-V es la naturaleza complementaria del *RS* mostrado por las dos interfaces. Cuando decimos complementaria significa que el efecto del campo eléctrico sobre la resistencia de las interfaces es opuesta. Así, si bajo una determinada polaridad del campo eléctrico la resistencia de una de las interfaces decrece, la de la interfaz opuesta crece y lo hacen simultáneamente. Cuando la polaridad del campo eléctrico se invierte también lo hace su efecto sobre la resistencia de las interfaces. De hecho, la interacción de ambas interfaces da origen a la característica propiedad *non-crossing* encontrada en las curvas I-V.

El estudio del efecto de un tratamiento térmico consistente en la aplicación de 600°C y 500°C durante 10 segundos, sobre las propiedades de los dispositivos reflejó un incremento del grado de cristalización del HfO_2 y del tamaño de grano. Por su parte la caracterización eléctrica desveló un deterioro en las propiedades del

dispositivo como memoria computacional, reflejado en la rápida degradación de uno de los dos estados resistivos tras la aplicación de un número de pulsos de voltaje.

El estudio de las propiedades eléctricas en un amplio rango de temperatura nos ofreció una serie de resultados en los cuales se puede observar como la amplitud de la curva de histéresis I-V disminuye con la temperatura hasta atenuarse totalmente. Por otro lado, el voltaje al cual se produce el SET se incrementa conforme la temperatura disminuye. Estos resultados parecen indicar que el mecanismo del *RS* pudiese estar basado entre otros, en un proceso de difusión, el cual se ve inhibido conforme la temperatura disminuye al ser éste un proceso térmicamente dependiente. Estas observaciones junto con la naturaleza bipolar observada del *RS* condujeron a considerar un mecanismo relacionado con la difusión de defectos o vacantes dentro del HfO_2 inducida principalmente por el campo eléctrico aplicado.

Como antes se ha mencionado, con el fin de obtener una correlación física entre el comportamiento eléctrico, es decir la manifestación o ausencia de *RS*, y las condiciones de crecimiento aplicadas se realizó un análisis mediante *X-ray Photoelectron Spectroscopy (XPS)*. Este análisis fue elaborado tanto en muestras que mostraban *resisitive switching* como en muestras en las que éste no se observaba. Los resultados señalaban que las muestras que mostraban *RS* presentaban vacantes de oxígeno en la interfaz en proporciones mucho más significativas que las encontradas en las muestras con ausencia del *switching effect*, donde no eran sustanciales. De este modo, la presencia de vacantes de oxígeno en la interfaz se reveló como requerimiento y causa al mismo tiempo del RS mostrado. Estos resultados proporcionaron la correlación física con el comportamiento eléctrico de los dispositivos, y nos permitió poner algo de luz sobre el mecanismo en el que estaba basado el *RS* en nuestros dispositivos. El mecanismo de conducción en el estado bajo resistivo fue determinado mediante las corrientes registradas a 15V, una vez que el dispositivo se encuentra en dicho estado. De este modo, se dilucidó un mecanismo de transporte *hopping*, el cual a su vez nos indicaba la presencia de estados energéticos en el *band gap* producidos por la presencia de defectos o

vacantes en la zona de interfaz entre óxido y electrodo lo que sería compatible con todos los resultados obtenidos hasta entonces.

Con el objetivo de determinar si el proceso de *RS* tenía lugar en una zona determinada de la interfaz óxido/metal, o si en cambio toda la interfaz estaba involucrada en el mismo, se fabricaron muestras con distintas relaciones de área entre los electrodos inferiores y superiores. Para ello, se fabricaron electrodos inferiores de distinta anchura y electrodos superiores de diferentes tamaños. En el caso de que toda la interfaz estuviese involucrada en el *RS*, la corriente en el estado de baja resistencia debería ser proporcional al área involucrada. Los resultados mostraron esta relación confirmando que el *RS* es un proceso en el cual se ve involucrada toda el área de la interfaz y no sólo una zona muy concreta y localizada de la misma, como ocurre con mecanismos de *switching* basados en la formación de filamentos conductores a través del material.

De este modo y una vez estudiados todos los resultados obtenidos, se realizó un conjunto matemático basado en sencillos supuestos para describir el mecanismo en el que se fundamenta el *RS* observado en nuestros dispositivos. Este modelo se basa en un cambio en la resistencia de la interfaz debido a la variación en la distribución de vacantes de oxígeno en las regiones de interfaz lo cual sería consistente con el comportamiento bipolar observado. En función de la polaridad del campo eléctrico aplicado estas vacantes son conducidas hacia la interfaz o repelidas de la misma. Así, al acumularse las vacantes en dichas interfaces originan la aparición de estados energéticos en el *band gap* que provocan el cambio en el estado resistivo de dicha interfaz de una barrera Schottky a un contacto cuasi-óhmico. Del mismo modo, este modelo sería compatible con la coexistencia de dos interfaces activas complementarias, ya que los electrodos están bajo valores de voltaje opuestos simultáneamente. Así pues, ambas interfaces metal/óxido son energéticamente modificadas por la variación en las densidades de vacantes de oxígeno en las zonas de interfaz por un campo eléctrico. Mediante este conjunto matemático se realizaron una serie de curvas I-V que reprodujeron con muy elevada analogía las curvas I-V experimentales, verificando la validez del mecanismo de *switching* sugerido

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CHAPTER 1

Introduction

Along this first chapter we introduce a current issue related with the semiconductor industry. The CMOS technology is near to its physical limits and soon further miniaturization will not be possible. This scenario was precisely the driving force that pushed ahead the search for a new technology which would be the basis to develop the further computational universal memory. The main candidates to become the oncoming universal memory are described as well as its advantages and disadvantages. One of the candidates will be reported in a deeper way as the present work is based on it: the resistive switching effect.

1.1 Diffusion and storage of data

The challenge of diffusion and storage of knowledge has been something existent since the beginning of the civilization as well as one of its driving forces. From the most basic knowledge transmission way as the primitive oral communication is to the current computing technology, the human being has developed and improved different platforms for data store along the times. Possibly one of the most relevant events was the emerging of writing, which is the representation of language by the use of a set of signs on a supporting medium. The first handwritten documents, also known as manuscripts, were supported on papyrus, which is a paper-like material produced from a plant, the *Cyperus papirus*. Progressively the papyrus was replaced as the usual manuscripts support material by parchment, a thin material made from hide, until the Arabians introduced the paper in Europe during the High Middle Ages. However, the widespread use of the paper did not occur until the XIV century that together with the development of the

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printing press by Johannes Gutenberg gave rise to the birth of the first book in 1449. It had to pass four centuries from Gutenberg's printing press creation, to contemplate in the XIX century the invention of the telegraph first and the radio later, which constituted the beginning of the age of communication in a real time regardless the distance. They allowed the immediate diffusion of information, and consequently of knowledge, becoming a revolution in the communication domain. However it was in the XX century as the greatest technological progress of the human being history took place. Among all the inventions and discoveries, I would like to focus on the conception and fabrication of the first transistor by Walter Brattain, John Bardeen and William Bradford at Bell Laboratories in 1948, and whereby they were awarded with the Nobel Prize in Physics in 1956. In addition, two years later Jack S. Kilby created the first integrated circuit (IC), most commonly known as chip and by which, he also received the Nobel Prize in Physics in the year 2000. The design and fabrication of these two technological concepts represented a technological revolution in the data storage, and set the fundamental basis of electronics and upcoming microelectronics, founding a new industry: the semiconductor industry. Its heart is composed by capacitors used for information storage in dynamic random-access memories (DRAMs) and complementary metal-oxide semiconductor (CMOS) field-effect transistor (FET). The transistor is the basic component in semiconductor manufacturing and the MOSFET the main member of the field-effect transistors family. The impressive advances in fabrication technology allowed a continuous scaling down of the integrated circuits. In 1965 Gordon Moore made an empirical observation, namely Moores´s law that predicted to double the number of transistors per square inch on ICs every year. The reduction in dimensions has led to an increase in performance and a reduction in the cost of the devices (a decrease of 25% per year per function). As example, the cost of flash memory has dropped from $600 per megabyte in 1987 to $0.01 in 2007 what has allowed the access to enormous amount of memory to the consumers[1]. Despite the miniaturization slowed down in subsequent years, data density has been doubled every 18 months as predicted by the Moore´s law[2]. However, the current hierarchy

storage and system memory mainly based on Hard Disk Drive (HDD) and Dynamic Random Access Memory (DRAM) respectively face serious difficulties to develop high performance computer systems. The continuity of the performance growth has to tackle obstacles as the energy consumption, space usage, cost of memory, and the continuous enlargement of the gap between the performance of hard disk and the rest of the system[3]. The gap in the performance is mainly due to the average access time of the hard disk that has been constant over the past decade at around 3-5 milliseconds. In order to overcome these drawbacks and extend the development of high performance computers, either remarkable progress in the disk drives must be achieved or new platforms for the data store must emerge and be developed. Intense research and development efforts are focused on several non-volatile memory technologies that not only enhance the existing memory and storage but also gather the benefits of storage (inexpensive, non-volatile) and memory (fast). These new memory technologies are called Store-class memory (SCM).

Memory and data storage are often confused but they are two separate entities, and the terms should not be interchanged. The main difference between them is their function. Storage is used to keep all the information of the computer in a non-volatile manner, i.e., it is not lost when the power supply is off. On the other hand, memory enables the computer to access files from the hard disk quickly but it is volatile, and the data are housed there only temporarily and it is lost once the power supply is removed. Thus, as we run an application as a word-processor for instance, the data (storage) are retrieved from the hard disk and loaded in the memory.

Nowadays different types of memory are used in computers. Random access memory (RAM) is a type of computer memory where the memory cells are arranged in arrays of columns (bitlines) and rows (wordlines). RAM is considered "random access" as you can access any memory cell directly if you know the row and column that intersect at that memory cell. On the contrary, Serial access memory (SAM) storages data as a series of memory cells that can only be accessed sequentially (hard disk, magnetic tapes, CD´s and DVD´s). SAM is much appropriated for memory

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buffers, where the data is stored in the order in which it will be used. In the most widespread form of computer memory, the Dynamic random access memory (DRAM), a capacitor and a transistor are coupled to form a memory cell where each capacitor stores a bit of information. The bit (contraction of binary digit) is the basic unit of information in computing and digital communications, and can only adopt one of two values, commonly represented as 0 and 1. The capacitor can be either charged or discharged and these two states are associated to the two possible values of a bit, i.e., 0 or 1, while the transistor acts as a switch that lets the control circuitry on the memory chip read the capacitor or change its state. DRAM memory is volatile and requires also of continuous refreshing due to the capacitor leaks charge and the information might be lost. It means high power consumption that together with the non-volatility constitutes the main disadvantages of DRAM. Respecting the established technology of flash memory, it represents an evolution to a more complex structure than DRAM and offers significant benefits as to be non-volatile and reprogrammable. Its memory cell is basically composed of a floating gate transistor, which has two gates instead one. The control gate has been redesigned to hold below a floating gate isolated all around by an oxide layer, where electrons can be stored during the writing process. The fundamentals of this memory are based on the charged or discharged state of the floating gate that represents the binary state of the cell. The detection of the memory cell state is based on the threshold voltage value of the transistor whose value shifts (restores) with the presence (absence) of charge in the floating gate. There are two main classes of flash memories NOR and NAND[3]. While NOR memory has each memory cell is directly connected to the wordlines and bitlines of the memory array, in NAND the memory cells are arranged in series creating small blocks. The different memory cells layout leads to denser packaging in NAND memory but faster access time in NOR memory. NOR flash memory is characterized by fast readout time but slow programming what focus its applications on read only access memory with sporadic modification of the data. On the other hand NAND memory allows the programming of many memory cells in parallel and the block-based architecture makes it suitable for applications demanding

block-based access such as the storage of media files (video, pictures, and music). The principal flash memory issue is the retention failure of charge with the scaling of the memory cell to ultrasmall dimensions what makes hard to keep its shrinking. This charge loss issue together with its cost, write endurance and write performance limit the potential of flash memory as candidate to replace hard disk on a large scale.

The scaling down of the memory cells dimensions drove also the subsequent thickness reduction of the dielectrics which are used as a core element of the two fundamental devices of the silicon semiconductor industry: as the capacitor dielectric used in DRAM for storage information, and as the transistor gate dielectric. The SiO_2 has been the preferred gate insulator for silicon MOSFET since its beginning in the 1960´s, and the oxide thickness has been reduced from 300 nm to the 1.2 nm over the years. But leakage currents coming from electron tunneling through the dielectrics have become the most significant limiting factor for SiO_2 films thinner than 1.5 nm, and a major technical barrier[4]. This scenario opened an intense research on high-k (k being the dielectric constant) dielectrics to replace the SiO_2 as gate dielectric material of computing elements and continue the scaling down. The materials called to substitute the SiO_2 must gather properties as good thermal stability in contact with Si, simple constituent, large electronics band gaps and sufficient band offset, much higher dielectric constants than SiO_2, and to be compatible with conventional CMOS processing[5-6]. Several materials as ZrO_2[7-8], HfO_2[9-10], TiO_2[11-12], La_2O_3[13], Al_2O_3[14-15], Y_2O_3[16-17] and Gd_2O_3[18-19] have been investigated as potential candidates. But despite the near future prediction made that ensures a further miniaturization of reliable devices due to the underlying device physics (materials and fabrication processes have been scalable so far), it will be hard to continue such scaling down in a few years[1]. For a further advance of information processing/storage technologies, we need new memory technologies with the option of meeting the integrated circuits features: small, cheap, reliable and fast. This picture means a great opportunity for alternative new technologies to become the upcoming non-volatile solid-state memory, so-called store-class memory (SCM), which would substitute current hard-disk drive. The emerging memories research focus on

obtaining non-volatile, fast, high-density, low power consumption, high data transfer rate reliable, and low cost memories. In this way, several technologies are already under an intense research and development to become the near future SCM. In the next section we will describe the basis of the upcoming store-data memory class.

1.2 Store-data memory class (SCM)

1.2.1 Introduction

As it was mentioned in the previous section, nowadays there is a gap between the performance of memory (fast, expensive, volatile) and storage (slow, non-volatile, cheap). Motivated by these circumstances, remarkable research and development efforts on several non-volatile memory technologies are taking place. These emerging technologies share the aim of reducing the differences between memory and storage and the common aspiration of becoming the next store class memory (SCM) and replacing rotating mechanical storage. A wide number of materials exhibit stable hysteretic transitions between two different and stable states. These materials can also be arranged in crossbar architectures of columns (bitline) and rows (wordline) in the way that each intersection forms a memory cell. The goal of SCM development is to create compact and robust storage systems with significant improvement of cost/performance ratios relative to other technologies. The main features for all SCM technologies are solid-state implementation, non-volatility, low cost per bit, low latencies (tens to hundreds nanoseconds), and physical durability[3]. Next we describe the main technologies that are seriously considered for becoming the forthcoming SCM.

1.2.2   Potential SCM candidates

In this section we will describe the main SCM candidates under development as well as its major benefits and disadvantages. The technologies described are ferroelectric, magnetic, phase change and resistive RAMs.

1.2.2.1   Ferroelectric RAM (FeRAM)

Ferroelectric materials belong to a type of crystals where the low symmetry produces a spontaneous polarization along one or more axes. These materials are characterized by polarization vectors that can be oriented in two opposite directions by applying an external electric field. The polarization states in a ferroelectric crystal are due to displacements of positive metallic and negative oxygen ions in opposite directions distorting the crystal and reducing its symmetry[20]. These two states are thermodynamically stable and can be switched from one to the other by applying an external field (known as coercive field) originating a characteristic hysteresis loop (see figure 1.1). The capacity showed by these materials to switch their polarization direction between two stable polarized states form the basis for the binary non-volatile memory random-access memory (FeRAMs).

In a FRAM the positive and negative saturation polarizations correspond to the logic "1" and "0" respectively, whereas the state of the system is determined by the remnant polarization when the external electric field is turn off. A ferroelectric capacitor is composed of a ferroelectric material placed in between two metallic electrodes. Although ferroelectric materials for non-volatile memory applications have been mainly complex oxides crystals and ceramics (lead zirconate titanate or PZT, strontium bismuth tantalite or SBT, etc.)[21-23], ferroelectric polymers and organic have been explored in the last years its properties known long time ago though[24]. The high-speed showed by the domain walls, enables nanoseconds speed

memories at one-micrometer film that together with its inherent low power, low-voltage operation and CMOS integration represent the main benefits of the FeRAM.
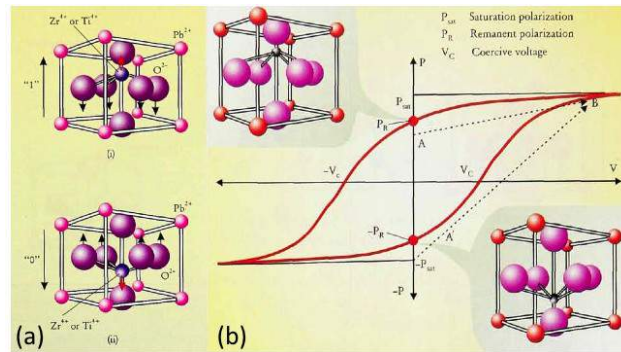
Figure 1.1: (a) Cubic perovskite $Pb(Zr_xTi_{1-x})O_3$ shows polarization up (i) or down (ii) corresponding to the logic states "1" or "0". (b) Characteristic hysteresis loop of polarization against voltage (image taken from reference 20).

On the other hand, the main drawback found is the loss of reliability or memory performance with integration of ultrasmall features using 3D ferroelectric capacitors[25]. Alternative structures have been proposed and developed as 2-transistor-2-capacitor concept (2T-2C) that deals twice signal but at a cost twice the device area[26]; or as a concept involving the fabrication of a FeFET (field-effect transistor with ferroelectric capacitor) as the gate electrode to create a NVM element[27]. The latter found several difficulties including the integration of ferroelectric materials on silicon. Additionally, other problems displayed are the fatigue (the remnant polarization decreases with cycling), imprint (a device left in one state tends to favor this polarization) and retention (loss of stored polarization over time) [25-28]. Ferroelectric polymers memory devices have been reported lately[29-32] highlighting the nanoimprinting method reported by Zhijun Hu and coworkers[33]. Nanoimprinting is a simple method for fabricating ferroelectrics bit arrays that could be used as low-cost, non-volatile random-access memories for emerging organic electronics technologies. The integration of ferroelectric polymers memory devices into larger memory arrays were reviewed by Naber et al[29] who also discussed on

that. Kang et al fabricated a polymer ferroelectric array by microimprinting[30]. It was also employed for the patterning of poly(vinylidene fluoride-trifluoroethylene) copolymer films with excellent pattern transferring[31].

There are also other key integration issues in FRAMs that have to be addressed, such as stacking technology for the preparation of robust ferroelectrics, capping technology to encapsulate the capacitors of the cell as well as etching technology to avoid capacitors damage by plasma[34]. Despite the issues and disadvantages enounced above, FeRAM has been already implemented into the market in in microcontrollers, memory products, and in high quality industries such as automotive where manufacturers such as Mercedes, GM, BMW, Ford, Porsche, and others, are now using FRAM in their automobiles [35].

1.2.2.2   Magnetic RAM

The development of very sensitive sensors for the detection of weak magnetic fields associated with the data bearing magnetic transitions on the disk permitted the fast improvement in the areal density of hard disk drive (HDD). The work on these sensors led to the magnetic tunnel junction (MTJ) [36] the heart of an MRAM cell. The MRAM memory cell is based on a structure of two magnetic layers separated by a dielectric material. through which, depending on the relative magnetization of the two layers, an amount of spin-polarized tunneling current pass. Thus, when the two magnetic layers have the same polarity the resistance is lower and it means "1", while when the polarity is opposed the resistance is higher and it is considered "0" (see figure 1.2).

The magnetization of one layer is fixed while the other is allowed to flip by the action of an external writing effect[1]. The resistance of the MTJ is low if they are parallel and high if they are antiparallel. The reading step is simple and consists of passing a small current through the MTJ by a sense circuit to determine if it is in the high or low resistance state. This effect is known as tunneling magnetoresistance (TMR).
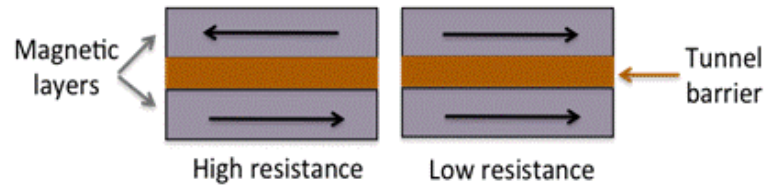
Figure 1.2: The two resistance states of a MTJ, low (left) and high (right) corresponding to two stable states.

There are two main types of MRAM known as toggle MRAM and spin-torque MRAM. They are different in the way they write the magnetic state, and while toggle MRAM employs magnetic fields to write, spin-torque uses a current pulse directly through the MTJ[37].

The magnetic RAM cell advantages are its fast speed, compatibility with embedded designs, non-volatility, and very high endurance as there is no known wear-out mechanism for magnetic switching. On the other hand, the main problem observed are the high writing currents (>1 mA), which are not elude by the scaling down of the devices. These currents are large enough to induce electromigration, damaging the wires themselves and becoming the major failure[1]. Despite the mentioned drawback, MRAM memory has been implemented. As examples, Airbus replaced SAM and flash components by 4 and 16 Mb MRAM chips for the flight control computer[38] and BMW also used 4 Mb MRAM chips in one of its super bikes models to store important calibration data in order to enhance the motor bike control[39].

1.2.2.3   Phase change RAM (PCRAM)

The operation of the PCRAM is based on the large divergence exhibited between the electrical resistances of the amorphous and crystalline states in phase-change materials that can be up to five orders of magnitude[40]. Generally the amorphous phase has higher electrical resistance than the crystallized phase. A phase-change material sandwiched in between two metal electrodes forms the PCM

cell. The SET operation, by which the amorphous phase becomes crystallized, is drove by means of an electrical pulse that heats the programming region of the cell above its crystallization temperature. To RESET the PCM cell into the amorphous state, the programming region is first melted by applying a larger electrical pulse than that used to SET, and then quenched. This amorphous region is in series with any crystalline region of the PCM and effectively determines the resistance state of the PCM cell between the two electrodes[40]. The phase change devices mainly use chalcogenides materials[40] that are ternary materials such as $Ge_2Sb_2Te_5$ (GST)[41], the most commonly used chalcogenide, GeSb (GS)[42] or Ga-Sb-Te[43].
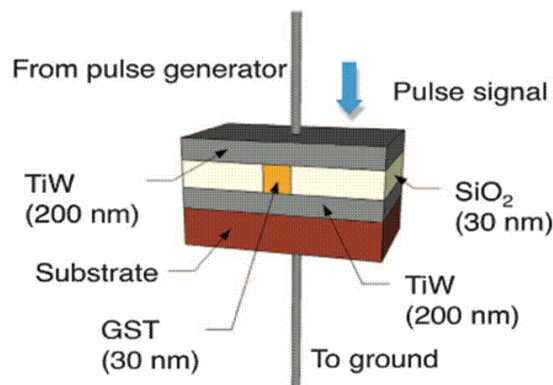
Figure 1.3: Schematic of the PCRAM structure with the pulse signal delivered to heat and crystallize the PC material (GST) (Image source: reference 47).

The benefits exhibited by PCRAM are its non-volatile nature, high scalability (beyond 22-nm node), low power consumption, high read/write speeds and long read/write endurance. Recent progresses in PCRAM were reviewed and described by Wong et al including strategies to achieve multibit operation and 3-D multilayer high density memory arrays[44]. These properties allow considering PCRAM as a solid candidate for the universal memory as reported by Wuttig[45]. However, this technique has to face issues as high access latencies, high power cost and a wearing performance faster relative to DRAM[46]. Besides, the crystallization speed is much slower than the melting process speed, which limits the overall writing speed of the

device making difficult to achieve speeds below 1 nanosecond. Nevertheless, Loke and co-workers reported crystallization speed of 500 picoseconds by controlling the crystallization kinetics[47]. Furthermore, the Micron Technology company announced in July of 2012 an industry first PCM with high-volume availability of its 45-nm for mobile devices featuring 1Gb which has been integrated in Nokia smartphones[48].

Next, we will describe deeper the remaining potential technology to become the further store-class memory: the resistive RAM.

1.3 Resistive random access memory (ReRAM)

1.3.1 Principles of resistive switching

The ReRAM memory cell is generally a two terminal capacitor-like structure composed of insulating or semiconductor materials sandwiched between two metal electrodes (see figure 1.4). The insulating-semiconductor materials are oxides, higher chalcogenides, or other ionic solids whose resistance state change can be reversibly switched by the effect of an electric field. Often, before these MIM cells can be electrically switched between at least two resistance states an initial electroforming process is required whereby a soft breakdown of the material is produced.
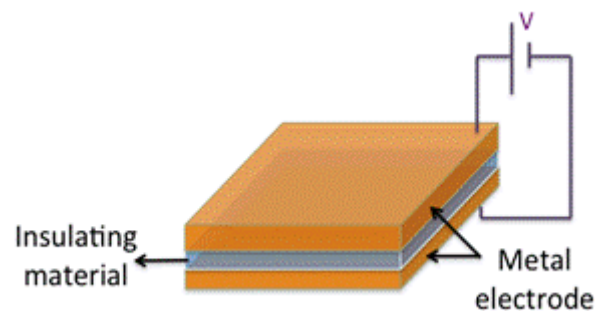

Figure 1.4: schematic diagram and electrical configuration of a typical two terminal ReRAM cell.

Resistive switching alludes to a physical phenomenon in which an insulating material changes its electric resistance by the action of an electric field or current. This change of resistance is characterized by being reversible and non volatile. By applying a programming voltage pulse of appropriated value, a device in its high resistance state (HRS) can be set to a low resistance state (LRS) by the called SET or writing process. In the same way, a device can be switched back to the HRS by a voltage pulse via the RESET process, also called erase operation. The ReRAM types can be classified in two switching mechanism: unipolar and bipolar[59]. If the SET and RESET processes occur at the same voltage polarity the switching operation is called unipolar. During the SET process the current is usually limited by the current compliance (figure 1.5a). On the other hand the switching operation is bipolar when SET and RESET processes occur at voltages of reversed polarity (figure 1.5b).
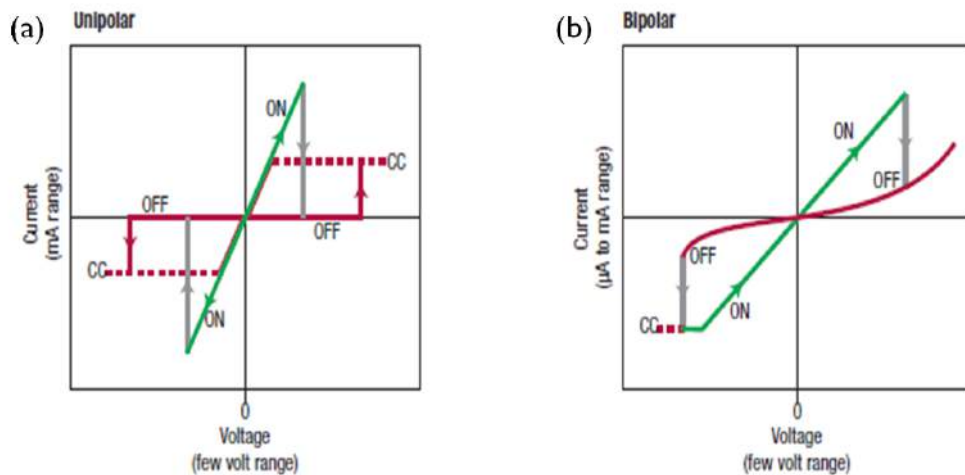
Figure 1.5: sketches of the characteristics I-V curves of the two basic types of resistive switching operation. Dashed lines indicate the current compliance applied. (a) Unipolar switching. (b) Bipolar switching, the SET and RESET require opposite polarity. In some systems current compliance is not used (Image taken from reference 59).

The simple memory cell structure is one of the benefits of ReRAMs together with its high scalability, compatibility with CMOS technology, potential application in

3D stacks, high speeds, low power operation, endurance and non volatility. The main handicap found to develop reliable and robust resistive switching memory devices has been the understanding of the underlying switching mechanisms.

Although resistive switching phenomenon manifestations can be traced back two centuries[49], the theoretical basis was not established until 1971 when L. Chua[50] announced the memristor concept (a contraction for memory resistor). The memristor has been proposed as the fourth basic circuit element together with the already known: the capacitor, the inductor and the resistor as depicted at figure 1.6.
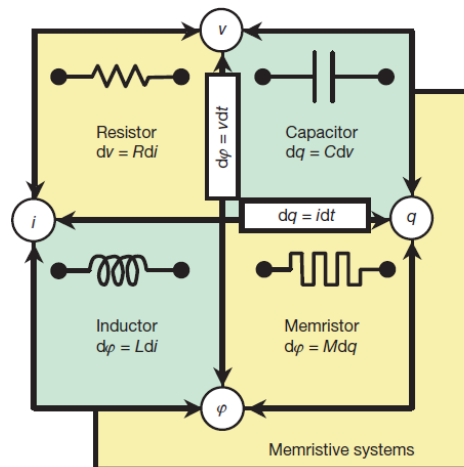
Figure 1.6: the four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor (image taken from reference 52).

A memristor behaves like a linear resistor with memory exhibiting nonlinear features. The memristor, with memristance M, provides a functional relation between the charge q and the flux as follows: d $= Mdq$. In the case M is itself a function of q it yields to a nonlinear circuit originating current (I) - voltage (V) characteristics which a combination of nonlinear resistive, capacitive and inductive components cannot reproduce. In 1976 Chua and Kang generalize the memristor concept to wider type of nonlinear systems described by the equations[51]:

$$v = R(w, i)i \qquad (1)$$

$$\frac{dw}{dt} = f(w, i) \qquad\qquad (2)$$

where *w* can be a set of state variables, and *R* and *f* can be explicit functions of time. Equation (1) allows discerning a memristive system from a dynamical device; when the voltage drop along the memristive system is zero no current flows through. However there was no direct correlation between the mathematics and the physical properties of any practical system until 2008, as Strukov and co-workers confirmed the connection between theory and experiment[52]. They presented a physical model of a two-terminal electrical device that produces hysteretic behavior controlled by the intrinsic nonlinearity of *M* and the boundary conditions of *w*. On the basis that hysteresis requires atomic rearrangement that modulates the electronic current Strukov et al. considered the total resistance of the device determined by two variable resistors connected in series that represented two regions discerned into the semiconductor film. One region had high concentration of dopants having low resistance R_{ON}, and the second region low concentration of dopants (essentially zero) and much higher resistance R_{OFF} (Figure 1.7). The drift of charged dopants via the application of an external bias *v(t)* across the device modified the boundary between the two regions yielding the resistive switching phenomenon. Thus, authors showed that memristance arises in nanoscale systems, in which ionic transport and solid-state electronic are coupled under an external electric field. These results provided an explanation for reports appeared for the last nearly 50 years[53,54] of I-V irregularities, including switching and hysteretic conductance, multiple conductance states and negative differential resistance, particularly in thin films two-terminal nanoscale devices However, despite this switching scenario proposed by Strukov et al is able to describe the behaviour observed in numerous materials systems, there are other materials where it fails. Different switching mechanisms have been proposed to explain diverse switching behaviors and they are described in the next section.
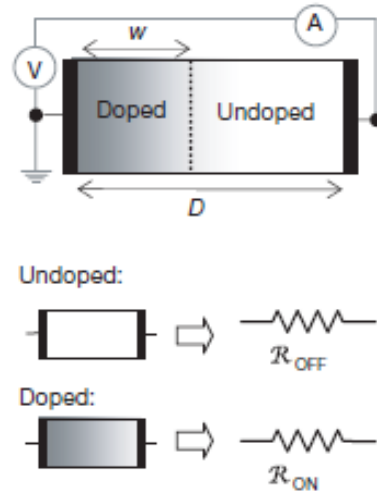
Figure 1.7: diagram with a simplified equivalent circuit. V, voltmeter, A ammeter (image taken from reference 52).

The advances in thin film technology experimented in the 1960s permitted the fabrication of ultrathin metal/oxide/metal structures wherein the resistive switching behavior was pronounced enough to be observed in different such as TiO_2, ZrO_2, Al_2O_3, SiO_x, Nb_2O_5 and Ta_2O_5[53,54]. However the research work faded away after a decade probably due to the amazing progress of the silicon integrated circuit technology. Ironically the gradual slow down undergone by the own silicon technologies in the late 1990s, gave rise to the exploration of new memory technologies what led to a renewing attention in resistive switching effect[55] led by Asamitu et al in manganites[56], Kozicki et al in chalcogenides[57], and Beck et al in pervskites[58]. The stochastic and localized nature of the switching effects has been the main difficulty for the understanding of the electrical switching[60]. However such understanding has experienced a significant progress mainly due to the advances in the growth and characterization of nanoscale materials during the last decades. In the next section we will focus on the description the most important switching mechanisms.

1.3.2   Resistive switching mechanisms

As it was mentioned before there are different mechanisms that have been suggested to explain the resistive switching effect observed in a wide range of materials. The key concepts of the switching mechanism described in this section are given in the next table. The valence change memory cells have associated two different switching sources.

Memory cell type	Switching source	Switching behaviour
Electrochemical metallization	Electrochemical formation/dissolution of metallic filament composed of cations M^{z+} from one cell electrode	Bipolar
Thermochemical	Conducting filament formation based on local stoichiometry variations and redox reactions induced by local temperature gradients that lead to a change in the electronic conductivity	Unipolar
Valence change	Formation of an oxygen vacancy enriched region that propagates from the cathode towards the anode	Bipolar
	Variation of oxygen vacancies density at interfacial metal/oxide	

Table 1.1: summary of the different memory cells together with the respective switching behaviour and a brief description of the switching source.

1.3.2.1   Electrochemical metallization memory (ECM)

In this memory cell the resistive switching operation is based on the electrochemical deposition and dissolution of a metallic filament in between the two electrodes. The electrochemical metallization (ECM) cell, also called Conductive Bridging (CB) o Programmable Metallization Cells (PMC) in literature, is composed of an active electrode (AE) made of an electrochemically active metal M (such as Ag, Cu, etc.), an electrochemically inert counter electrode (CE) (Pt, Ir, Au, etc.) and a thin film of a solid electrolyte[61]. This thin film is either a solid electrolyte containing M^{z+} as a host cation (e.g. Ag_2S, Cu_2S) or an insulator doped with M^{z+} cations.
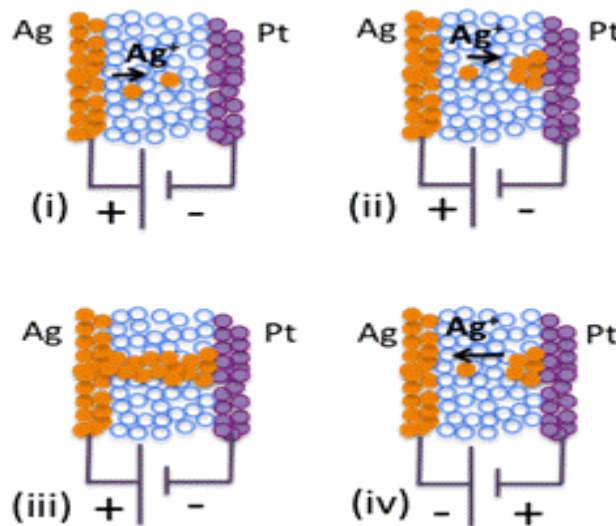
Figure 1.8: schematic illustration of the growth and dissolution of the metallic filament at an ECM cell. (i) Anodic dissolution of M (Ag in this example). (ii) Migration and electrocrystallization of the cations M^{z+} at the inert electrode (Pt in this example). (iii) Metallic filament formation in between the two electrodes. (iv) Dissolution of the metallic filament when the voltage bias is reversed.

A SET operation occurs if a large enough positive bias voltage is applied to the active electrode. The SET process starts with the anodic oxidation and dissolution of M in the solid-electrolyte thin film as a metal cation M^{z+} [see figure 1.8

(i)]. The cations migrate across the solid-electrolyte under the action of the electric field towards the inert cathode, where they are reduced and electrocrystallized [figure 1.8 (ii)]. The electrocrystallization process leads to the growth of a metal filament in the direction of the active electrode. The cell is switched to the ON state when the metallic filament bridged the two electrodes [figure 1.8 (iii)]. The RESET process takes place by applying a sufficient voltage of opposite polarity that causes the electrochemical dissolution of the metal filament [figure 1.8 (iv)]. In some ECM cells the amorphous thin film contains no cations M^{z+} of the electrochemically active metal after fabrication[62] what makes necessary a forming process before reproducible resistive switching can be observed. Via such electroforming procedure mobile M^{z+} cations are introduced into the insulating amorphous film. Another motive for the necessity of the forming process can be the formation of a first metallic filament causing a nano-morphological change in the electrolyte. As reported for the $Ir/SiO_2/Cu$ memory cell[63] the first I-V cycle was regarded as the forming process The switching voltage during this first cycle was higher than in the consecutive cycles. A possible explanation is that the metallic filament has to be formed once and later on switching occurs at the interface of the metal dendrite and the metal electrode.

Although several filaments might nuclei and growth simultaneously, it is generally accepted that only one filament provide the contact between the two electrodes, as the electric field drops abruptly when the first filament makes the contact and reaches the current compliance. Regarding the growth of the filament in MIM cells, it is considered to be formed through the thin film during the electroforming and the SET operation. It is also thought that the filament growth is supported by extended defects as nanopores and grain boundaries by limiting the local mechanical stress.

Hirose and Hirose[64] reported in 1976 the first resistive switching due to the formation and dissolution of a metallic filament in a lateral system $Ag/Ag-As_2S_3/Au$. Nowadays, the most frequent ECM systems have Ag or Cu as electrochemically active metal. Sakamato and coworkers[65] described nanometer-scale switch in the

sandwiched structure Cu/Cu_2S attributed to the formation and annihilation of a conductive path inside the Cu_2S, resulted from the migration of Cu ions. Crystalline-amorphous phase transition was ruled out as origin of the switching as it showed to be depend on the voltage polarity applied. Several cells based on different solid electrolytes as Ag-Ge-Se, Ag-Ge-S, and $Cu-WO_3$ were described by Kozicki et al.[66] who reported switching speeds of 35 ns and endurance superior to 10^{10} cycles. On the other hand Wang et al.[67] elucidated the resistive switching described earlier in Zn_xCd_{1-x} showing that a metal easily oxidized and capable to diffuse into the ZnCdS film is needed to form a conducting filament. They also described that the formation process was more random than the annihilation of an existing filament, due to the competition among localized filaments, resulting in a large variation in the threshold SET voltage value.

1.3.2.2   Thermochemical Memory (TCM)

Thermochemical memory cells are also composed of a transition metal oxide in between two metal electrodes, which are often the same metal as no asymmetry is required. Its operation is based on local stoichiometry variations and redox reactions that lead to a change in the electronic conductivity induced by local temperature gradients. Metal transition oxides display in the most oxidized states a high resistivity, which decreases in reduced states.

The electroforming process is triggered by the residual conductivity of the insulating material that leads to local generation of Joule heat. As the pristine state conductivity in semiconducting cells is thermally activated, the heating further increases the current to induce finally a thermoelectric breakdown. The application of a current compliance limits this process and controls the ON-state resistance. This event originates a local discharge channel where the temperatures are high enough to produce redox reactions and a resulting conducting filament between the electrodes. The negative free energy formation, common to all the stable oxides, is the driving force that supports lower valence states at higher temperatures. The

abrupt temperature gradient between the hot filament and the surrounding regions causes a significant thermodiffusion of oxygen anions out of the filament and/or cations in the opposite direction[62]. The cation and anion contribution depends on the material system. Thus, the filament formation switches the cell into the low resistance state (LRS) or ON state. When the current compliance is reached the voltage drops, the local temperature decreases and the cell remains at the ON state. The cell is switched back to a high resistance state (HRS) or OFF state by applying a voltage of the same polarity with current compliance held inactive, resulting in a high current and the corresponding Joule heat, which disrupts thermally the filament. After describing the switching effect, it can be assumed that TCM systems are characterized by displaying unipolar switching characteristics. Due to a partial rupture of the filament during the RESET process and not a complete dissolution the switching voltage in the subsequent SET processes will be lower than the forming voltage. As the distance between the electrode and the end of the residual filaments is smaller than the entire oxide layer, the voltage required to trigger the SET process is notably reduced.

The resistances of both the pristine and OFF states were found to be nearly proportional to the electrode area[68], proposing a uniform current density in the oxide over the cross section of the electrode area for transition metal oxide based MIM cells such as NiO[69], CoO[70] and Fe_2O_3[71]. However, there is a controversy in the literature if the ON state is induced by a single filament[70-71], suggested by ON resistance independent of the electrode area, or multiple conducting filaments[69,72]. In the former case the reduction of the device area does not reduce the operation current what implies an increase of the current density per cell with scaling. In other words, feasibility of higher density memories cannot be guaranteed due to the heat produced by large currents required to program them. In the latter case, if the LRS is composed of multiple conducting filaments the currents should decrease upon the scaling down of the cells. The multiple filamentary paths picture has been corroborated by different authors in literature as Ahn et al. who reported in a Ti-doped NiO system a decrease of the programming currents with scaling down of the

cell size. Son et al[72] observed multiple filamentary paths by AFM analysis in NiO (see figure 1.9).
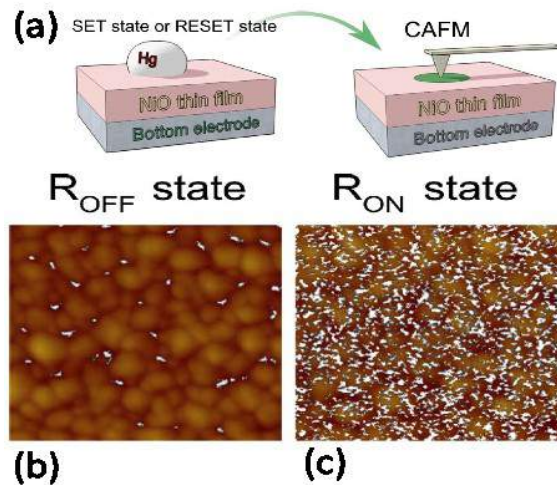

Figure 1.9: (a) Removable Hg drop top electrode on NiO thin film to induce ON and OFF states (left), and CAFM scanning for ON and OFF states after the removal of the Hg drop (right). CAFM images of the NiO thin film for the OFF state (b) and ON state (c) by applying a bias of 0.1V. (Image taken from reference 72).

The authors employed an Hg drop as top electrode to switch NiO. After turning the NiO into ON and OFF state, they removed the Hg drop and analyzed the surface by conducting AFM. At the ON state the AFM scanning revealed multiple conducting paths on the surface what supported the formation of multiple conducting paths and not single. Alternative switching model has been proposed by Inoue and co-workers[71] who proposed a model based on an "electric faucet" formed at the interface barrier. The model postulated that the bulk region after the electroforming becomes a conductive region by multiple conductive filaments or domains. The total current at the ON state (low resistance state) is localized and controlled by the mentioned "electrical faucet" located at the high resistance interface, while the OFF state current (high resistance state) flows almost homogenously over the highly resistance interface. In addition, the SET and RESET voltages values did not depend

on the oxide thickness what led to consider the SET/RESET processes as interfacial phenomenon. The authors regarded the "faucet" as a tip of a particular filament or a conductive domain going into the interface region. The area of the faucet must be much smaller than the whole area of the electrodes, and the resistance at the ON state can be considered area independent.

1.3.2.3   Valence Change Memory (VCM)

The typical MIM cell of a valence change memory system consists of an active electrode (AE), an ohmic counter electrode (CE) and an insulating layer in between. Many binary transition metal oxides and complex oxides with at least one transition metal display bipolar switching characteristics, despite the electrodes do not inject metal cations unlike ECM cells. This lack of cation insertion could be due to either the metal is not easily oxidized (Pt, Au, etc.) or the oxidized form is hard to be reduced back to metal (Ti, Al, Nb, etc.). There are several switching mechanism designated in literature within VCM cells. First, we describe switching behavior based on an n-type filament. The active electrode is a metal with a high work function and low oxygen affinity (e.g. Pt, Ir, etc.) while for the counter electrode a metal with a low work function and high oxygen affinity is preferred. In most MIM devices, an electroforming process is required before regular resistive switching can be performed. Most papers in literature report a SET upon a negative bias applied to the active electrode, and a RESET process under positive polarization. In the valence-change mechanism, the creation and electromigration of oxygen vacancies induces the distribution of the charge carrier density and the valence states of cations. The devices where the resistive switching is governed by this mechanism are characterized by showing bipolar behavior.

The electroforming process current is limited by a current compliance, and the forming voltage results larger than the subsequent SET voltages. The achievement of the forming process is usually indicated by a sudden increase in the current. During the electroforming, an electrochemical oxidation at the anode (counter

electrode) may occur inducing the evolution of molecular oxygen and the corresponding injection into the oxide of oxygen vacancies, which are drifted towards the cathode (active electrode) by the electric field. A highly n-conducting region is originated due to accumulation of the oxygen vacancies (donor defect) and a reduction of the valence of transition metal cations. This conductivity increase produces a drop of the electric field in this region reducing the mobility of the oxygen vacancies. This oxygen vacancy enriched region can be compared to a virtual cathode, which propagates from the cathode towards the anode mainly along extended defects (see figure 1.10). The active electrode represents an electrostatic barrier modified by the applied voltage. In single crystals and epitaxial thin films, it was demonstrated that the oxygen vacancies migrate through the dislocation network and originate a change in the conductivity as visualized in ternary oxide $SrTiO_3$ by local conduction atomic force microscopy (LC-AFM) [73].
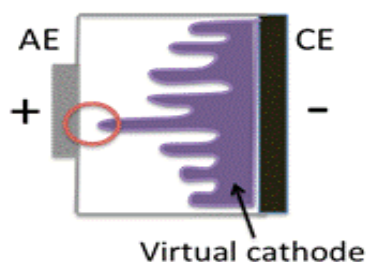

Figure 1.10: Sketch of a VCM cell after the forming process with the enriched oxygen vacancy region, so called virtual cathode, growing from the counter electrode towards the anode. The circle encloses the accumulation/depletion oxide region of oxygen vacancies responsible of the switching.

For amorphous and nanocrystalline oxide thin films, the conducting filament can be formed anywhere in the cross section of the cell. This behavior can be explained by a diffusion of oxygen vacancies (positively charged) attracted from the "tip of the virtual electrode" to the active electrode. This yields significant narrowing of the electrostatic barrier and switches the system into the low resistance. The

electron transmission will be increased due to a narrow barrier and a lowering of the Schottky energy barrier, which leads to quasi-ohmic I-V characteristics.

The formation and disruption of Ti_nO_{2-n} filaments (composed of a high density of oxygen vacancies) was probed to be the resistive switching origin in Pt/TiO$_2$/Pt device by high-resolution transmission electron microscopy (HR-TEM) together with *in situ* current-voltage and low temperature (~130K) conductance measurements [74]. On the other hand, under a positively biased active electrode the oxygen vacancies are repelled from the near vicinity, breaking the local contact with the active electrode. The electrostatic energy barrier is restored returning the cell into the high resistance or OFF state[62].

Non-volatile resistive switching effect in SrZrO$_3$ doped with 0.2% of Cr thin films was reported by Beck et al[75], who associated the origin of the bipolar switching to intrinsic vacancies and impurities with different oxidation states that formed a series of states within the energy gap. Reproducible bipolar resistive switching was also observed in Cr-doped SrTiO$_3$ single crystal. The low resistance state was claimed to be originated from a change in the bulk property, in particular by charge carriers at the bulk after perceiving large conductive changes at current-temperature scans, and the emission of trapped carriers[76].

Summarizing, the operational fundamentals of the bipolar switching are based on the local Schottky barrier modulation of the active electrode/oxide interface. This is induced by voltage driven accumulation and depletion of oxygen vacancies via negative and positive electric pulses respectively within the oxide near the active electrode (see figure 1.11). In addition, reports about resistive switching interface-type where the change of resistance takes place at the whole metal/oxide interfacial region were also suggested. In cells exhibiting this type of switching mechanism a scaling of the device resistance with the electrode area is observed. Thus, the switching effect is based on a homogenous electric field-induced change of the interface resistance over the whole electrode area[77]. This switching mechanism has been associated to describe the bipolar switching behavior in different materials such as manganites peroskites[78-80], transition metal oxides[81] (TMO) and ZnO[82]. The

authors appealed the hypothesis of oxygen vacancies migration with vacancy pile-up at the interfacial region as the active process to trigger the resistive switching effect.
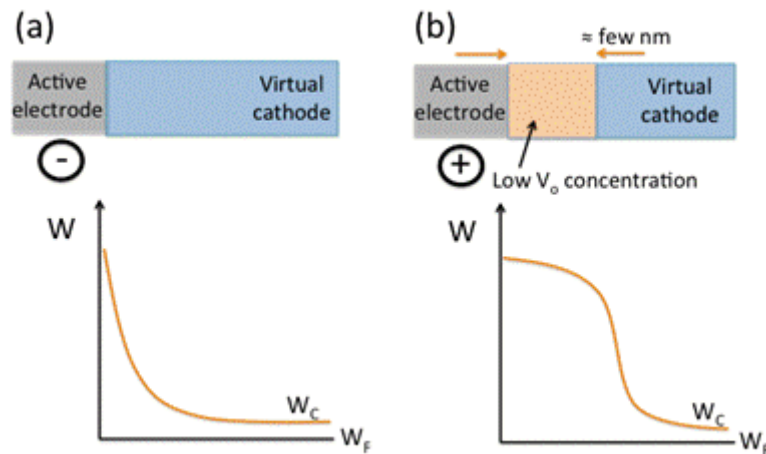

Figure 1.11: The blue network illustrates the extended defects which show n-conductivity due to accumulated oxygen vacancies, while the orange network represents the depletion layer at the interface corresponding to the OFF state. (a) ON state by a negative polarity attracting oxygen vacancies, which turn the interface into ohmic contact. Below, illustration of the corresponding band diagram where W, W_C and W_F denote the energy, the energy of the conduction band, and the Fermi energy respectively. (b) OFF state induced by positive polarity repelling oxygen vacancies, and increasing the electrostatic barrier. Below, illustration of the corresponding band diagram where W, W_C and W_F denote the energy, the energy of the conduction band, and the Fermi energy respectively.

However, in some cases the authors suggest that the oxygen vacancies are formed and annihilated by electrochemical reactions at the interface depending on the bias polarity as claimed for $Pt/TiO_2/Pt$[83] devices. In this way, the anodic reaction induces the oxygen vacancies formation due to the migration of oxygen atoms from the TiO_2 to the anode. On the other hand the cathodic reaction drives to oxygen vacancies annihilation as oxygen atoms move back towards the interfacial region.

In this section we have described the main resistive switching mechanism observed. In what follows we will focus on the literature on resistive switching behavior reported for HfO_2-based memory devices.

1.3.3   Resistive switching and Hafnium oxide

Literature offers us a wide variety of different studies reported on resistive switching in HfO_2-based memory devices. This diversity is just an evidence of the elevated number of parameters that have a potential impact on the performance of the memory devices. In this way, we can find in literature reports related to the effect on the device performance of the thin film growth conditions, the post-annealing processes as well as the metal electrodes selected to form the metal/insulating/metal (MIM) cell. In order to obtain a deeper insight of HfO_2 thin films properties and the underlying switching mechanism, diverse characterization techniques have been employed, such as electron energy loss spectroscopy (EELS)[84], scanning transmission electron microscopy (STEM)[84], high resolution transmission electron microscopy (HR-TEM)[85], X-ray photoelectron spectroscopy (XPS)[85,86], conducting atomic force microscopy (C-AFM)[87-88] and high-resolution Rutherford backscattering spectroscopy (HRBS)[89].

1.3.3.1   Growth conditions effect and metal electrodes relevance

The HfO_2 growth conditions can strongly affect the electrical transport properties of the material. In this way, Hildebrandt and colleagues modified the electrical transport properties of HfO_2 inducing oxygen vacancies[90]. The HfO_2 thin films were fabricated by using oxygen engineering reactive molecular beam epitaxy (RMBE) with an oxygen flow rate between 0 and 2.5 sccm. The largest measured band gap corresponded to the stoichiometric HfO_2, while it decreased for compounds fabricated with oxygen flow both lower and beyond the ideal value

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(stoichiometric HfO_2). The oxygen vacancies originate a defect band at the Fermi level and a reduction of more than 1eV of the band gap was observed.

The effect of metal electrodes with high oxygen affinity, and post metal-deposition annealing (PMA) has been reported to enhance significantly the performance of bipolar HfO_2-based memory devices. In this way, HfO_2-based ReRAM devices improved significantly the memory performance using into the anodic side thin layers of different materials as Ti[91,92] and AlCu[92,93]. Devices consisting of $TiN/Ti/HfO_2/TiN$ structure[91] with a Ti thin layer inserted between the HfO_2 and TiN, showed high reliability , fast switching operation (5 ns), large resistance window ($>10^3$) and low operation voltage ($\sim$ 3V). The Ti capacity to react with the oxygen from the HfO_2 resulted in the formation of HfO_x ($x\sim1.4$) and TiO_x. Walczyc et al[86] demonstrated by XPS analysis that a Ti overlayer on HfO_2 scavenges oxygen from the interface, and this gettering activity is increased with the temperature. Lee et al fabricated $TiN/Ti/HfO_2/TiN$ devices with Ti[92] and AlCu[93] thin layers as reactive capping layers and compared their effect on the memory performance. Despite both devices exhibited bipolar resistive switching behavior, AlCu device exhibited small resistance ratio ($\sim$5) and required high compliance to sustain stable switching behavior. However, Ti device was more robust, with lower operation currents ($<$) and larger resistance ratio ($>$100). The authors attributed the better performance with Ti layer to the superior oxygen gettering capacity of Ti that yields a larger amount of oxygen vacancies at the interfacial region. The improvement of the switching properties by using a reactive metal layer was related with the switching mechanism. This was associated to trapping and detrapping process, so that the resistance ratio increases with increasing trap levels in the insulator. Since oxygen vacancies act as trapping centers, then it could be reasonable that devices with Ti layer exhibited better bipolar resistive switching properties since it originates larger amount of oxygen vacancies, i.e., traps centers at the HfO_x than that of AlCu devices.

In this context, the impact of top metal electrode on the conduction mechanism of HfO_2-based MIM cells within a temperature range was reported by C.

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Vallée and coworkers[94]. The leakage currents measurements were carried out at Al, Cr, Au/HfO$_2$/Pt devices with Pt electrode positive biased to study transport phenomena at the metal/HfO$_2$ interface. The experimental data at high electric field revealed that the leakage current density is governed by Fowler–Nordheim (FN) tunneling for Al and Cr/HfO$_2$/Pt devices with barriers heights of 0.77 and 0.95 eV. Nevertheless, the leakage current density obtained for the Au/HfO$_2$/Pt device at high electric field could not be fitted by FN law. It exhibited instead a good fitting by the Schottky emission theory, Au/HfO$_2$ interface acting as a Schottky barrier with a height of 1.06eV. The authors claimed that metals with high oxygen affinity, as Cr and Al, act as oxygen sinks originating more oxygen vacancies providing n-type doping. In contrast, Au electrodes with low oxygen affinity do not react with the HfO$_2$. The oxygen vacancies induce a narrowing of the depletion layer width and a higher electron tunneling probability from the cathode to the HfO$_2$. Evidences of oxygen vacancies in the switching origin were also described by Goux et al[95]. They reported the effect of the chamber atmosphere and the Pt top electrode thickness on TiN/HfO$_2$/Pt ReRAM cell operation. The switching mechanism described for this cell is based on the formation/annihilation of oxygen vacancies conducting filaments and the effective switching reset relies on filament re-oxidation and the availability of oxygen in the filament surroundings. An O$_2$ poor ambient resulted in the degradation of the reset switching yield regardless the thickness of the Pt layer. Evacuation of oxygen through Pt layers might occur during electroforming due to the high mobility of oxygen species in Pt layers. Thus, larger oxygen evacuation is expected for thinner Pt layers (shorter diffusion distance) and ambient with low O$_2$ partial pressure. Several samples were set to the LRS applying high current compliance (50 mA) resulting in irreversible breakdown of the cell. Subsequently, the cells were annealed at 500°C for 3 minutes in pure oxygen atmosphere leading to an increase of the cell resistance, and most of the cells exhibited again resistive switching after annealing. This effect is related with an oxidation process of part of the filamentary region due to oxygen diffusion through the Pt at 500°C and supports the interaction between the filament and the atmosphere at high temperatures. The authors claimed that the

use of oxygen barrier layer would be required for better cell functionality in order to avoid the diffusion of oxygen to the atmosphere. The effect of oxygen concentration was also reported to affect the work function of Ru in Ru/HfO$_{2-x}$/TiN devices[96]. In this way, low oxygen concentration at the interfacial region led to a reduction of the Ru work function, while a high oxygen density increased it. As a consequence, variation in the oxygen concentration at Ru/HfO$_x$ interface should be responsible of the unstable barrier height of the interface and the wide set voltage value dispersion.

1.3.3.2 Switching mechanism

Regarding the switching mechanism in HfO$_2$ devices, most of the literature reported attributes the resistive switching effect to the filamentary model. This describes the resistive switching based on the formation and rupture into the HfO$_2$ matrix of conducting filaments composed of percolated oxygen vacancies. A widely accepted mechanism is described here below. During the electroforming process (if required) oxygen is extracted at the anode and produces positively charged oxygen vacancies that migrate to the cathode. The filaments grow from the cathode to the anode, so that the filament connects both electrodes as the device switches to the LRS. When the filament is partially ruptured or dissolved the device switches back to the HRS. The filament model is suggested independently of the type of resistive switching observed, i.e., both for unipolar [6, 97-100] and bipolar [6, 100-105] behavior. These two resistive switching types discern in the mechanism that leads to the rupture of the conducting paths. On the one hand, at devices displaying bipolar behavior the reset process is attributed either to the partial re-oxidation of the filaments by oxygen ions that are repelled from the cathode (former anode), or to the rupture of the filament at the anodic interfacial regions as the oxygen vacancies are repelled from the anode (former cathode). On the other hand, in unipolar switching devices it is considered that the filaments are ruptured or dissolved by current Joule heating. A transition from bipolar to unipolar behavior was described by Chan et al[6] after an annealing treatment at 400°C and O$_2$ ambient. The authors

attributed that effect to the strong influence of oxygen content and oxygen-related defects on the switching properties of the HfO_2 film. In this way they considered that the O_2 atmosphere during the annealing treatment could produce the passivation of oxygen vacancies inducing changes in the film composition and the switching properties. It is worth to mention reports that describe devices where coexist both bipolar and unipolar behavior. Lee et al[85] described such coexistence in $Au/HfO_2/Pt$ device, although bipolar displayed unstable behavior and the resistance ratio between HRS and LRS was low compared with that of other materials displaying the two switching modes. The authors associated this feature to the higher HfO_2 bandgap (5.6 eV) in comparison with that of TiO_2 (3.2 eV) and ZrO_2 (4.8 eV). Coexistence of unipolar and bipolar switching was also observed at $TiN/HfO_2/Pt$ devices by Goux et al[100]. According to the authors both switching behaviors may be induced independently of the preceding switching history. Besides, multiple intermediate resistance (IR) states were observed attained consequence of a gradual reset process. The IR levels were achieved after applying different reset voltages values to the LRS. The gradual reset was attributed to progressive annihilation of the oxygen vacancies conducting paths close to the Pt anode. Temperature-dependence measurements revealed retention loss events above 50°C that were associated to thermally activated mobility of the oxygen vacancies. This mobility could result in a chain rearrangement of the oxygen vacancies leading to an undesired switch to the LRS. Although the IR levels result attractive for a potential memory multilevel cell operation to be used in a memory application, they should display the stability, reproducibility and retention properties of the HRS and LRS.

Direct observation of reversible creation and annihilation of individual local currents paths was stated by using ultrahigh-vacuum conductive atomic force microscopy on HfO_2/SiO_2[87]. Areas of 500x500 nm^2 were scanned increasing the tip bias 0.1V each time the scanning was completed. Doughnut-shaped leakage spots (~50 nm diameter) started to appear at a tip bias value of 4.2V. It was observed that the spots quantity and the current passing through them increased as the tip bias enhanced. These scans were conducted at two different areas on the surface. Nice

reproducibility was obtained at both tip bias polarity for both the tip bias value, at which the first spots appear, and the increase rate of leakage spots density. Similarly, enhanced conductive atomic force microscopy (ECAFM) was used to analyze the RS phenomenon in amorphous and polycrystalline HfO_2 thin films[88] (see Figure 1.12). At polycrystalline MIM capacitors, ECAFM obtained *in situ* observation of bipolar resistive switching at nanometer scale. Amorphous samples did not reveal any RS effect. The results demonstrated that RS occurred only at polycrystalline HfO_2 films, and took place along grain boundaries. The authors associated that to the higher conductivity of the grain boundaries than that of the grains. Such higher conductivity at the grain boundaries was attributed to a large density of oxygen vacancies therein.
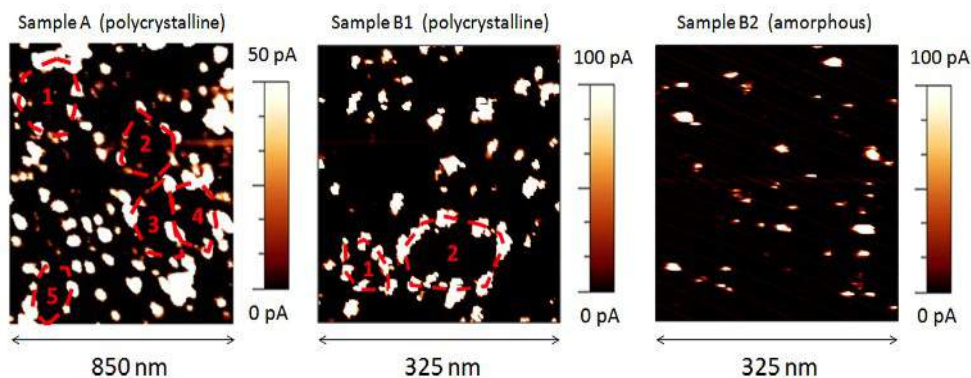

Figure 1.12: Current maps obtained after scanning the surface of polycrystalline samples (left and centre) and amorphous (right) with the tip of a C-AFM. At left and centre images grain boundaries more conductive than grains can be discerned. Amorphous sample displays more homogeneous leaky sites arrangement (image taken from reference 88).

In the same way, Wu and colleagues achieved direct visualization of multiple conductive filaments in ultrathin HfO_2-based ReRAM memory device by HRTEM along with EELS for nanoscale chemical analysis[84]. Their physical analysis showed that nucleation and rupture of conducting nanoscale metallic filaments are responsible for

the resistive switching. Oxygen ion drift in the vicinity of the filament was considered to play a significant role in the SET/RESET processes.

In contrast to filamentary switching, other authors proposed bipolar resistive switching based on the modulation of the interface resistance by spatial distribution of the oxygen vacancies concentration at interfacial regions[94,96]. The SET/RESET processes would be associated with an electric-field drive accumulation/depletion of oxygen vacancies at the metal/oxide interface. A negatively charged electrode will attract the oxygen vacancies turning the Schottky barrier into an ohmic contact and triggering the low resistance state; under positively bias such vacancies will be repelled from the interfacial region turning the device back to the high resistance state. The main difference between the interface switching mechanism and the filamentary model is that the former should exhibit scaling of the device resistance with the electrode area, while the current density at the latter should not scale down as contact area shrinks.

1.3.3.3   Post-annealing treatments effect

Finally, the post-annealing treatments effect on resistive switching properties was also explored. Such annealing treatments induced an increase of the crystallinity degree and usually also led to the introduction of grain boundaries, dislocations, and crystalline defects in the HfO_2 layer, e.g., oxygen vacancies or metal ions. Grain boundaries and dislocations provide diffusion paths for bulk defects that could percolate and form conducting paths through the bulk. Memory performances were studied according to the post-annealing temperatures in $Pt/HfO_2/Pt$ devices[106]. The as-deposited HfO_2 films were annealed within a temperature range for 2 minutes in O_2 ambient and they were found to crystallize at a temperature 600°C according to XRD results. Sample annealed at low temperatures (300-500°C) exhibited a poor endurance of less than 30 cycles. However, the devices that underwent annealing at 600°C showed reversible and stable resistive switching behavior. It was accounted for the easy migration paths for the oxygen vacancies, provided along the grain

boundaries to form local conducting filaments. These results would agree with the results described above on *in situ* direct observation by C-AFM[88] where conductive filaments exhibiting resistive switching are mainly formed at the grain boundaries, which contain intrinsic high density of oxygen vacancies. A significant further point is that the annealing treatments also intensify the oxygen gettering capacity displayed by some metals as showed by Nakajima and coworkers[89]. They used high resolution RBS to study the oxygen gettering by a titanium overlayer on $HfO_2/SiO_2/Si$. It was found that oxygen was released from the SiO_2 into 1.8 nm Ti layer. It is something reasonable as to form HfO_2 is energetically more favorable than SiO_2. Upon annealing at 330°C in UHV and with thicker Ti layer (7.8 nm) oxygen released from the HfO_2 was also observed even remaining SiO_2 layer.

Although there is still an uncertainty about the mechanisms the resistive switching is based on, the literature seems to point at the significant role of the oxygen vacancies in the resistive switching as well as physical processes occurring at the anodic interface. All the data and information gathered from literature will be taking into account and consider during the treatment and interpretation of the results obtained along the development of this thesis.

1.3.4   Trends and perspectives at ReRAM

As described in previous section, ReRAM is one of the most promising candidates for next negation of non-volatile memory due to inherent properties as its simple structure, high switching speed, and high scalability. Its compatibility with the current CMOS technology ensures a promising scaling down prospective.

In this matter, several papers focused on the integration of ReRAMs cells into the conventional CMOS memory architecture to achieve high-density non-volatile ReRAM. Rozicki and coworkers[107] integrated ECM cells using electron beam lithography to define sub-100-nm openings, which further become the active switching area, in polymethylmethacrylate (PMMA) layers used as dielectric in between electrodes. The authors reported endurance superior to 10^{10} write cycles

for a single memory cell. Regarding TCM cells, integration of NiO-based memory cells with 180 nm CMOS technology was also communicated[108]. A reduction of the switching parameters dispersion was achieved by integrating an IrO_2 thin layer between NiO and electrodes. The IrO_2 enhanced the crystallinity of NiO at NiO-IrO_2 interfaces and would also help to stabilize local oxygen migration for the formation and rupture of conducting filaments resulting in more stable switching parameters. The device displayed excellent temperature stability up to 300°C, and write endurance of 10^6 cycles. Integration with 180 nm CMOS technology was also confirmed in an 8 kbits memory array composed of TaO_x VCM cells[109]. The memory cell displayed an endurance of 10^9 cycles and switching speeds of 10 ns. The switching operation was confirmed to be based on a redox reaction that changed the interface energy barrier between bulk TaO_x and the anode. Hard X-ray Photoemission Spectroscopy (HX-PES) confirmed the presence at the interface region of TaO_{2-} and Ta_2O_{5-}. As positive bias is applied at the anode, oxygen ions drift from bulk TaO_x towards the anode and oxidize the TaO_{2-} leading to the formation of Ta_2O_{5-} which enlarges the band gap in a change of the resistance state to HRS. On the contrary, a negative bias induces the Ta_2O_{5-} reduction decreasing the energy barrier and triggering the switching to LRS.

On the search towards superior computer performance and memory density, crossbar arrays architectures were proposed as non-volatile memory holding the expectative of a reduction of energy consumption. The crossbar arrays consist of a set of parallel bottom electrodes and perpendicular top electrodes with a thin layer of resistive switching material in between. Each capacitor-like structure crosspoint of the crossbar represents a memory cell where binary information can be stored as HRS or LRS. However not negligible drawbacks have still to be overcome at memristive crossbar arrays as the interferences from sneak-path currents through neighboring cells. As all the cells in a row are connected to each other by the top electrode and in a column by the bottom electrode, the currents through parallel elements affect significantly to the voltage drop and current over the addressed cell. Linn et al[110] proposed to overcome the sneak currents paths by connecting two

bipolar memristive elements A and B antiserially into one complementary resistive switch (CRS). CRS makes use of the same principle as a CMOS inverter, in which one of the transistors is always OFF. Thus, the CRS state associated to 0 corresponds to element A and B in HRS and LRS respectively. On the other hand, the opposite situation when element A and B are in LRS and HRS respectively, represents CRS state 1.Therefore, the total resistance of a CRS is always high: R_{CRS} = $R_{HRS}+R_{LRS}\sim R_{HRS}$ (as $R_{LSR}<<R_{HRS}$). This structure achieves significant reduction of the static power and makes feasible the application of large passive crossbar arrays architectures.

The similarity between biological synapses and memristor performance has been also reported on neuromorphic circuits that can possibly offer both high connectivity and elevated density required for effective computing. Similar to the conductance of a memristor, the synaptic weight refers to the strength of connection between two neurons, which can be modified by controlling the charge through it. Jo and coworkers[111] designed a crossbar of memristors that consisted of layered device structure incorporating a co-sputtered active layer with Ag/Si mixture gradient. This resulted in the formation of Ag-rich region (low resistance) and Ag-poor (high resistance) region and the formation of a uniform conduction front in between the two regions. Under a positive voltage bias, Ag ions move from the Ag-rich region to the Ag-poor region increasing the synaptic weight, and vice versa. Thus, the device conductance can be adjusted by tuning the duration and sequence of the applied programming voltage.

Thus, the potential application of memristor into different high density systems focused on a superior computing efficiency seems certainly promising.

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CHAPTER 2

Experimental methods and device fabrication

This chapter gives an overview of the fabrication techniques and experimental methods used in the thesis. The description of the device fabrication is also provided together with the instruments and measuring protocols utilized to characterize both the physical and electrical properties of the devices.

2.1 Fabrication techniques

2.1.1 Atomic Layer Deposition (ALD)

2.1.1.1 Introduction

The origin of atomic layer deposition (ALD), originally named atomic layer epitaxy (ALE), has been traced back to a patent published in the 70´s by Suntola and co-workers[1], though there is a less known origin which locates its roots in experiments conducted in the 60´s to grow GeO_2 by the group of Professor Aleskovskii in the Soviet Union[2]. It seems that at the beginning the two groups were unknown of each other´s work, until communication between both groups started at the 80´s. Originally ALD was developed for deposition of epitaxial layers of II-IV or III-V semiconductors. However, the necessity of ultra-thin films brought about by the scaling down of semiconductor devices together with ALD inherent advantages, produced an increasing interest towards ALD technique from the metal oxide semiconductor field effect transistors (MOSFETs) and high-density memory devices[3,4]. Nowadays, ALD is considered as one of the most promising technique for the

fabrication of high quality thin films as it offers good uniformity, low deposition temperatures, unprecedented atomic scale thickness control and excellent conformality, i.e., the capability to coat every exposed surface regardless the physical geometry with uniform thin film. The thickness control lies on the layer by layer grown that governs ALD processes and leads to ideal growth rates of one monolayer per cycle (1ML/cycle). However it is the self-limitation for precursor chemisorption, and the sequential exposure of reactants and precursors, the distinctive characteristic between ALD and chemical vapor deposition (CVD). Precisely, the self-limited adsorption of the precursors is the most remarkable ALD characteristics as described in section 2.1.1.3.

2.1.1.2   Fundamentals of ALD

ALD technique is a type of chemical vapour deposition based on self-limiting chemisorption or gas-solid reactions between precursor and surface. The chemical reaction proceeds via alternate exposure of the substrate surface to precursor molecules in gas phase, which are chemically tailored to react saturatively with the surface groups. An inert gas typically N_2 or Ar purges the chamber between precursor injections to take away the excess of reactants and the gaseous reaction by-products from the chamber and desorbed materials from the chamber walls.

Usually one growth cycle is composed of a sequence of four steps (see Figure 2.1):

1-A first step produces the substrate surface activation by the exposure to first precursor, coating it with chemically adsorbed hydroxyl (-OH) functional groups until surface saturation. Further chemical adsorption process ceases.

2-A purging gas flows into the reaction chamber to ensure the elimination of unreacted molecules of precursors and other sub-products of the process in gas phase or physically absorbed on the surface.

3-The substrate surface, chemically complementary to the second precursor, is exposed to it. The second precursor is chemically adsorbed until the surface is saturated and no more chemical adsorption occurs.

4-A second purge process takes place to remove unreacted molecules of precursors and other sub-products of the process in gas phase or physically absorbed on the surface, which is chemically complemented to the first precursor.
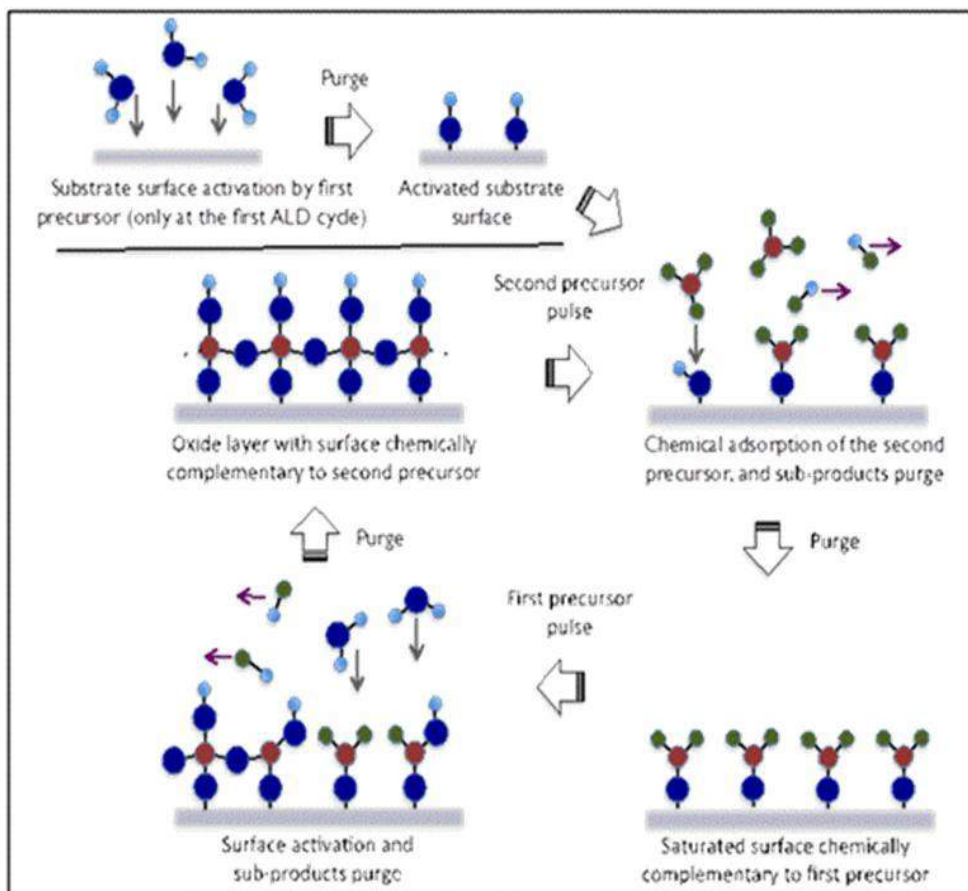

Figure 2.1: Schematic of the first ALD cycle and consecutive. Chemical agents in the ALD process introduced into deposition chamber as gases, and supplied in pulses delivered at different times. A purge gas separates reactants from each other. Each reactant pulse chemically reacts with the wafer surface leading to a self-assembling monolayer grown process.

The grow sequence is repeated as many times for the desired film thickness. Unlike CVD, in ALD reactions with a G value as negative as possible are preferred as the cycle time fluctuates depending on the aggressiveness of the film-formation reactions.

The precursor molecules react or chemisorb with the surface group saturatively and no added adsorption occurs after the formation of the chemisorbed layer. The saturated conditions of the reaction entail a self-limited growth of the thin film, i.e., the amount of material deposited at each cycle is constant. The main drawback of the ALD is that the fabrication rates are low as under ideal conditions the film grows one atomic layer at a time (1ML/cycle).

The ALD process has some parameters to consider as the deposition temperature (or reaction chamber temperature), the precursors and the purge process length that could influence onto thin film properties.

2.1.1.3   ALD characteristics and applications

The self-limited chemisorption of the precursors makes the conformality intrinsic to the ALD process. However there are several nanostructures no limited to planar devices as nanoscale features with a high aspect ratio, such as nanoscale trenches or holes, where to ensure uniform coating requires much more control over deposition parameters. Conformal films deposition entails the saturated chemisorption of precursors over the entire surface what is controlled by several factors as molecule flux, chemisorption probability and surface diffusion. In three dimensional nanoscale structures with high aspect ratio, the saturation could be different on the flat surface and on the walls or bottom of the holes, leading to a non uniform layer thickness. The saturation enhancement could be achieved by an increase of the exposure time as well as through surface modification which would improve the precursor chemisortion or sticking probability.

Another factor to consider is the purging between the precursor and reactants exposure since if it is not enough it could lead to CVD growth and to an

inappropriate removal of unreacted precursor molecules and/or byproducts. Precursors reaction in gas phase could also occur into the chamber before reaching the substrate surface. On the contrary, an excessive purge time could produce undesired contamination of the film due to reaction sub-products and/or the decomposition of the precursor on the surface.

The effects of the molecular flux was reported by a model and contrasted with experimental results for HfO_2 and water establishing that the necessary exposure time for heavy molecules is longer since the molecular flux is inversely proportional to the molecular weight[5]. The relevance of the exposure time and sticking probability of precursor molecules was studied via nanopores and scanning electron microscopy (SEM). The results indicated that by varying the exposure time or working pressure a satisfactory saturation can be achieved. Enhanced precursor chemisortion on the inner surface of the nanopores was shown under higher working pressure resulting in a reduction of the exposure time required for saturation[6].

The inherent self-limiting deposition process by alternate exposure also allows an atomic level control both the thickness and the composition. Thus, ALD is an optimal deposition technique to fabricate atomic size films and multilayer or nanolaminate structures. However atomic scale thickness control is not always assured as the growth rate can be lower than the ideal 1ML/cycle. There are several factors that produce a deviation from the ideal layer by layer behavior[7,8] such as steric impediment of molecules and the formation of islands during the early growth stage, which changes the growth rate producing a non-linear film thickness vs. the number of cycles.

Another significant characteristic of ALD is the capacity to grow at low temperatures thin films of high quality. A low impurity level is expected compared with CVD as a complete reaction is expected between precursor and reactant at low temperature. However the substrate heating is frequently needed both for the surface reaction with reactant and for precursor molecule chemisortion. Deposition of Al_2O_3 using trimethylaluminum (TMA) and water has been reported even at

33°C [9]. Other examples of ALD depositions below 50°C including TiO_2, SiO_2, B_2O_3 and CdS are summarized[10]. The importance of the ALD capacity to grow materials at low temperature enables the introduction of this technique on a wide range of applications as polymer encapsulation[11], polymer-based devices and coating heat-sensitive materials such as biomaterials or polymers. ALD deposition on plastic substrate also allows flexible electronic devices, as transparent thin film transistors fabricated on glass and polymer substrates at 125°C[12]. Another remarkable benefit of low temperature ALD is the possibility of using photolithography methods during the fabrication processes and subsequent lift-off steps as the resist is not degraded.

Therefore the potential applications of ALD cover different research fields. One of the most intensive field studied is the deposition of high-k gate oxides for MOSFETs whereby it is expected to solve the leakage currents caused by the scaling down of the devices[13,14]. The field effect transistors (FET) with 1D channel materials are another noteworthy emerging nanodevices where ALD is used for the fabrication of high k gate oxides[15], as well as non-volatile memory (NVM) devices, including nanocrystals memory (NC)[16], resistive switching memories (ReRAM)[17] and phase change memory (PRAM)[18].

2.1.1.4 ALD and HfO_2

In this work we employed the ALD technique for growing HfO_2 thin films during the fabrication of metal/insulator/metal devices (MIM). In literature different Hafnium precursors have been reported; hafnium halides precursors such as $HfCl_4$ resulted in significant residual chlorine content[19] (1-3% at.) and produced noxious byproducts as hydrochloric acid. The complicated removal of chlorine even by annealing[20] affected film properties as the dielectric performance. Therefore chlorine-free precursors were developed and used as alkylamides: hafnium tetrakis(diethylamide) $Hf[N(C_2H_5)_2]_4$ (TDEAHf)[21], hafnium tetrakis (ethylmethylamide) $Hf[N(CH_3)(C_2H_5)]_4$ (TEMAHf)[22,23] and hafnium tetrakis (dimethylamide) $Hf[N(CH_3)_2]_4$ (TDMAHf)[24,25], which led to HfO_2 thin films with

lower impurity levels than those grown from $HfCl_4$. A study dealing with the temperature effect on the HfO_2 films properties[24] revealed that uncompleted reaction between precursor and reactant at lowest temperature (205°C), and thermal decomposition at the highest temperature (400°C), were the cause of increase contamination content and deterioration of thin film properties. No dependence of the film properties on the pulse length was also reported as well as linear relation between film thickness and number of cycles, denoting self-limited growth. Hackley et al. [26] characterized by atomic force microscopy (AFM) smooth HfO_2 films, grown by using TEMAHf, and found that roughness increased with thickness. The HfO_2 film crystallization phase was also determined, being predominant the monoclinic phase as determined by X-ray diffraction (XRD) analysis. The major crystalline phase in HfO_2 thin films was also found to be monoclinic in other works[27,28]. Concerning deposition processes at low temperatures Biercuk et al.[29] demonstrated a process that allows ALD-grown dielectric films to be patterned using lift-off where the films were deposited at 100°C-150°C using TDMAHf for the case of HfO_2. Also the effect of use different oxygen sources as H_2O and O_3 on film properties was studied[30]. Temperature-dependent leakage current analysis revealed leakage currents densities three orders of magnitude smaller at films grown using O_3 than that of the films using H_2O. A smaller carbon impurity content determined in films grown with O_3 was attributed to a high oxidation potential.

The HfO_2 thin films deposition process during this thesis covered a range of deposition temperatures (125°C-350°C) and purge times values (1s to 35 s). The oxygen source and hafnium precursor employed were deionised water and tetrakis(dimethylamido)hafnium respectively. Millipore Advantage A10 filtering system provided purified deionised water (18 M cm^{-1}), while Sigma Aldrich provided hafnium precursor. Additional deposition process information will be specified in advance chapters.

2.1.1.5   Chemisorption mechanisms

Three main chemisorption mechanisms have been recognized for self-terminating ALD reactions: ligand exchange, association and dissociation[2]. The three mechanisms are schematically illustrated in Figure 2.2.

In ligand exchange mechanism the precursor molecule ML_n is split on the surface due to the reaction between the ligand L and a surface group a, forming a volatile compound that is released as gaseous byproduct aL. The rest of the molecule chemisorbs to the surface as ML_{n-1}.

In dissociation mechanism the precursor molecule is split onto reactive sites on the surface, while in association mechanism a coordinative bond is formed between the precursor molecule and a reactive site on the surface being chemisorbed without a release of ligands.
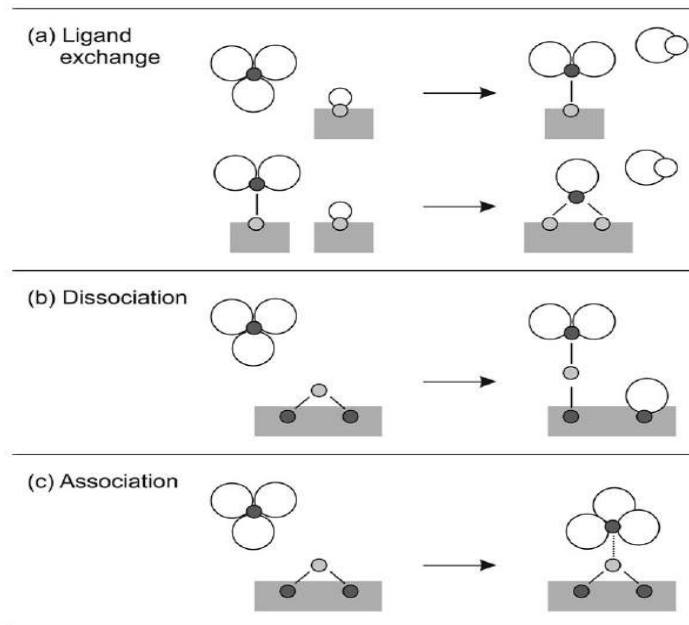
Figure 2.2: chemisorptions mechanism identified for ALD: (a) Ligand-exchange, (b) dissociation and (c) association. Figure taken from reference [2].

Concerning the HfO_2 thin films deposition in this thesis, as it was mentioned earlier we employed deionized water and tetrakis(dimethylamido) hafnium (TDMAHf) as oxygen and hafnium source respectively. The literature suggests a possible mechanism for the ALD reaction of water and hafnium alkylamides[31-32] as TDMAHf (Figure 2.3). The proposed mechanism consists of two steps: first the hafnium precursor reacts with a hydroxylated surface to eliminate two alkylamine ligands (Figure 2.3 a-b). This step entails the rupture of Hf-Nitrogen bond and the formation of Hf-Oxygen bond, together with a concurrent deprotonation of the hydroxilated surface by the amide ligand to form a volatile byproduct ($H-NMe_2$). These reactions are highly exothermic due to the weak acidic nature of the amines, and the weakness of the metal nitrogen bonds in comparison to the metal-oxygen. In a second step H_2O reacts with chemisorbed Hf precursor to remove the other two alkylamine ligands and generates a new hydroxylated surface and release two additional alkylamines (Figure 2.3 c-d). This mechanism would correspond to ligand-exchange mechanism previously described.
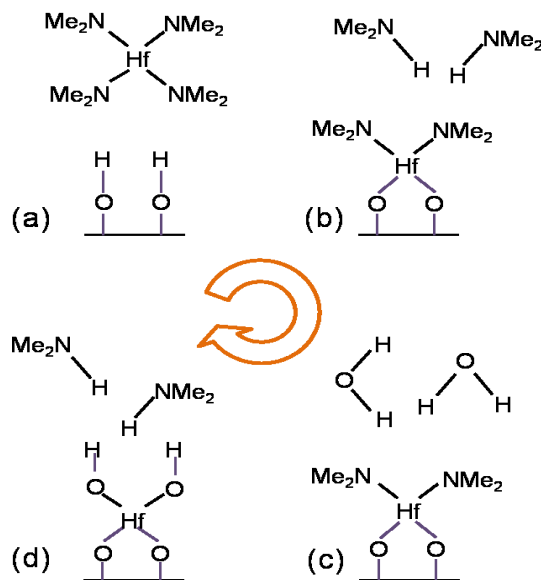
Figure 2.3: A possible reaction mechanism proposed for TDMAHf and water.

2.1.1.6   Deposition temperature

The deposition temperature plays a key role in monitoring the saturation mechanism of the ALD process and its effect on the growth conditions are illustrated at Figure 2.4. The ALD window determines the temperature range at which the self-limiting reactions are fulfilled and characterized by a growth rate of one monolayer per cycle[2]. Into the ALD window temperature range, the chamber heating allows a brief time reaction between the precursor and the surface. It also provides an assisted transport of sub-products and unreacted precursor molecules away from the chamber by increasing desorption of physically adsorbed precursors and sub-products.
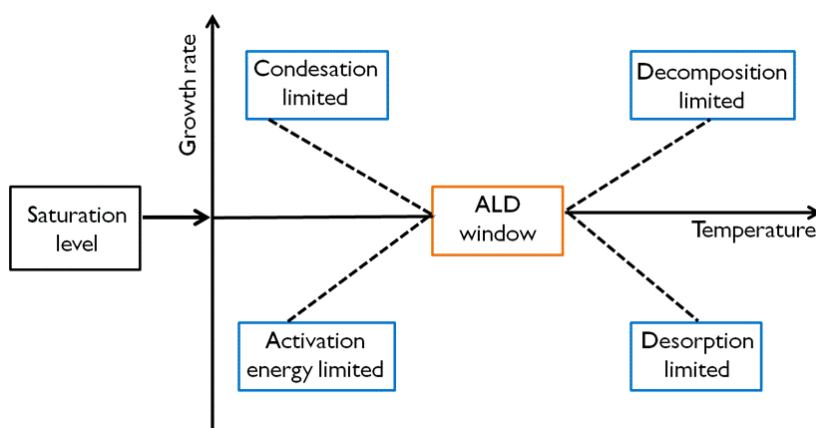
Figure 2.4: Overall effects of deposition temperature on the ALD process.

If the deposition temperature is too low the reaction between precursors and surface may not have enough thermal energy becoming less efficient (uncompleted reaction), decreasing the growth rate. It could also lead to the condensation of the precursors on the surface, not allowing their purge before the complementary precursor injection into the chamber. On the other hand, too high chamber temperatures could lead to both an undesirable contamination of the film by precursor decomposition and desorption of species needed for ALD from the surface.

2.1.1.7   Precursors

The precursors may be gases, liquids, or solids, but the vapour pressure has to be high enough for effective mass transport. In order to ensure that some liquids and all solids require to be heated. Precursors should gather some characteristics as volatile nature, thermal stability and must be chemisorbed on the surface or to show a particularly high reactivity with the surface groups[33]. The fast reactions would allow reaching the saturation stage in a short time, developing a reactive surface for the complementary precursor, high purity film and not originate reactive sub-products. Precursors should also not self-decompose, since it would affect the thin film thickness uniformity and film contamination. Different type of inorganic materials can be grown by ALD as oxides, nitrides, sulphides, selenides, tellurides, pure elements and other, though the oxides are the type most extensively investigated. The number of precursors and reactions existing in ALD is high. The non metal precursors used are: water, hydrogen peroxide and ozone for oxygen. Concerning metal precursors they can be classified into two main groups: metalorganic and inorganic[2]. The former can be further divided in those containing a direct metal-carbon bond (organometallic) and those precursors with no direct metal-carbon bond. The inorganic metal precursors usually used are those of metallic elements and halides, while respecting organometallic precursors, alkalis and cyclopentadienyls are the most common. In relation to other metalorganic precursors, alkylamides, alkoxides, amides, -diketonates and amidinates have been used.

2.1.1.8   ALD facility description

The deposition of HfO_2 thin films was carried out by means of Savannah 100&200 Atomic Layer Deposition System provided by Cambridge NanoTech Inc. The process is monitored and controlled by a PC via software. The equipment permits two modes of operation:

-Continuously flowing nitrogen carrier gas while pulsing (adding) precursor and pumping all along the process.

-Pulsing precursors with stop valve closed and pumping between pulses.

The growth of the HfO_2 thin films carried out by the method with continuous pumping of the reaction chamber.

The ALD system is constituted of the following components:

Reactor chamber: made of stainless steel is where the thin films deposition process takes place. It contains different pieces:

- A tubular (outer) and inner disk heaters that provide the heat to reach the required temperature for the deposition process.

- Two reactor temperature sensors (RTD´s) to monitor the chamber temperature.

- A Kalrez® O-ring and an aluminium lid hinged on the back.

Precursor assembly: metal face seal VCRTM fittings connects the different parts. Such parts are:

- Two ports precursors manifold.

- Two ports nitrogen manifold.

- Two high-speed ALD pulses valves.

- Heater block of valves.

- The precursor vessels and a heating jacket if the precursor required

Pumping line: all connections are made with Kwik Flange^{TM} clamps, and the pressure gauge is attached to it. A trap is coupled at the pumping line in order to protect the pump from reaction residues and/or unreacted precursor molecules that get confined.
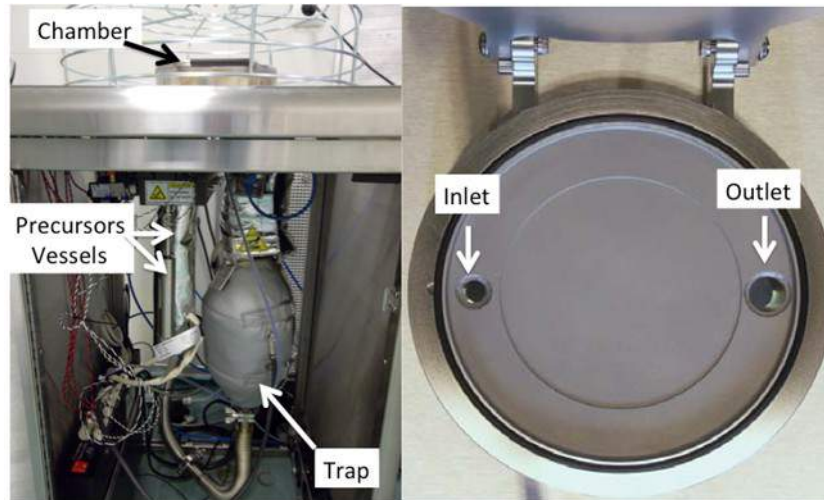
Figure 2.5: image of the ALD facility used for the HfO$_2$ thin films deposition process (left), and detail of the stainless steel reactor chamber (right).

Carrier gas: it is usually an inert gas (nitrogen, argon, etc…) and it is supplied through a provided mass flow.

Pump: provide the vacuum conditions required both for proper deposition and adequate purging of precursors from the chamber. A trap attached at the pumping line protects it from process residues that could erode the internal components of the pump.

Electrical connections: are located at an electronic control unit with 22 3-pin connectors for 115V AC, 16 2-pin connectors for RTD´s 5 2-pin connectors for 24V DC valves.

Heat guard: is a standard security feature to prevent burning form hot lid and reactor surfaces.

Regarding the control software, it allows the operator to control the ALD valves, pumping system, heaters and to set deposition recipes. The user-interface

consist of 3-tab pages: "Process", "Notes & Items" and "Advanced", a "Help" button, and temperature set point/reading clusters. The software also allows the creation and edition of recipes by a process sequence table. Selecting commands and setting in numerical values accomplish the edition of the table.

2.1.2   Optical photolithography

2.1.2.1   Introduction

Optical photolithography is a fabrication method whose development has been strongly related with the microelectronic industry, and at the present time the patterning of nearly all integrated circuits fabricated is carried out by this technique[34]. It could be defined as an optical method used to transfer a pattern from a mask to a light-sensitive chemical thin film onto a substrate carries out by a light source. The photolithography process consists of several steps described below.

2.1.2.2   Optical photolithography process

The optical photolithography process is composed of several procedures: adhesion promotion, resist coat, soft-bake, alignment, exposure, post-exposure bake and development.

Adhesion promotion: the photosensitive chemicals deposited on the substrates might not adhere properly, so such substrates are usually treated before the resist coating. The first step is the dehydration by heating the substrates between 100ºC and 200ºC at vacuum, followed by the deposition of an adhesion agent onto the substrate surface to prevent the further adhesion of water. The most common adhesion agent is the hexamethyldisilazane (HMDS).

Resist coat: in order to coat the substrate with resist, a small volume of the liquid resist is dispensed onto a substrate, which is spun about its axis at several thousand revolutions per minute. The centrifugal forces spread the resist and leave a uniform and thin film adhered to the surface. The attractive molecular forces that make the resist viscous play a role onto the rate of thinning. In this way, the larger is the viscosity of the resist the thicker is the resist film onto the substrate.

Softbake: the resist film does not fulfil the desired dissolutions properties in developer after coating, frequently due to an elevated porosity. The baking is the most common method of densifying the resist film as it removes the excess of solvent retained. Although several methods have been tried (convection, infrared and microwave ovens) hot plates have provided the best temperature control.

Alignment: this step is carried out in the cases the designed structure involves a sequence of patterning steps. At the alignment, the overlay of new patterns to patterns previously exposed on the substrate occurs. In order to facilitate it, marks are placed on the wafer at the first masking step, usually within scribe lines or in areas near the wafer edge.

Exposure: resist coated substrates are placed on the exposure chuck and aligned if necessary. Once the substrate is properly positioned a shutter in the illumination system is opened and the substrate is exposed to radiation that produces the pattern image on the resist. The pattern is formed on the wafer by a mask, which defines the resist areas to be exposed or to be protected from the radiation. The masks are sheets of glass partially covered by an opaque material (generally chromium) removed according to the required pattern. The photoresists are substances that undergo photochemical reactions when exposed to light. Depending of the type of resist the chemical properties of the exposed areas are different. In this way, for a positive resist irradiated regions become more soluble in the developer, and less soluble for the negative resist case. Regarding the light sources

the mainly used are Hg arc lamp, and KrF and ArF excimer lasers each of them with a range of wavelengths.

Post-exposure beak: after exposure, the photoactive compound varies in concentration proportionally to the light energy, which is not completely uniform and leads to standing waves. These standing waves degrade toughly lithographic performance. The most common method to reduce the effects of standing waves is the post-exposure baking, which induces the diffusion of such photoactive compound from regions of high density towards regions of low density. Currently, most resists are designed for treating with a post- exposure baking[34].

Development: during this step the resist pattern is defined on the wafer and it will serve as the physical mask to protect wafer areas from further chemical attack at subsequent processes (etching, lift-off, etc.). Chemical reactions occur at the development process by which the protected (unprotected) areas of the positive (negative) resist during the exposure get dissolved in the developer. Developing can be carried out by immersion, spray or puddle, and regardless the method used it has to be followed by rinsing and drying to ensure the developer has been removed and development step does not continue.
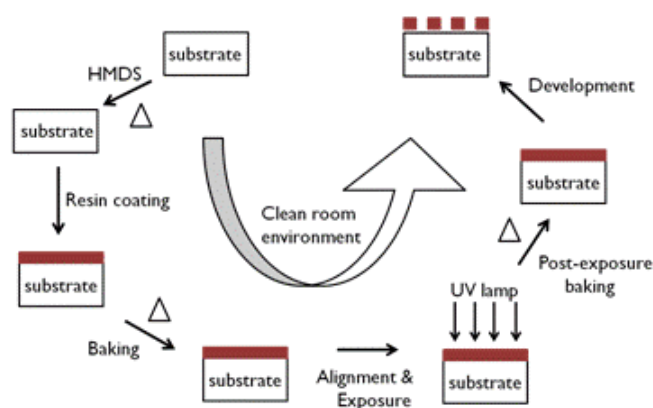
Figure 2.6: photolithography process scheme.

2.1.2.3   Optical photolithography facilities

All the optical photolithographic processes carried out during this thesis, were run in clean room atmosphere class 1000 at photolithography bay. The cleaning of the substrates, resist spin coating, baking and development processes took place at Ramgraber solvent wetbench made from polypropylene, provided with exhaust flow and designed as fumehood. Fabrication processes regarding detailed recipes will be described at device fabrication chapter. In our case no adhesion promotion of the surface substrate was required and the substrates were straight cleaned before the coating processand drying with nitrogen gun. The resist applied for all the photolithographic methods was AZ n Lof 2070 Photoresist provided by MicroChemicals Company. This is a thermally stable negative resist ultraviolet (UV) sensitive with high thermal and chemical stability. The softbake and post-exposure baking were done at the wetbench hot plates.
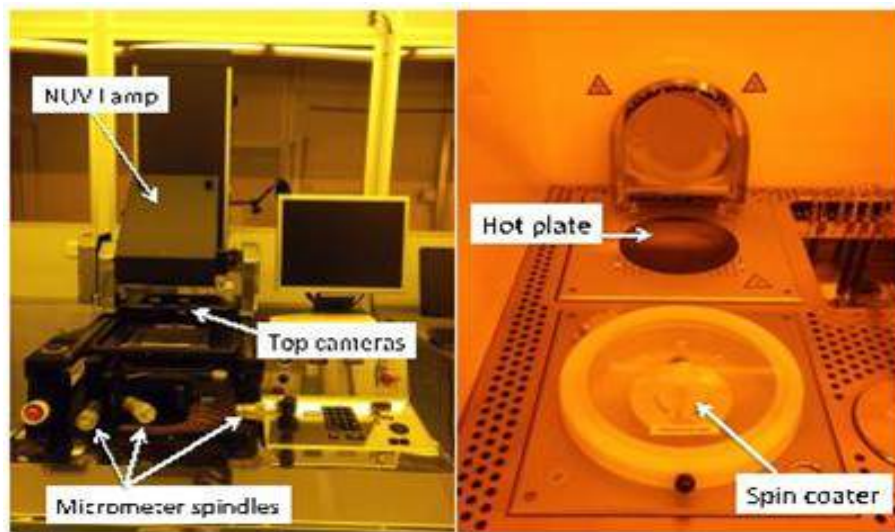
Figure 2.7: image of the mask aligner used during exposure processes (left). Hot plate and spin coater detail at solvent bench (right).

Regarding the exposure process, it was conducted by means of EVG620 Double Side Mask Aligner provided with a 350W Hg light source near ultraviolet

(NUV) range (280-450 nm). The alignment stage has precision micrometer spindles in X, Y and Theta as well as automatic wedge compensation system. The mask aligner is also equipped with top and bottom side microscopes with high-resolution cameras, and a digital zoom providing 2x and 4x image magnification for fine alignment. The system allows different exposure modes: hard, soft and vacuum contact and separation distance adjustable via software (0-300 m). The equipment operation process was PC controlled by software with self-explaining commands that also storages recipes for different processes. Finally, the development process took place at wetbench employing AZ 726MIF developer (tetramethyl-ammonium hydroxide solution) also provided by MicroChemicals Company.

2.1.3   Metallization techniques

2.1.3.1   Sputter deposition

This is a technique widely employed for depositing films materials where a target of the required material is bombarded by positive-ions. Sputtering gathers some advantages over other techniques: any material can be volatilized, volatilized compounds keep the stoichiometry and the film distribution rate can be uniform over very large areas. In the case of conducting materials, inert gas ions are generated by applying a dc voltage across the electrodes within the plasma vacuum chamber. For insulating materials ac or rf voltage is applied instead[35]. The parallel plate configuration (see figure 2.8) is the most common plasma configuration and potential distribution used between the anode (target material) and the cathode (substrate).

The ions are accelerated out of the plasma by the voltage drop between cathode and anode into the target, bombarding it with a constant energy and releasing atoms from the target. The plasma confinement near the target is assisted

by the magnetic field of the magnetron sputter source. The target atoms reach the substrate with enough energy to remain onto the substrate surface and form the film. To dissipate the heat produced by the bombardment the target must be bonded to a cooled copper backing plate. Inert gasses of extremely purity and clean target materials assisted the film purity. A new target or one exposed to air must be pre-sputtered to ensure the cleaning of the surface before deposition process.
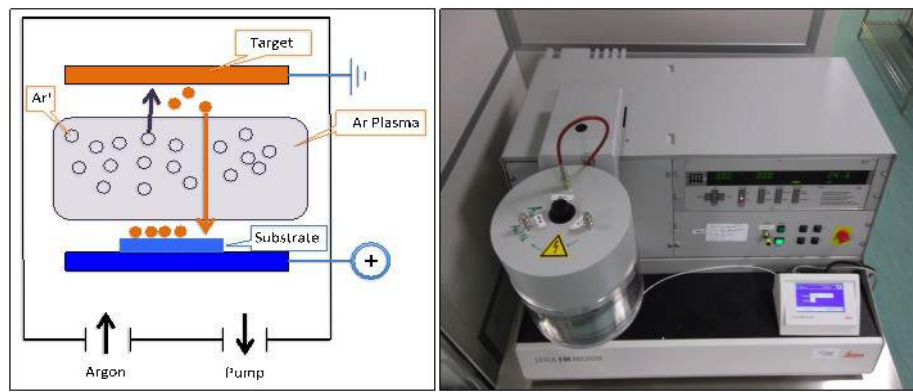
Figure 2.8: Schematic representation of a sputter deposition process (left) and image of the sputter system employed (right).

Leica EM MED020 sputter system sited at the clean room was employed during this thesis for the deposition of both titanium and Palladium by using argon plasma. The deposition rate was monitored via quartz crystal through a touch screen panel.

2.1.3.2   Electron beam deposition (EBD)

Electron beam deposition is a technique employed to evaporate a wide range of materials including refractory metals, alloys and low vapour pressure metals. The process takes place into a high vacuum chamber wherein an intense beam gun of high-energy electrons is employed to evaporate target materials. The electrons are

thermoionically emitted from a hot tungsten filament, and orientated and deflected by means of magnetic fields towards the target material. The tungsten filament is located outside the deposition area in order to not contaminate it. The electron beam reaches the target material and electrons convert its kinetic energy into thermal energy enabling the material evaporation. The heat generated during the process makes necessary a cooling system for the materials holders to prevent them from melting and alloying with melted source materials. The electron beam should be aimed at the center of the target material in order to avoid hitting the material´s holder[35]. The electron beam depositions performed during this thesis were done at UNIVEX 350 from Oerlikon Leybold Vacuum, placed at the clean room and equipped for thermal and electron beam evaporation and provided with a high vacuum pumping system. The system operation was controlled through a PLC and touch screen panel. Cobalt and gold were deposited by electron beam evaporation and thermal evaporation respectively.
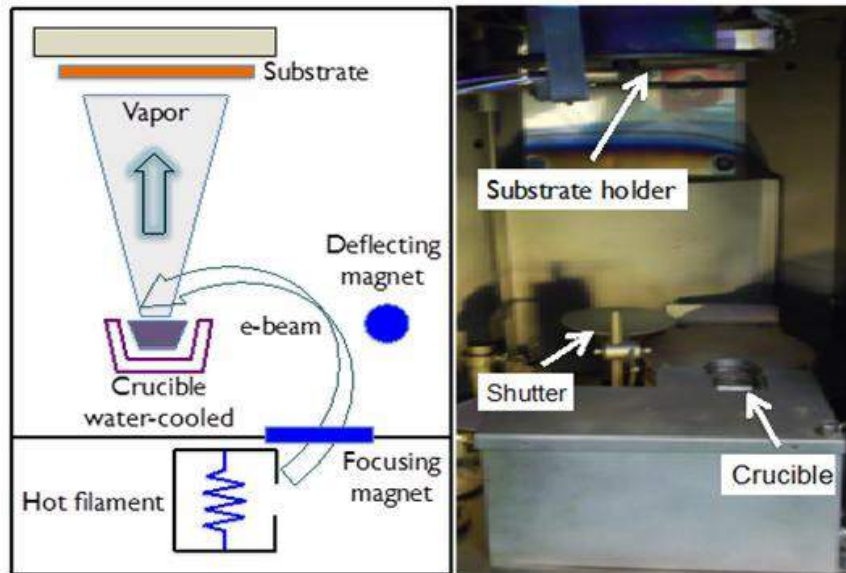
Figure 2.9: schematic representation of electron beam evaporation process (left) and image of the e-beam electron evaporation facility chamber (right).

2.2 Devices Fabrication

In this thesis two different types of samples were fabricated to be tested as non volatile memory based on the resistive switching effect: metal/insulating/semiconductor (MIS) and metal/insulating/metal (MIM). Within the MIM samples we also fabricated metal/insulating/metal devices with patterned bottom electrodes. The fabrication processes of all these samples are described in this chapter. The whole fabrication process took place in clean room atmosphere class 1000.

2.2.1 Metal/insulating/metal (MIM) devices

The fabrication of the metal/insulating/metal (MIM) devices was wholly carried out under clean room conditions except the cleaving of the wafers. The device fabrication was divided in several parts for MIM and MIM samples with patterned bottom electrodes as described below..

2.2.1.1 Substrates preparation

The devices were fabricated on p-type silicon substrates with 150 nm of thermally grown SiO_2 on top to avoid leakage currents through. The Si/SiO_2 wafer was cleaved into 10x10 mm^2 size substrates by a mechanical saw, and cleaned successive in acetone, isopropanol and deionized water with ultrasounds for five minutes at each solvent. Finally, the substrates were dried with a nitrogen gun.

2.2.1.2   Bottom electrode deposition

Several materials were tested as bottom electrodes (Ti, Co, Au, Pd and AuPd) by depositing 20 nm-thick films. In order to allow the deposition of several metals as Au, Co and Pd on SiO_2 substrates, 5 nm thin film of Ti was deposited previously to overcome adhesion problems. . All the materials were deposited by means of sputtering systems but gold, which was thermally evaporated at Oerlikon system.

The bottom electrode deposition in MIM samples with patterned bottom electrodes differed from that of the MIM samples in a photolithography process preceding the bottom electrode deposition (see figure 2.12). In this way, once the substrates were cleaned as described above, negative photoresist AZ n Loft 2070 was spin coated (applying 4000 r.p.m. for 60 seconds) before the first baking at 110°C for 1 minute. Next the sample was exposed at EVG620 Double Side Mask Aligner with 70 mJ. We patterned the different width bars used as bottom electrodes through an optical mask. The bottom electrode widths were within a range between 25 and 250 μm. A second baking (110°C for 1 minute) followed before dipping the samples into the developer for 1 minute. Once the bottom electrodes were patterned, Titanium (20 nm) was sputtered at Leica sputter system, to finish the process with the lift-off process.

2.2.1.3   HfO$_2$ thin film deposition

The HfO$_2$ thin film (20 nm thick) was grown by atomic layer deposition technique at Savannah 100&200 Atomic Layer Deposition System provided by Cambridge NanoTech Inc. Along the development of this thesis, the HfO$_2$ thin films were deposited as a function of two parameters: the deposition temperature and the purge time. The rest of deposition process parameters values were constant, namely, pulse times of oxygen and hafnium precursors (0.015s and 0.15s respectively) and

nitrogen flow (20 sccm). The ranges of values for deposition temperature and purge time were from 125°C to 350°C, and 1s to 35s respectively. The chamber pressure was about 0.5 Torr. The grown rate dependence as a function of the deposition temperature made necessary to determine it for the different growing conditions as described at the succeeding section 3.2.1.1.

In the case of the HfO_2 thin film growth for the MIM patterned electrode samples was conducted only at 300°C and applying 5 seconds of purge time.

2.2.1.4   Optical photolithography

After the HfO_2 deposition optical photolithography process was carried out as described previously at section 2.2.1.2 and in order to define the top electrode array on the HfO_2 by the use of an optical mask. The top contacts array pattern was composed of 80 squared top contacts (16x5) 200 μm size. In the case of MIM, patterned electrode samples the process differed in the range of top electrode sizes patterned (from 100 to 800 μm width stripes) that was carried out by an optical mask. The top electrodes where then aligned with the bottom electrodes for the required overlay. Such overlap gave rise to devices with different bottom electrode width/top electrode size ratio needed for an analysis of the current dependence on electrode area described at chapter 7.

2.2.1.5   Top electrode deposition and lift-off

In the same way than the bottom electrode, we tested different materials such as Palladium, Gold, Titanium and Cobalt as top electrode. The thickness of the top electrodes was 35 nm, except the Pd (75 nm). We covered the top electrodes with sputtered Pd until a total thickness of 75 nm to avoid any oxidation of some of the metals (Co, Cr, Ti), and facilitate the subsequent lift-off process. Sputter system

was used for depositing Pd, Cr and Ti, while thermal evaporation and electron beam evaporation were employed for the Au and Co deposition respectively.
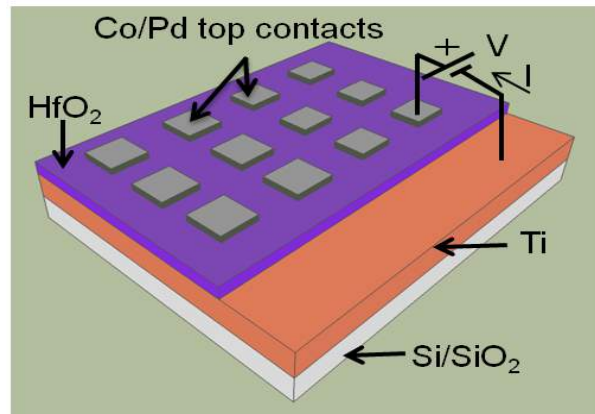
Figure 2.10: Schematic diagram and electrical configuration of a typical MIM sample with an array of top contacts.

In the case of the MIM patterned bottom electrodes samples the top metal electrodes were made only of Cobalt (35 nm) by electron beam evaporation, and subsequently stacked with sputtered Palladium for a total thickness of 75 nm. Finally, we dipped the samples in acetone to produce the lift-off for both type of MIM samples.
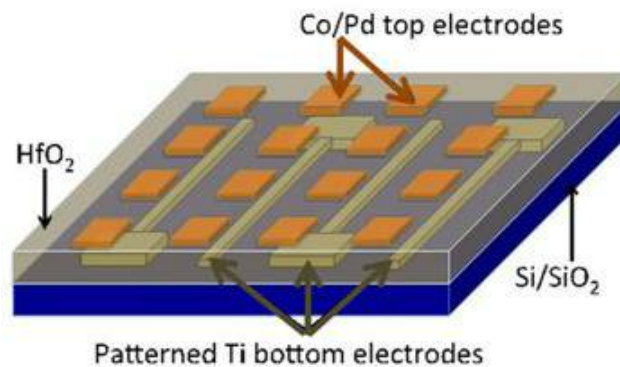
Figure 2.11: Schematic diagram of a patterned bottom electrodes sample with an array of devices.
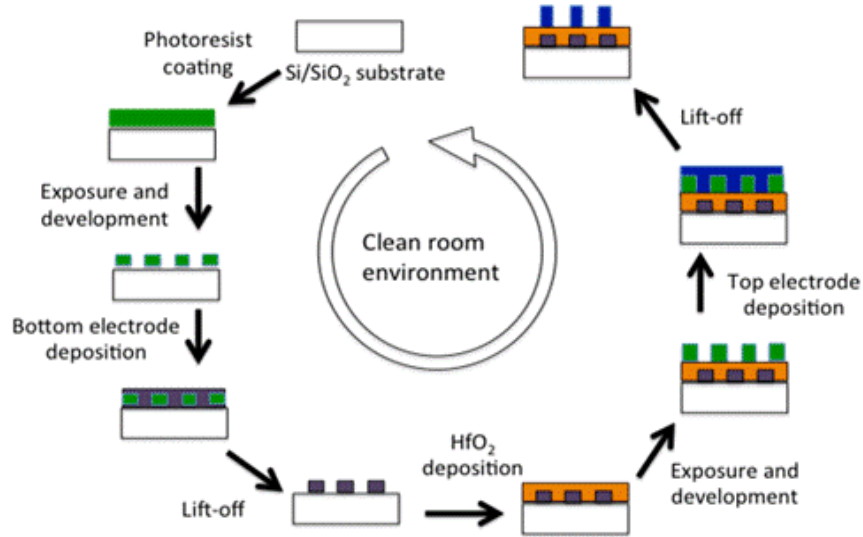
Figure 2.12: Fabrication process scheme of the MIM devices with patterned bottom electrodes. At samples with common bottom electrode, this was fabricated in a single deposition process.

2.2.2 Metal/Insulating/semiconductor (MIS) devices

The metal/insulating/semiconductor devices were fabricated from p-type SiO_2 (150 nm thermally grown)/Si wafer which was cleaved in samples of 10x10 mm^2. The p-type silicon wafer was highly doped with a resistance value of $\sim$ 4-40 mΩ cm. The fabrication process is showed at figure 2.13.

2.2.2.1 HF dipping

The first step was to remove the 150 nm SiO_2 layer from the top by dipping the samples in a 2%HF solution for 30 minutes in the acid bench (SiO_2 etching rate $\sim$ 5 nm/min). All the material employed during the HF dipping was made of Teflon. Once the etching process was completed the samples were placed into deionized

water to stop the etching and remove the HF from the sample. After dipping the samples in three different water beakers and check the pH was ~5.5, the samples were dried with a nitrogen gun.

2.2.2.2   HfO$_2$ ALD deposition

As soon as the samples were dried from the previous step, they were placed into the ALD chamber to proceed with the HfO$_2$ deposition and to avoid the grown of native SiO$_2$ on the surface. The 20-nm thick HfO$_2$ thin films were grown applying the recipes provided by the ALD facility company. In this way, the HfO$_2$ was grown at 175, 200 and 250ºC, with 25, 20 and 15 second of purge respectively. As mentioned at section 2.2.1.4 the rest of deposition process parameters values were constant, namely, pulse times of oxygen and hafnium precursors (0.015s and 0.15s respectively), nitrogen flow (20 sccm) and a chamber pressure of about 0.5 Torr.

2.2.2.3   Optical Photolithography

Square top contacts of 1x1 and 0.5x0.5 mm^2 were defined by photolithography techniques. Before the resist coating the samples were cleaned ultrasonically by successive solvents (acetone and isopropanol) for 5 minutes at each, and dried with nitrogen gun. After, the photolithographic process was run as described at section 2.2.1.2.

2.2.2.4   Top electrode deposition and lift-off

Aluminium and Cobalt were the metals deposited by sputtering as top electrodes before the samples were dipped in acetone to induce the lift-off. The estimated thickness checked by profilometer measurements was 100 nm.
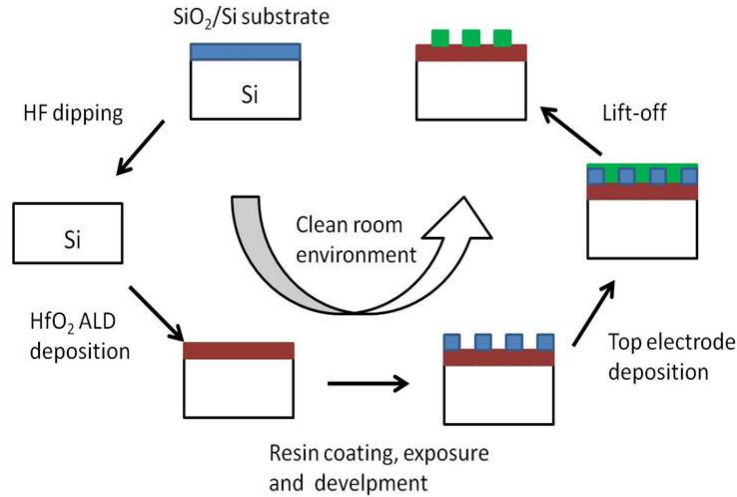
Figure 2.13: Fabrication process scheme of the metal/insulating/ semiconductor (MIS) devices.

2.3 Characterization techniques

2.3.1 Electrical characterization

2.3.1.1 Facilities description and set-up

The electrical characterization measurements performed during this thesis were carried out at EVERBEING probe station using a Keithley 2635A sourcemeter controlled by custom computer software run by LabVIEW (see Figure 2.14) and employed two-wire (high and low) local sense connection. The probe station is mainly composed of a sample holder, four tungsten tips attached to manipulators, which allow accuracy during the tip disposing on the top contacts, and an optical microscope also provided to support the tips arrangement.
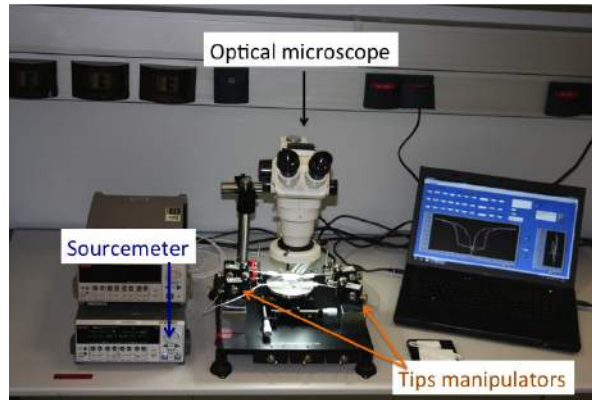
Figure 2.14: image of the probe station set-up used for electrical characterization.

Regarding the hardware, the Keithley sourcemeter uses triax type connectors while the probe station uses BNC type tips cables. This mismatch required the use of BNC-triax adaptors to connect the Keithley and the cables from the probe station. On the other hand, the communication between the hardware (sourcemeter) and software (PC) was through a general purpose interface bus (GPIB). The GPIB transmitted the commands introduced via the PC software to the sourcemeter, and returned the measurement data acquired to the PC.
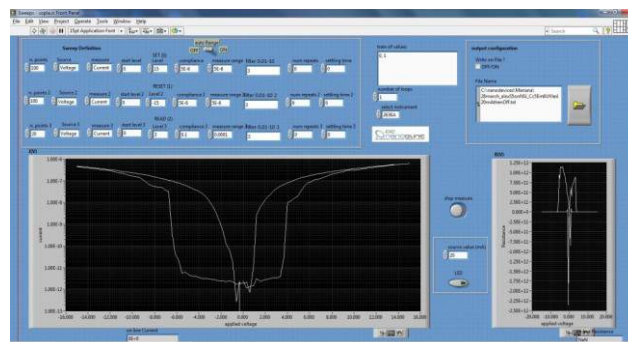
Figure 2.15: example of LabVIEW custom software used for I-V characterization measurement.

One feature of the sourcemeter is the *autorange* (automatic adjustment of the measurement range).This feature enables automatic current range selection while the I-V sweep is in progress. That means that the user has not to select a fixed current range, which can reduce measurement resolution. In our case the considerable and abrupt change in the current sensed during electrical characterization (> 3 orders of magnitude), made indispensable the application during the measurements of the *auto measure ranging* to minimize the error and maximizes the accuracy of the measured data. Otherwise, if *measure range* is applied, a measurement out of the selected *measure range* will have associated a significant error and lack of reliability and accuracy.
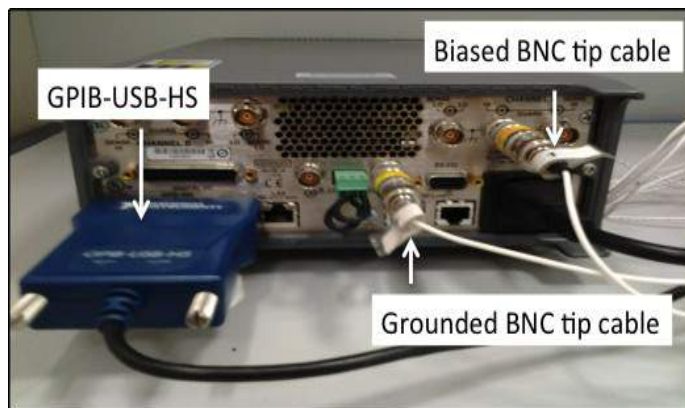
Figure 2.16: Backside of the Keithley sourcemeter where the GPIB and the two-wired set up can be observed.

Regarding the precision and accuracy of the measured data, another significant parameter to consider is the number of power lines cycle (NPLC), which indicates how long an input signal is integrated to obtain a single measurement.It affects the usable digits, the amount of reading noise and the ultimate reading rate of the instrument. A NPLC value of 1 PLC for 50 Hz means 20 ms (1/50). The fastest integration time (0.001 PLC) leads to the fastest reading rate, but at the expense of increased reading noise and lower precision. The slowest integration time (25 PLC)

gives the best noise rejection, but the slowest reading rate. In between settings are a compromise between speed and noise (1 PLC). In our case, in all the measurements showed in this thesis carried out by LabVIEW custom software a NPLC value of 3 was applied. Higher NPLC values did not reflect an improvement regarding accuracy and noise.

2.3.1.2   Current-voltage curve

The characteristic current-voltage (I-V) curves are conducted by applying a dc triangular voltage sweep through the sourcemeter and controlled by LabVIEW custom computer software. The dc voltage sweep was as follows: 0V→15V→0V→-15V→0V, with 0.3V step size, applying *autorange* and NPLC=3. Top and bottom electrode were biased and grounded respectively. Figure 2.17 shows a schematic representation of the dc triangular voltage sweep and an experimental I-V curve.
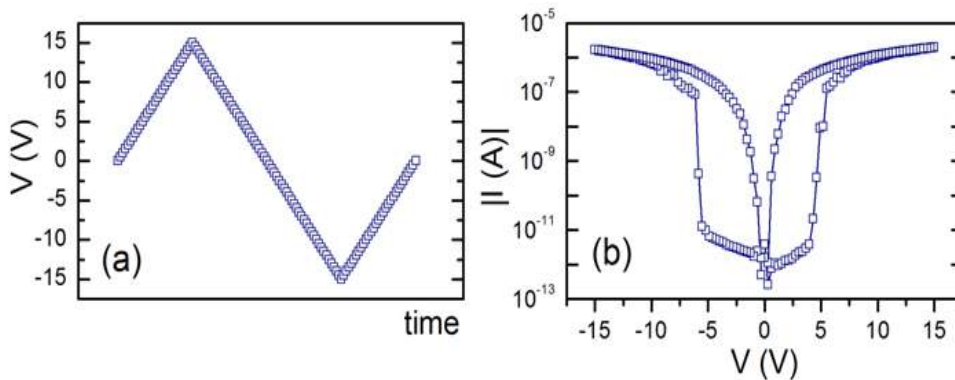
Figure 2.17: (a) Schematic representation of the dc triangular voltage sweep. (b) I-V curve obtained from Ti/HfO$_2$/Co sample with HfO$_2$ grown at 300°C and 5 s purge time after applying the dc triangular voltage sweep.

The performance of the I-V curves allowed us to discern the existence of stable hysteretic transitions between two different and stable resistive states, driven by the application of an electric field (figure 2.17b). The analysis and interpretation of

the I-V curves obtained for different HfO_2-based MIM devices is described in detail at chapter 5.

2.3.1.3   Voltage pulse application

The voltage pulses characterization carried out by a train of voltage pulses, through which we induce the logical computing processes: writing, reading and erasing (see top of Figure 2.18). A delay time can be applied after reaching the voltage pulse value and before the current measurement. The writing voltage pulse 20 ms width induces a change into resistance state of the device (from high to low resistance state) while the erasing voltage pulse value got an amplitude of opposite bias large enough to return the device at its original high resistance state.
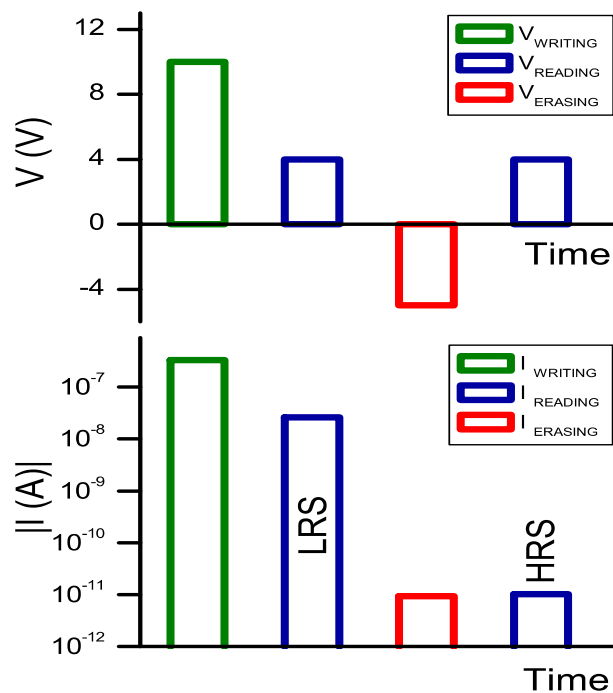
Figure 2.18: Schematic representation of potential pulses train employed to induce logical computing processes (top) and the associated currents (down).

Regarding the reading voltage pulses, which are applied to sense the resistance state, its value is below the required to cause any change onto the current resistance state. The fulfilment of the writing and erasing on the change of the resistance state of the system was tested by the currents associated to the subsequent reading voltage pulses applied. Thus, the currents sensed after the writing and erasing pulses belonged to the LRS and HRS states confirming the resistance switching as exhibited in figure 2.18. The voltage pulses train have the next sequence: writing, reading, erasing and reading. In order to verify the non-volatile nature of the resistance states, zero volts pulses are applied in between each logical potential pulse.

2.3.1.4   Hysteresis switching loops

HSL is a parametric plot that displays the evolution of the resistance of a device during the application of a train of electrical pulses (figure 2.19) [36-38].
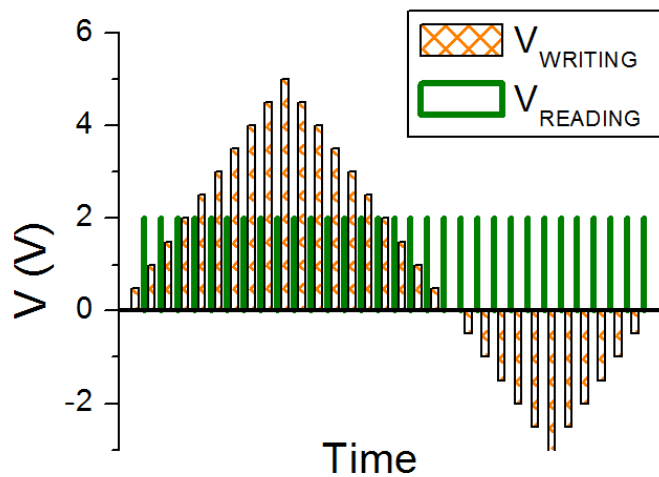
Figure 2.19: schematic representation of the voltage writing pulses values during the potential loop together with the reading remnant resistance voltage pulses in between.
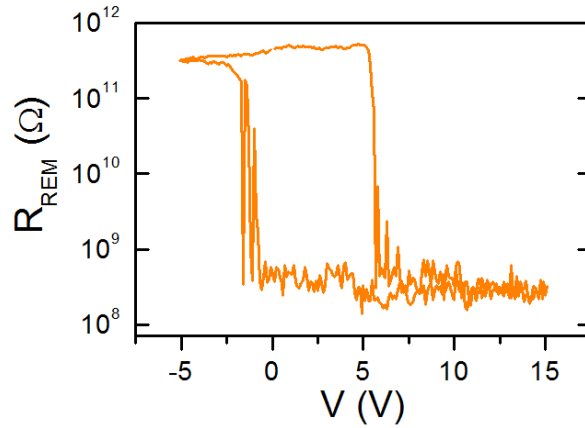
Figure 2.20: Experimental HSL obtained from Ti/HfO$_2$/Co (HfO$_2$ grown at 300ºC and 5 s purge time) for a V$_{READING}$ = +4V. The data displayed correspond to the remnant resistance value measured by V$_{READING}$.

HSL plots are defined as the sequence of points [V$_{PULSE}$(i), R$_{REM}$(i,V$_{READ}$)], being i the pulse index, V$_{PULSE}$ the voltage of the i-th pulse and R$_{REM}$ is the remnant resistance after the i-th pulse, sensed with the reading voltage V$_{READ}$ (figure 2.20). The V$_{READ}$ value is lower than the corresponding V$_{SET}$ value to not induce any resistance change into the device.

2.3.1.5   Stability and retention measurements

The stability measurements were also conducted by the application of voltage pulses. The system is set at either HRS or LRS, and a subsequent significant number of reading steps (several hundred) are run to detect any degradation of the resistance state.

The retention test is a similar performance whereby a constant voltage is applied and the current is measured uninterruptedly for a time (some hundred seconds) after setting the system at either LRS or HRS. This retention test was realized for both resistance states. The monitored current would indicate whether the resistance undergoes degradation or it is stable.

2.3.1.6   Minor loops

A minor loop consisted of the application of a voltage sweep as follows: 0V→15V→A→15V→ 0V, where A is a variable voltage value. This electrical measuring protocol was used to determine the effect of applying voltage values of opposite bias on the resistance state of the device. Minor loops can be used to clarify the resistive switching nature, i.e. if it is unipolar or bipolar. In this work, the A voltage values were applied in this order: 0, -1, -2 and -3V. The measurements begin with the device in an initial HRS, which is switched to the LRS as showed by path 1 in Figure 2.21.
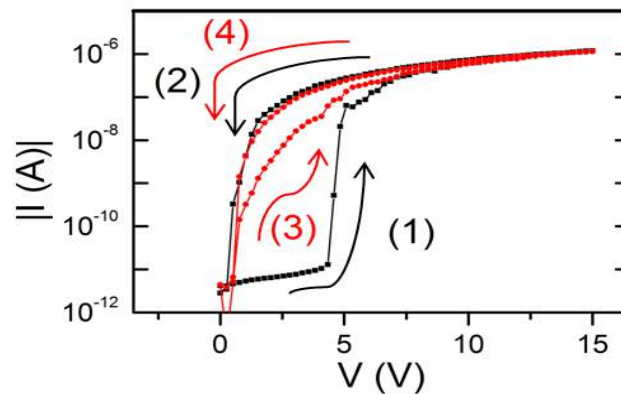
Figure 2.21: experimental minor loop where the system was set to the LRS from the HRS (path 1) and after the device was swept to 0V (path 2), an increasing of the resistance state was found reflected by the path 3.

When the voltage is then swept back to the first A value, zero volts (path 2), it results in an increase of the resistance state of the device as showed by the subsequent path 3. As the A voltage value was swept to more negative values the resistance state during the initial stages of path 3 became more robust. As the voltage was swept to -3V, the initial HRS was recovered back. The results were very similar for both voltage polarities and are described at the section 4.2.1.

2.3.2 Atomic force microscopy (AFM)

Atomic force microscopy (AFM) is a high-resolution type of scanning probe microscopy technique where a physical probe scans the sample surface to form images with sub-nanometers resolution [Figure 2.22(a) shows a picture of the AFM facility used]. This technique emerged as one application of the scanning tunnelling microscope capability of measuring forces as small as 10^{-18} N[39]. Such degree of sensitivity allows the access to the regime of interatomic forces. AFM is basically composed of a cantilever with a sharp tip at its end, whose radius is on the order of nanometers, attached to a piezoelectric crystal, a laser beam, a sensitive photodiode and a feedback circuit. Atomic force microscopy operation is based on sensing interatomic forces between the probe tip and the surface as a function of the position during the sample scan [illustrated scheme can be found at Figure 2.22(b)].

Variations in sample topography produce interatomic forces changes between probe and sample causing cantilever deflection up or down, measured by the spot laser reflection position onto the photodiode. Such deflection is due to the piezoelectric crystal expansion or contraction in response to the voltage provided by the feedback circuit, which is reflected into a height measurement providing topographic information of the sample surface. There are different types of AFM operation depending on whether the tip is in contact or not with the surface during the scanning, namely contact and dynamic or "tapping" mode respectively. In the former, the tip is in contact with the sample surface and it is deflected as it slides over the surface. The feedback circuit maintain constant the force between tip and surface, calculated by Hook´s law $F = -k \, z$, where k is the stiffness of the tip and z the distance the cantilever is bowed. The sample surface may be damaged during the scan by frictional forces. In the latter, the tip oscillates near its resonant frequency by means of the piezoelectric crystal and the sample topography fluctuations induce changes on the amplitude that is maintained constant by feedback circuit adjusting the

tip-sample separation the during the scan process. Thus, amplitude oscillations are used to identify and measure the surface features.
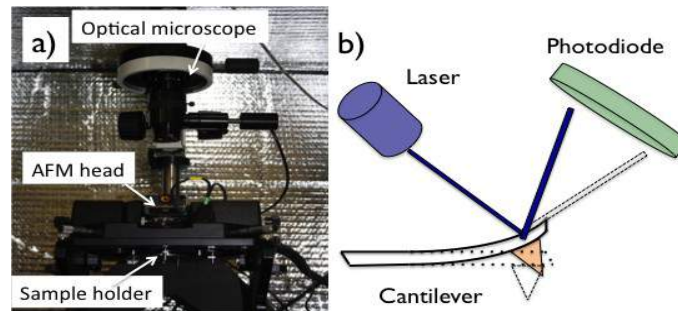

Figure 2.22: (a) Picture of the AFM facility used for surface physical characterization. (b) Schematic representation of optical detection method employed to determine the cantilever displacement.

The characterization of the thin films roughness was carried out by means of an Agilent AFM and tapping mode aluminium coated scanning probes. The maximum scanned area permitted was 100x100 μm^2 and 10 x10 μm^2 in the case of regular and high-resolution piezoelectric scanner respectively. Other significant parameters during the running of a topographic scan were the speed (line s^{-1}) and the level of resolution (point line^{-1}) whose values will be specified in further chapters. In order to diminish environmental disturbance that could affect the measurement reliability the AFM was isolated by a cage. Regarding the analysis of AFM topographic measurements it was conducted with the software Gwyddion 2.24, which allows different treatment of the data as mean plane subtraction, lines correction by matching height median or removing polynomial background. The software also enables topographic images in 2D and 3D (see example at Figure 2.23), topographic profiles at any direction and the determination of several statistical parameters for the roughness characterization as the average height value, the minimum and maximum height values, the median and the root-mean-square (rms), which indicates the even degree of a surface.
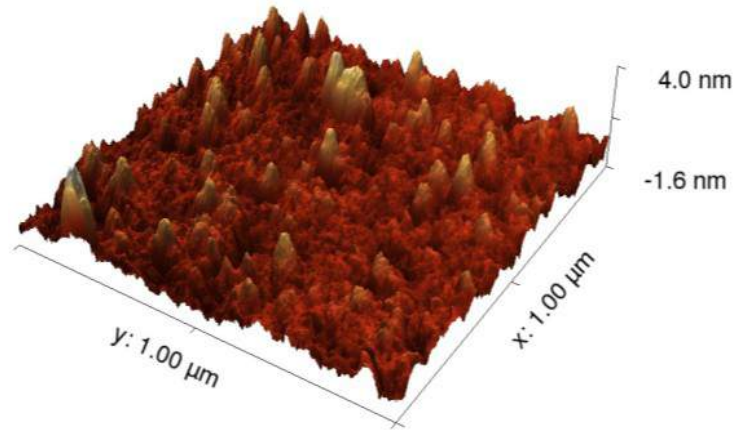
Figure 2.23: 3D AFM image obtained from HfO_2 thin film grown at 200ºC

2.3.3 X-ray diffraction (XRD)

This technique based on the Bragg´s law allows us to determine the degree of crystallinity and the crystal phase of a material. The X-ray diffraction is originated by the similarity in length of the interatomic distances of atomic layers and X-ray wavelength. Diffraction occurs when Brag´s law is satisfied during the incident angle sweep for constructive interference, i.e., when the difference in path length between two parallel X-ray beams is an integer number of X-ray beam wavelength[40]:

$$n\lambda = 2d_{hkl}sin\theta \qquad (6)$$

where n is an integer number, λ is the wavelength of incident wave, d is the spacing between the planes in the atomic lattice, and θ is the angle between the incident ray and the scattering planes.
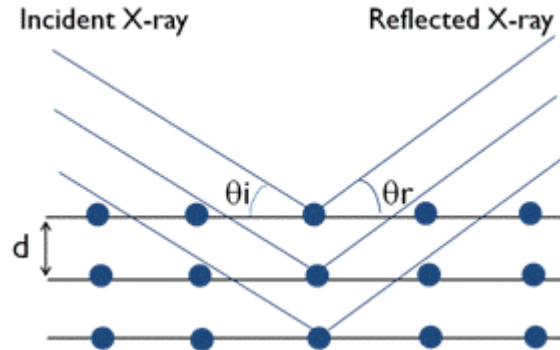
Figure 2.24: Illustration describing the interaction of X-ray with a periodic crystal lattice.

When an X-ray beam hits an atom the electrons around oscillates at the same frequency than the incident X-ray beam, giving rise to interferences. Such interferences are destructive as the combining waves are out of phase except when the atoms are arranged in a regular pattern. In that case the interferences are constructive (in phase) in some directions and a defined X-ray beam leaves the sample at various directions. Thus, a diffracted beam can be described as a large number of scattered rays strengthening each other. The peaks corresponding to different crystallographic orientations are related with a specific 2θ value of the reflected beam. A highly crystalline material produces and X-ray diffraction spectra with very sharp peaks while an amorphous material gives a broad hump instead sharp peaks.

Further structural information as average grain size of polycrystalline materials can be obtained from Scherrer equation through the peak width at half maximum. Also information on lattice strain is given by the peak position, which shifts to lower angles (2θ) in the case of uniform strain or broadens for a non-uniform strain:

$$\Delta\theta_{FWHM} = {k\,\lambda}/{1 - cos\theta_i} \qquad (7$$

Where λ is the X-Ray wavelength and in our case λ = 1.5405 Amstrongs (Cu K), k is the shape factor and its values is k=0.4 if b=b$_{1/2}$, , i.e. the line width at half maximum. The most intense line of the spectra was used, and b was previously converted in radians.

Due to the large depth penetration of X-ray into the matter, X-ray diffraction produces a low sensitivity for thin films analysis due to the small diffracting volumes, which results in low diffracted intensities compared to the substrate and background. Gracing incidence X-ray diffraction overcomes this restriction by applying very low stationary incident angles (typically 0.3 ° to 3°), which increases the path length of the X-ray beam into the thin film (figure 2.25).
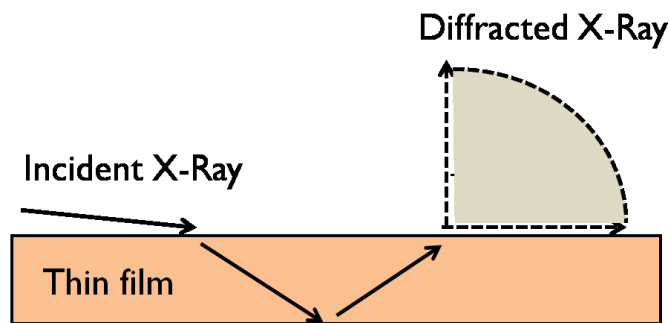
Figure 2.25: schematic representation of the interaction of X-ray with a refractive thin film for grain incidence X-ray refraction technique.

As the length path into thin film is enlarged, the diffracting volume increases and the refracted intensity is enlarged, meanwhile the intensity from the substrate is reduced leading to an increase in the thin film-background signal ratio. During the collection of the diffraction spectra only detector sweeps the angular range while incident angle is maintained constant resulting in an also constant beam path length into the thin film and a constant diffracted volume.

Figure 2.26 shows a GIXRD spectra obtained from a 20 nm HfO$_2$ thin film where different peaks belonged to a polycrystalline phase can be noticed.
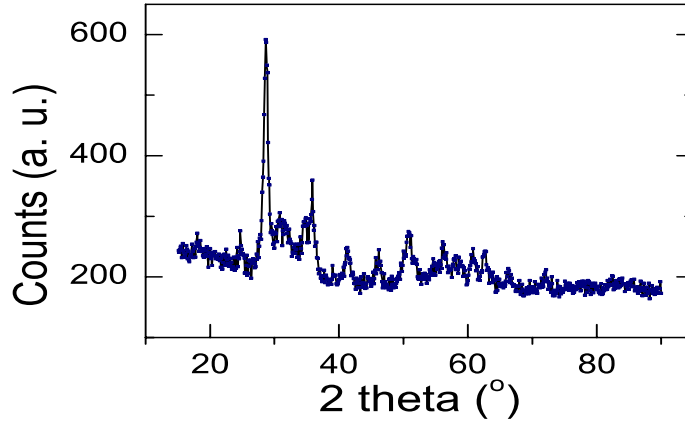
Figure 2.26: GIXRD spectra from a 20 nm HfO$_2$ thin film grown at 300ºC.

In relation to the determination of the thin film thickness, we used X-Ray reflectivity (XRR) which is a technique related to X-ray diffraction (XRD)[41]. This technique is based on interference of X-ray reflected from two interfaces (vacuum-film, film-substrate or film-film for multilayer thin film structures) and it is defined as the ratio of the intensity of the incident radiation to the intensity of the reflected radiation. Reflections for angles above the critical angle (below this angle X-ray undergo total external reflection) will have contributions from both the air-thin film interface and thin film-substrate interface. The rays reflected from thin film-substrate interface travel an additional distance (Δl) given by:

$$\Delta l = 2t sin(\theta_{r1}) \approx 2t(\theta_{r1}) \qquad (8)$$

where θ_{r1} is the angle of the reflected ray from air-film interface and t is the film thickness.
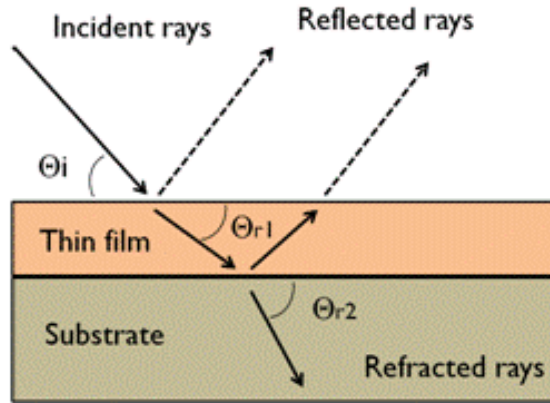
Figure 2.27: schematic representation of the interaction of X-ray with a refractive thin film.

The interference resulted from rays reflected from each interface will affect the intensity of the reflected rays and produce interference fringes whose maxima or minima occur at the following incident angles:

$$\theta_i \approx \sqrt{\theta_c^2 - \frac{(n+\Delta n)^2 \lambda^2}{4t^2}} \qquad (9)$$

where n is an integer number, the value of Δn is ½ for maxima and zero for minima, t is the film thickness, λ is the X-ray wavelength and θ_c is the critical angle for the air-film interface. The film thickness can be approximated from the distance between maxima o minima fringes:

$$t = \frac{\lambda}{2\Delta\theta} \qquad (10)$$

where $\Delta\theta$ is the difference in radians between maxima or minima fringes.

The X-ray measurements carried out at X´PERT PRO X-Ray Diffration system provided by PANalytical B. V. The anode material of the X-Ray source was a cupper filament with a wavelength K_1 of 1.5405 Amstrong.
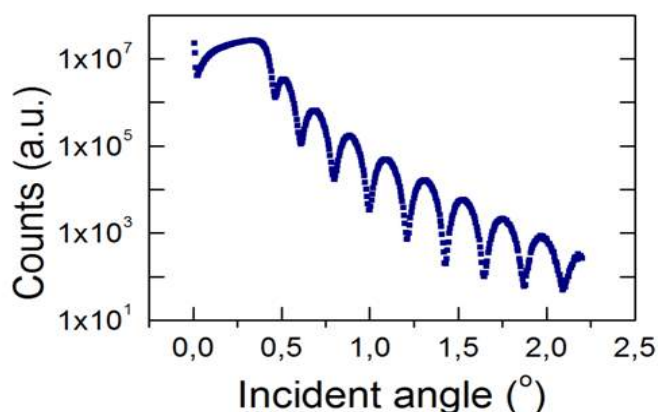
Figure 2.28: X-ray reflectivity spectra from a 20 nm HfO_2-thick film.

The measurements data were examined and treat by the software supplied by the equipment. Reflectivity and grain incidence diffraction spectra were analysed by X´Pert Reflectivity and X´Pert HighScore Plus respectively. Specific details on the measurements and results will be specified in chapter 3.

2.3.4   X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy is a surface analysis technique that provides elemental composition and chemical information from the top ~10 nm of a solid surface, though by the use of an ion gun is also capable of carrying out deep profiling to sputter away the surface during analysis.

This technique is based on the photoelectric effect that describes the interaction in between X-ray of known energy and an atom. When a highly energetic X-ray photon hits and transfers its energy to a core-level electron, it is emitted to the vacuum level with a kinetic energy dependent of the incident X-ray and the binding energy of the atomic level from which it originated. The initial state of the photoelectron can be either a core-level state or a valence band. In this respect, soft X-rays (300-1000 eV) are suitable to probe the core levels of a solid, which generally

show no dispersion. The photoemission process obeys the following energy conservation rule:

$$hv = Es + \phi + Ekin \qquad (11)$$

where hv is the photon energy, E_s is the electron binding energy respect to the vacuum level prior to ionization, ϕ is the sample work function and E_{kin} is the kinetic energy of the photoelectron.

The binding energies (BEs) provide information on the chemical composition, and distinct BE shift results from the chemical environment in which the core electron is found before the photoemission process (type of bonding, oxidation sate, etc.). In this way the analysis of the energy and intensity of the emitted photoelectrons as well as the BE shift, allows to identify and determine the concentration of the elements and the chemical environment of the sample.
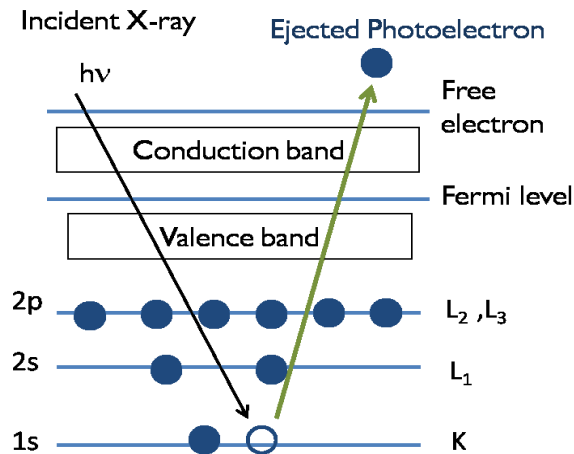
Figure 2.29: XPS process. Incoming x-ray beam excites the atoms and as result emits a photoelectron.

XPS experiments were performed using a Phoibos photoelectron spectrometer equipped with an Al K X-ray source (16 mA, 12.5 kV) as the incident photon radiation. The overall resolution was approximately 0.9 eV. The pressure in

the analyzing chamber was <1.0×10^{-9} mBar during measurements. Tantalum foil was used to create an electrical contact between the sample surface and the sample holder to avoid charging effects. Calibration of the binding energy scale was performed by fixing the adventitious C 1s peak to a value of 284.8 eV. CasaXPS sofware (version 2.3.15) was used to analyze the sample spectra[42]. A Shirley type baseline was employed and Gaussian (70%) - Lorentzian (30%) [GL (30)] profiles were used to fit the individual components. The background has been subtracted in the spectra detailed in the figures. Depth profiles of the deposited films were acquired by taking XPS measurements after each argon ion beam etching cycle (1 keV for 10 minutes)[43]. These conditions resulted in the removal of 3-4 nm of material during each cycle, a sputter rate of 0.3-0.4 nm/min.

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CHAPTER 3

Morphological characterization

In this chapter we describe the results from the HfO_2 thins films characterization carried out by ,Atomic Force Microscopy (AFM) and X-Ray techniques. We analyzed by AFM the effect on the HfO_2 films surface morphology of the deposition temperature and purge time applied during the HfO_2 growth process. On the other hand, reflectivity X-ray (XRR) and grazing incidence X-ray diffraction (GIXRD) techniques were employed to determine the HfO_2 thin films thicknesses, HfO_2 thin film structure and crystallinity degree.

3.1 Atomic force microscopy (AFM) measurements

Atomic force microscopy (AFM) was used for the determination of the surface roughness both of several substrates and different thin films. All the measurements were performed by tapping mode with a resolution of 512 points per line and a speed of 0.5 lines per second. In order to obtain a reliable roughness value, we carried out AFM measurements on each sample at least twice at different areas. The scan size was usually 20x20 μm^2 for surface analysis, but 1x1μm^2 scans were also performed for detailed surface images. The AFM data were treated with the software Gwyddion 2.24 that provided visualization and processing functions, and processed via levelling (facet levelling, polynomial background removal) and statistical functions (root mean square).Scan speed effect on the accuracy of the surface roughness determination was tested by scanning a sample area 20x20 μm^2 scan size at different scan speeds. It was observed that scan speeds up to 0.5 lines per second led to accuracy lose as shown at Figure 3.1.
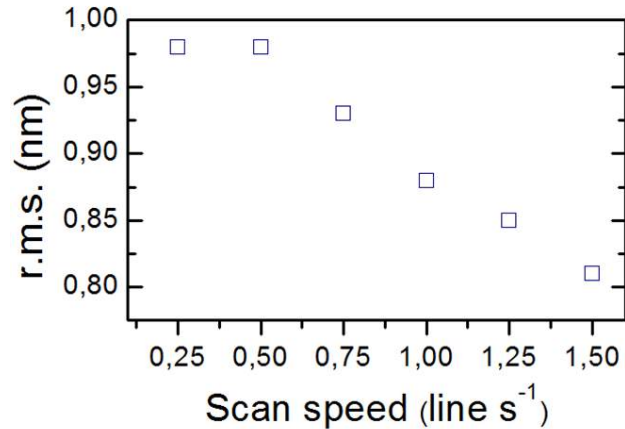
Figure 3.1: scan speed effect on the accuracy measurement. Scan speed higher than 0.5 lines per second leads to accuracy lose.

As the scan rate becomes faster, the magnitude of the rms amplitude increases as the feedback loop is more and more unable to correct the encountered topographic changes. This leads to an incorrect and higher value of the surface roughness measured by the AFM tip.

3.1.1 Substrate choice

Surface roughness analysis of different substrates was conducted in order to select the device substrate. We measured the surface roughness of three different substrates: borosilicate glass, namely *Pyrex*, glass and silicon (150 nm thermal SiO_2 on top). The AFM images were analyzed and processed with the software Gwyddion 2.24. The rms data averages are showed in the figure 3.2 together with the standard deviation obtained from the calculated average from three measurements.
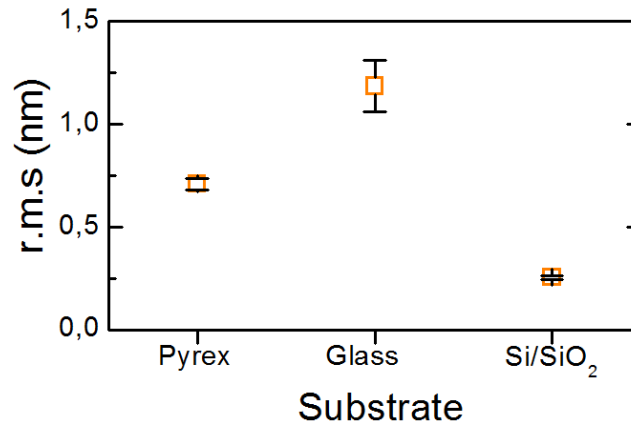
Figure 3.2: rms roughness obtained for different bared substrates (squares).

The results clearly indicated that the SiSiO$_2$ substrate provided the smoothest surface. In consequence it was selected as substrate for the metal/insulating/metal samples. The AFM results showed hereafter correspond to thin films deposited on SiSiO$_2$ substrate.

3.1.2 Surface morphology for different metal bottom electrodes

In order to study different candidates to act as bottom metal electrode at the metal/insulating/metal (MIM) devices, diverse metals were deposited on the bare SiSiO$_2$ substrate to characterize the surface morphology by AFM. Thin films 20 nm thick of different metals (Ag, AuPd, Co, Pd and Ti) were sputtered while Au was thermally evaporated on Si/SiO$_2$ substrates. In the case of metals as Pd, Au and Co adhesion problems on the substrate were solved by depositing 5 nm of Ti as adhesion layer onto the substrate. The AFM surface analysis results are showed in table 3.1.

Metal	r.m.s. roughness (nm)
Co	0.44±0.01
Au	0.49±0.04
Ti	0.65±0.04
Pd	0.74±0.01
AuPd	1.83±0.04
Ag	4.43±0.03

Table 3.1: rms roughness values obtained for several metal 20 nm thick thin films on SiSiO$_2$ substrates. In the case of Co, Au and Pd a 5 nm thick layer is beneath the metal layer to improve the adhesion on the substrate.
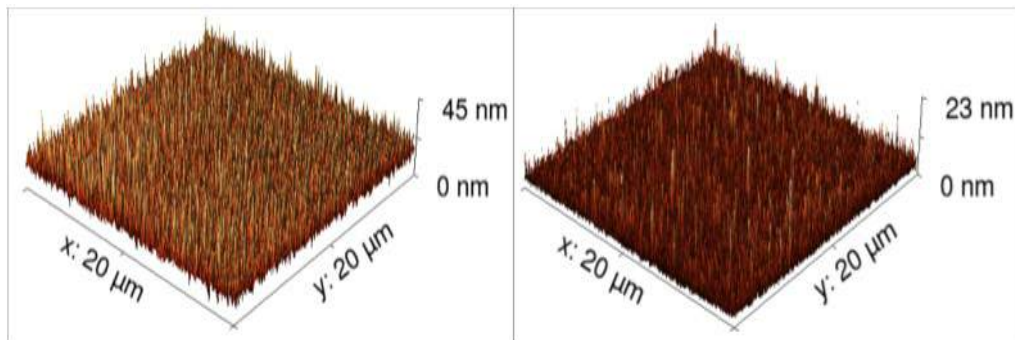
Figure 3.3: 3D topographic profile obtained for Ag (left) and AuPd (right) 20 nm thick thin films on SiSiO$_2$ substrates.

The roughness values obtained for the different metals deposited were dissimilar. Metals as Au, Co, Pd (those including the 5nm thick film Ti adhesion layer) and Ti presented smooth surfaces while metals as AuPd and Ag displayed uneven surfaces with a significant roughness as showed at figure 3.3. The necessity of obtaining smooth bottom electrodes is not trivial, as it would ensure a further smooth HfO$_2$ film without the potential formation of pinholes. Thus, only the metals

displaying smooth surfaces were considered as candidates to be the bottom electrode of the MIM device. In this way, AuPd and Ag were ruled out as metal bottom electrodes. However metals as Co and Au showed again adhesion problems during HfO_2 deposition process at high temperatures (300°C for 45 minutes). In order to improve the metal adhesion, a thicker Ti thin film (10 nm) was sputtered as adhesion layer for Co and Au. However, during the further electrical characterization of these Co and Au bottom electrode devices, characteristics drawbacks related with the potential presence of pinholes were detected. The surface roughness of Ti (10nm)/Co (20 nm) and Ti (10 nm)/Au (20 nm) samples were characterized by AFM after sputtering, and also after undergoing 300°C for 45 minutes. The AFM results (see table 3.2) showed a substantial increasing of the roughness after the thermal treatment. This roughness increment could lead to the formation of undesired pinholes through the HfO_2 thin film during the deposition process.

Metal	rms roughness (nm)
Ti/Co	0.44 ± 0.01
Ti/Co 300°C-45 min	3.6 ± 0.13
Ti/Au	0.71 ± 0.03
Ti/Au 300°C-45 min	0.89 ± 0.04

Table 3.2: rms roughness values for Ti/Co and Ti/Au after sputtering and thermal treatment (300°C for 45 minutes).

Eventually the metals selected to form the bottom electrode after AFM results and adhesion drawbacks were Titanium and Palladium, which displayed a smooth surface and good adhesion properties on $SiSiO_2$ substrates independently of the HfO_2 deposition temperature.

3.1.3 Deposition temperature and purge time effect on surface morphology

A set of 20 nm thick HfO_2 thin films were grown at different deposition temperature by ALD to study the effect of the deposition temperature on the HfO_2 thin films roughness. The deposition temperature varied from 125°C to 350°C, while the rest of the fabrication process parameters were constant (values reflected at table 3.3).

Oxygen precursor pulse	0.015 s
Hafnium Precursor pulse	0.15 s
Purge time after water pulse	5 s
Purge time after Hafnium precursor pulse	5 s

Table 3.3: parameters values applied at HfO_2 deposition process for the study of the deposition temperature effect on the surface roughness.

The hafnium precursor pulse was 10 times longer than that of water (oxygen precursor) increasing then the hafnium dose available at the chamber to ensure that all the active hydroxyl groups (-OH) originated on the surface during the water pulse saturate. The self-limited ALD process makes that the excess of non reacted precursor is removed from the chamber during the subsequent purge step. The 20 nm thick HfO_2 films were deposited both on bare $SiSiO_2$ and $SiSiO_2$/Ti (20nm) substrates to determine whether the Ti layer had any unwanted effect on the HfO_2 film roughness. The AFM analysis of the HfO_2 thin films on $SiSiO_2$ (figure 3.4) and on $SiSiO_2$/Ti (figure 3.5) indicated an increasing of the surface roughness along with the deposition temperature. The rms roughness at low deposition temperatures was about 2% of the film thickness while at high temperatures this value reached a value of 7%. The AFM results also showed similar trends of the roughness at both samples suggesting that Ti layer did not have any significant effect on the HfO_2 roughness,

apart from the obvious roughness increase due to the own Ti underlayer. Figure 3.6 shows a 3D AFM profile of HfO_2 films grown at 150°C and 300°C with a significant surface roughness increment at the latter.
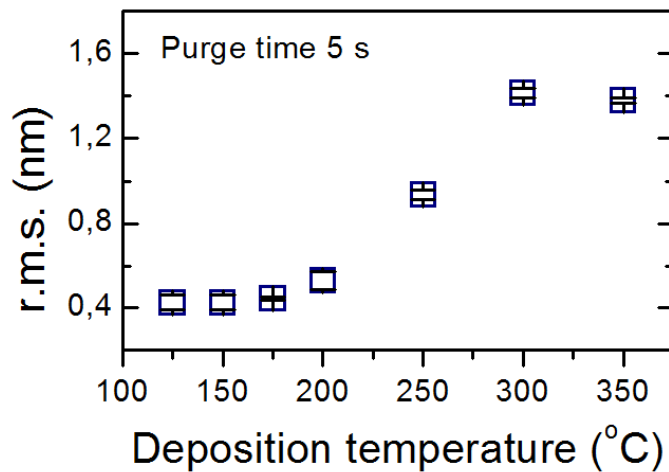

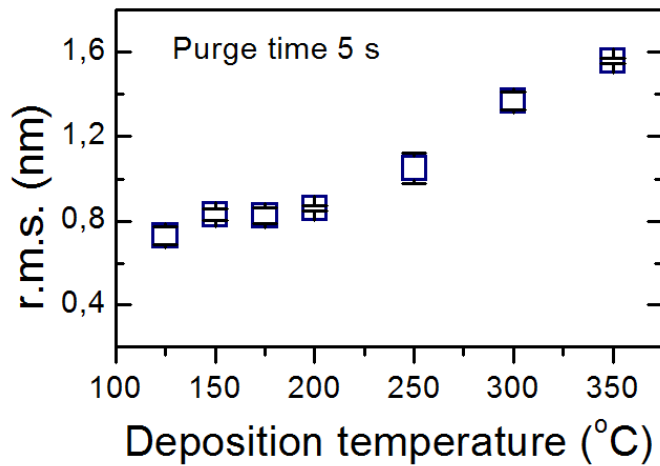Figure 3.4: HfO_2 film on $SiSiO_2$ surface roughness value as a function of the deposition temperature.

Figure 3.5: surface roughness value of HfO_2 film on $SiSiO_2$/Ti as a function of the deposition temperature.
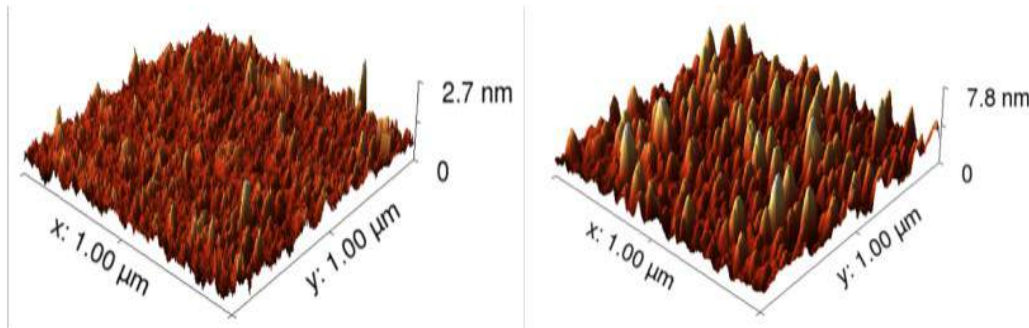
Figure 3.6: 3D AFM images obtained from 20 nm thick HfO_2 thin films grown at 150°C (left) and 300°C (right) on $SiSiO_2$ substrates.

This surface roughness increasing is in agreement with results reported in literature[1-3]. An explanation for this increasing of the roughness at the samples deposited at 300°C and 350°C may be related with its polycrystalline structure unlike the mainly amorphous structure found for lower deposition temperatures as it will be described at section 3.3.

In the same way than the analysis carried out to study the deposition temperature effect on surface roughness, a set of HfO_2 films (20 nm) were grown on bared $SiSiO_2$ and $SiSiO_2$/ Ti (20nm) substrates to analyze the effect of the purge time on the surface roughness. The samples were deposited at different purge time values maintaining constant the rest of the deposition process parameters as described above (see table 3.4).

Oxygen precursor pulse	0.015 s
Hafnium precursor pulse	0.15 s
Deposition temperature	150°C

Table 3.4: parameters values applied at HfO_2 deposition process for the study of the purge time effect on the surface roughness.

The surface roughness is highly conditioned by the initial density of active sites, as hydroxyl groups (-OH) in our case. In this way an initial situation with very

few active sites for nucleation yields to a high surface roughness. However as the density of active sites is enough the surface becomes covered by the film and it leads to smoother surfaces[4]. Regarding the effect of purge time on roughness, an increasing length of the purge step could enable a dehydroxylation of the surface in certain degree, reducing the number of active sites on it and then increasing the rms roughness[5].
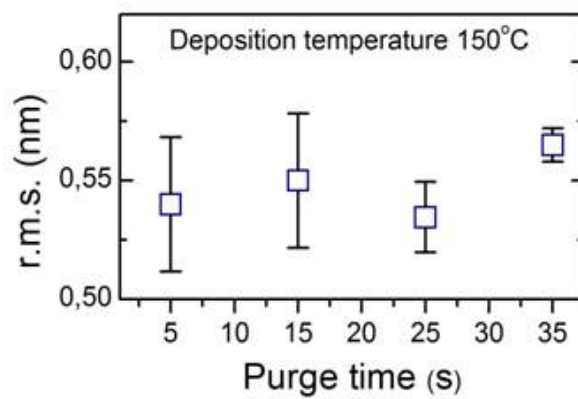

Figure 3.7: HfO$_2$ film on SiO$_2$Si surface roughness value as a function of the purge time.
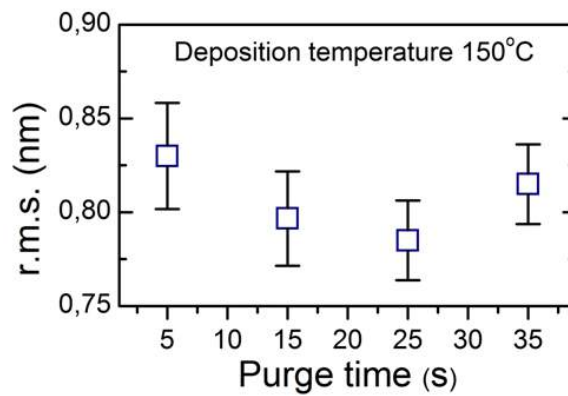
Figure 3.8: roughness value of HfO$_2$ films on SiSiO$_2$/Ti surface as a function of the purge time.

Figures 3.7 and 3.8 show similar rms roughness values for the films deposited at different purge time both on $SiSiO_2$ and $SiSiO_2/Ti$ respectively. AFM results suggested no effect on the film surface roughness of the purge time applied during the fabrication process. It would indicate that at a deposition temperature of 150°C the purge time lengths applied did not affect the number of active sites on the surface that could yield to a significant variation on the surface roughness.

3.2 Thin film thickness and growth rate determination

Reflectivity X-ray (XRR) technique was used to determine the HfO_2 thin films thicknesses as well as the growth rate of the ALD process at different deposition temperatures. Additionally, we studied the effect on the growth rate of the deposition temperature and purge time through two set of samples. At one set of samples the HfO_2 thin films were grown at a range of temperatures from 125°C to 350°C keeping the rest of fabrication parameters constant. At a second set we varied the purge time within a range of 5 to 35 seconds with a constant deposition temperature of 150°C. In order to study the growth rate behavior of ALD process, HfO_2 thin films were grown at three different temperatures: 125, 200 and 300°C. As mentioned at section 2.1, the HfO_2 films were fabricated on silicon oxide surface using tetrakis (dimethylamido)Hafnium (TDMAH) and water as metal and oxygen precursors respectively. The values of the rest of the parameters of the deposition process were constant and are reflected at table 3.5. Prior the deposition the substrates were cleaned following the process described at section 2.2. At each deposition temperature different numbers of cycles were deposited, 50, 100, 150 and 200, and the corresponding thicknesses measured by reflectivity X-ray as depicted at figure 3.9.

Oxygen precursor length	0.015 s
Hafnium precursor length	0.15 s
Purge time for both precursor	5 s

Table 3.5: parameters values applied at HfO_2 deposition process for the study of the deposition temperature effect on the growth rate.
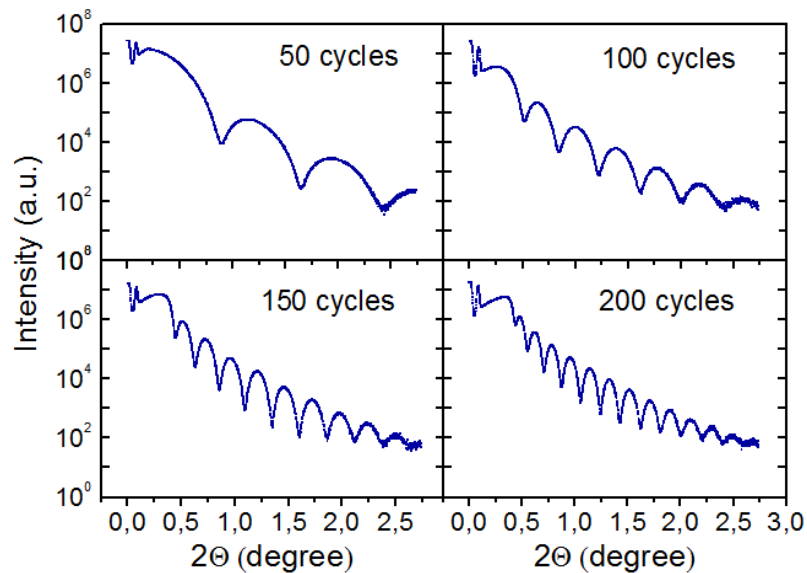

Figure 3.9: X-ray reflection curves corresponding to HfO_2 thin films with different number of growth cycles at deposition temperature of 200°C.

The linear dependence of the film thickness on the number of growth cycles applied was demonstrated and displayed at figure 3.10 for the three deposition temperatures analyzed. The extrapolation of the curves results in a line, which intersects with the Y-axis at the origin referring to the non-retarded nucleation[3]. It means that from the very first cycles, the surface becomes fully covered by the film and the growth is linear from the beginning. It indicates in turn that the surface contains an enough density of active reaction hydroxyl groups (-OH). In contrast, if there is only few or any hydroxyl active groups on the surface, the growth rate is

slower at the beginning during the nucleation period, and it takes a certain number of cycles to achieve a linear correlation between the thickness and the number of ALD cycles (retarded nucleation).
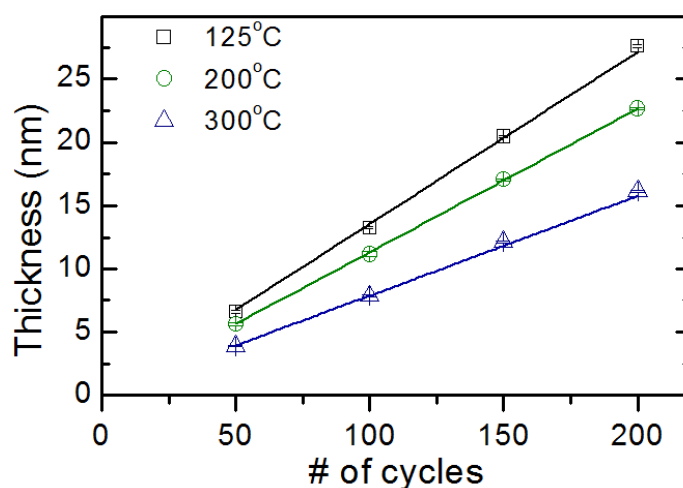

Figure 3.10: growth rate of HfO$_2$ films deposited at 125 °C, 200 °C and 300°C.

The growth rate was found to be dependent on the deposition temperature, and as the deposition temperature increased the growth rate diminished. This dependence is consistent with a lower hydroxyl groups desorption rate from the surface at lower deposition temperatures what leads to higher growth rate[3].

TEM images verified the smooth of the as deposited Ti and HfO$_2$ thin films. Figure 3.11 depicts the TEM image from the 20 nm thick HfO$_2$ film grown at 125°C on a 20 nm thick Ti film that confirmed the AFM results. Besides TEM images revealed an amorphous HfO$_2$ structure in 125°C deposited sample that was also further corroborated by X-ray analysis (see section 3.3).

In order to study the influence of the deposition temperature on the growth rate of the ALD deposition process, a set of HfO$_2$ thin films were grown changing only in the deposition temperature and keeping constant the rest of parameters (see table 3.6). The deposition temperatures were: 125°C, 150°C, 175°C, 200°C, 250°C, 300°C and 350°C. The figure 3.12 shows the growth rates obtained as a function of

the deposition temperature and as it can be observed a decreasing of the growth rate with the deposition temperature was found. This result is consistent with the literature where authors appealed the lower growth rate to a partial dehydroxylation of the surface at high temperature, i.e., a lower density of hydroxyl (-OH) active surface sites [3]. The hydroxyl groups are regenerated on the surface after each water pulse, but at high temperatures the dehydroxylation is not negligible and their density remains lower leading to a decrease of the growth rate[5].
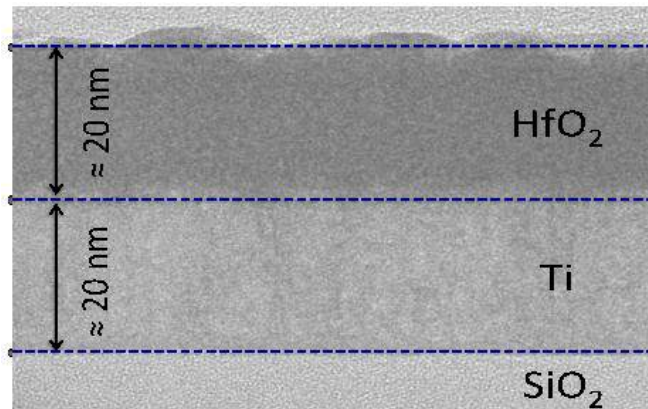
Figure 3.11: Transmison electron microscopy image of the 20 nm HfO_2 grown on $SiSiO_2$/Ti (20 nm) at 125°C.

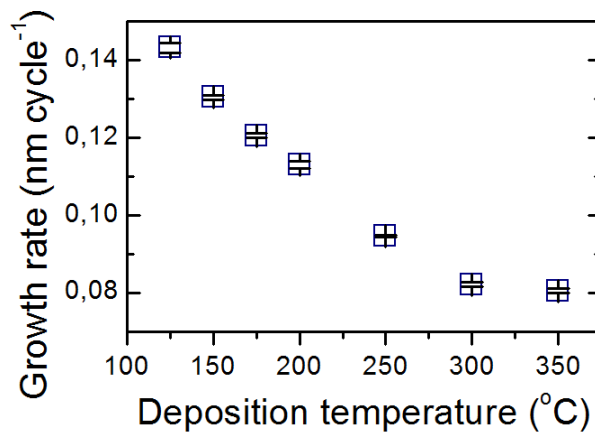
Figure 3.12: growth rate as a function of the deposition temperature.

Regarding the effect of the purge time during the HfO_2 deposition process effect on the growth rate, it was analyzed by a set of thin films were grown varying uniquely the purge time: 5, 15, 25 and 35 seconds. Table 3.6 shows the parameters values used during the HfO_2 deposition processes.

Oxygen precursor lenght	0.015 s
Hafnium precursor lenght	0.15 s
Deposition temperature	150°C

Table 3.6: parameters values applied at HfO_2 deposition process for the study of the purge time effect on the growth rate.
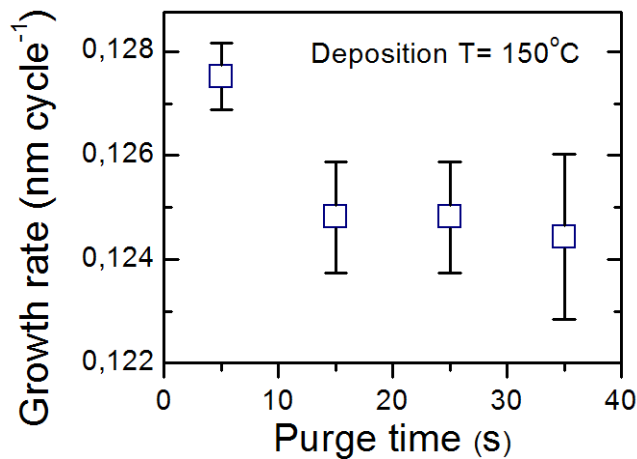

Figure 3.13: growth rate as a function of the purge time.

The curve from figure 3.13 shows a slight higher growth rate for the shorter purge time (5 seconds) to decrease and become stable for larger purge time values evaluated. This slight larger growth rate at short purge times has been already reported. In particular, as it was described above an increasing length of the purge step enables a dehydroxylation of the surface in certain degree and thus to a decrease of the density of the active adsorption sites and growth rate[2].

3.3 Crystalline structure determination of the HfO_2 thin films

This technique was used for the study of the structure and the phase characterization of 20 nm thick HfO_2 thin films grown at different deposition temperatures. The use of low incident angles avoids in the spectra peaks coming from the substrate and allows a larger sensitivity and phase analysis.
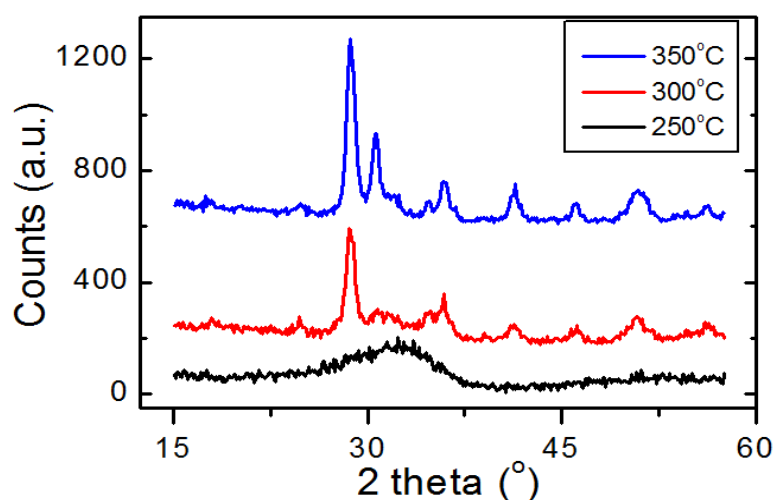

Figure 3.14: GIXRD spectra obtained for 20nm thick HfO_2 films grown at 250ºC, 300ºC and 350ºC.

Figure 3.14 shows the grazing incidence X-ray diffraction scan ranging 2 from 15 to 90º with a step size of 0.1º for a set of samples growth at 250ºC, 300 ºC and 350. The HfO_2 thin films deposited from 125ºC to 250ºC exhibited amorphous structure (as observed at Figure 3.11) displaying a broad hump. In contrast the HfO_2 thin films grown at 300ºC and 350ºC displayed a polycrystalline film structure. Nearly the totality of the observed Bragg peaks can be assigned to the monoclinic polymorph (see figure 3.15) in agreement with previous observations[5-10]. Although the monoclinic phase is the thermodynamically stable one minor trace reflections

assignable to metastable phases emerged at $\approx$ 30.3°. This peak has been attributable to the orthorhombic HfO_2, as well as to the tetragonal and cubic phase[10-12]. An increase of the Bragg peaks intensity was observed with the deposition temperature. The crystal structure information was provided by the database of the spectrometer software.
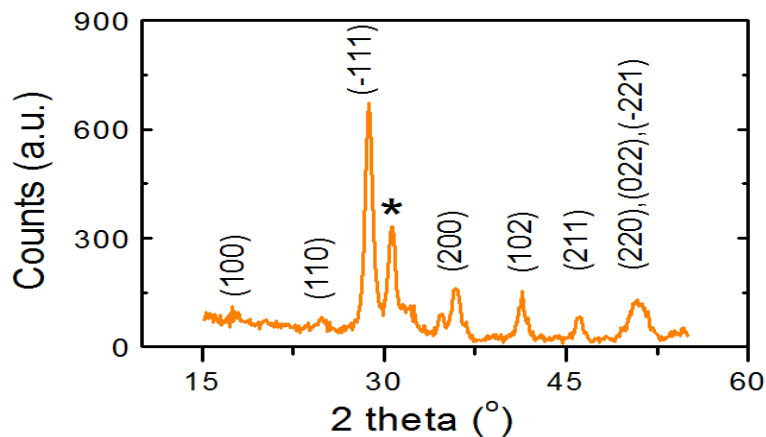

Figure 3.15: GIXRD spectra from 20 nm thick HfO_2 grown at 350°C. Labels give plane reflections of monoclinic phase except peak labelled with a star (*).

The study of the effect of thermal annealing process on the phase structure carried out with the $Ti/HfO_2/Co$ growth at 300°C and 5 seconds purge time. Annealing treatments at 500°C and 600°C were conducted for 10 seconds at an oven with Nitrogen flux. Figure 3.16 shows the GIXRD spectra obtained after the different annealing processes and together with the spectra from the as deposited device at 300°C and 5 seconds purge time. As can be observed the first effect was the increasing of the peaks intensity denoting a larger crystallization degree. No additional peaks were observed after the thermal treatment indicating the absence of new phases into the HfO_2 thin film, which displayed monoclinic phase as indicated previously.
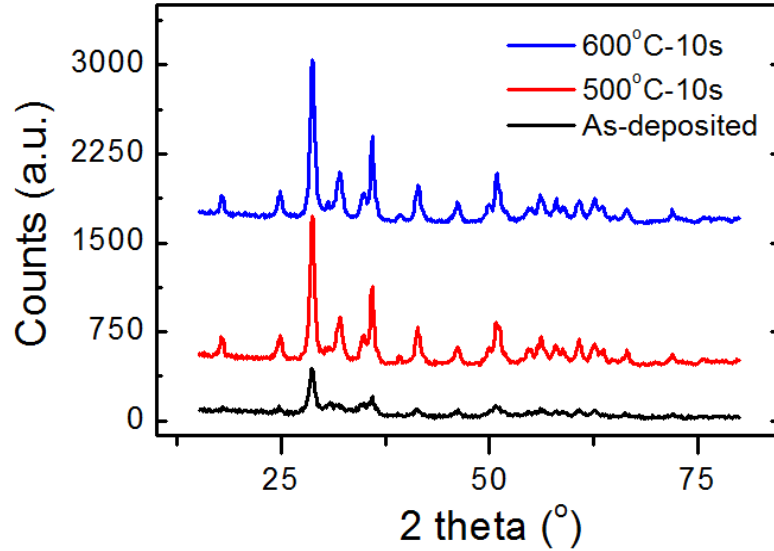
Figure 3.16: GIXRD spectra from 20 nm thick HfO$_2$ as deposited (grown at 300ºC), and after a thermal treatment for 10 seconds at 500ºC and 600ºC.

An enlargement of the grain size was found after determining the average diameter of crystalline grains from the width of the diffraction line by using the next formula:

$$d = \frac{k\,\lambda}{b\,\cos\theta} \qquad\qquad (1)$$

where λ =1.5405 Amstrongs (Cu K), k=0.4 if b=b$_{1/2}$, the line width at half maximum. The most intense line of the spectra was used, and b was previously converted in radians. The average diameter of crystalline grain increased from the 9 nm at as deposited HfO$_2$ at 300ºC, to 12 nm for both thermal treatments.

The impact of the thermal treatments on the electrical properties of the device was studied and the results exposed at chapter 6.

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CHAPTER 4

Metal/Insulator/Semiconductor devices

As it was mentioned previously along the thesis two types of HfO_2-based samples, metal/insulating/ semiconductor (MIS) and metal/insulating /metal (MIM), are fabricated and characterized to determine if they fulfil the required properties for a potential application as non volatile memory. In this chapter we present the result obtained from the electrical characterization of metal/insulating /semiconductor (MIS) HfO_2 based devices. Two different MIS devices with different metal top electrodes, aluminum and cobalt, were characterized by conducting current-voltage (I-V) curves and the application of voltage pulses.

4.1 Current-voltage curves

The principal requirement for non volatile memory application is the stable store of data, namely "1" or "0". As described at chapter 1.3, in the case of the resistive switching (RS hereafter) the binary data are stored through two resistance states that can be alternated by the application of an electric field. The current-voltage curves allow identifying if a system exhibits two alternating resistance states expressed by a hysteretic I-V curve. Besides, the application of successive I-V curves allows determining the degree of stability and reproducibility of the two resistance states.

The electrical characterization of the metal/insulating/semiconductor (MIS) devices was carried out at a probe station and using a source meter Keithley2635A at room temperature. All the measurements were conducted with two tips on two top contacts. As described at section 2.2, three samples were fabricated by growing

the HfO_2 film at 175 °C, 200 °C and 250ºC with 25, 20 and 15 seconds of purge time respectively. Two different metals were tested as top contacts: aluminium and cobalt. Following we described the results obtained during the electrical characterization.

4.1.1   Aluminum top electrode MIS devices

The $Al/HfO_2/Si$ samples were characterized via the application of I-V curves sweeping different voltage value ranges. The general behaviour did not exhibit any RS effect (figure 4.1a) or it was random resistance changes without any reproducibility (figure 4.1b).
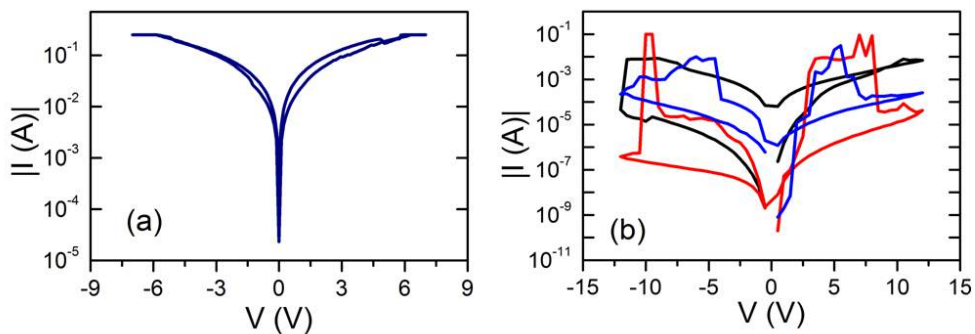

Figure 4.1: (a) I-V curves exhibiting non reproducible switching performance for $Al/HfO_2/Si$ device with HfO_2 grown at 200ºC. (b) Random performance found at three successive curves at $Al/HfO_2/Si$ device grown at 250ºC.

In few devices hysteretic I-V curve was obtained but it cannot be considered representative of the general behaviour. The RS showed bipolar behaviour but faded away after a short number of curves (in general no more than 15 cycles) where scarce reproducibility was found as illustrated at figure 4.2. The poor performance in the $Al/HfO_2/Si$ devices was observed in the totality of the samples independently of the HfO_2 growing conditions.
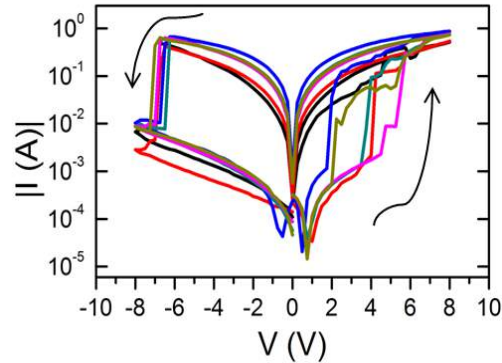
Figure 4.2: bipolar switching exhibited for Al/HfO$_2$/Si device with HfO$_2$ grown at 175°C.

The measurements carried out with the Al top electrode MIS devices revealed no reproducible and unstable resistive switching. During the characterization and after few I-V curves the Aluminium top contacts got damaged, probably produced by the high currents passing through the electrodes (~1 A).

4.1.2   Cobalt top electrode MIS devices

Regarding the general behaviour found for the Co/HfO$_2$/Si devices, it was comparable with that observed at Aluminium devices. The I-V curves did not exhibit hysteretic behaviour (figure 4.3) and when it was found displayed large dispersion of switching parameters as set and reset voltage value (see figure 4.4). The hysteretic curve showed bipolar behaviour and large currents close to 1A associated to the LRS. Another feature was the current peak at negative bias when the bias value approaches zero volts. This peak, which drifts to higher bias values with the number of measurements, might be accounted for capacitive or inductive effects.
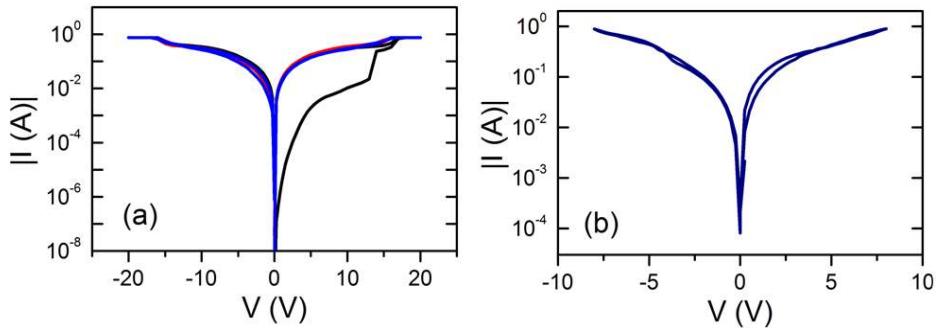
Figure 4.3: representative I-V curve of the non switching performance found at Co/HfO$_2$/Si devices observed for devices with HfO$_2$ grown at 175°C (a) and 250°C.
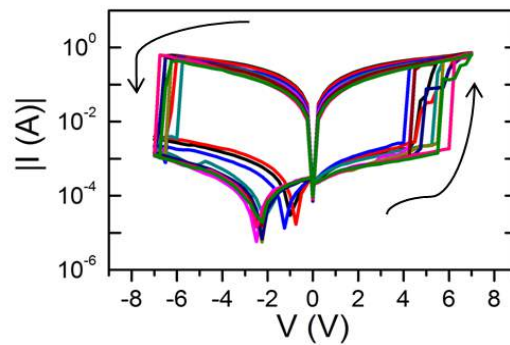
Figure 4.4: (a) successive characteristics I-V curve of switching performance observed at Co/HfO$_2$/Si devices with HfO$_2$ grown at 200°C.

The MIS HfO$_2$-based devices exhibited general poor switching performance and just few devices showed hysteretic behaviour but with a high dispersion in switching parameters. Despite that, the memory properties of devices that showed hysteretic I-V curves as shown at figure 4.4 were tested as described at the next section.

4.2 Voltage pulses analysis

As mentioned at the previous section, the non volatile memory properties of those cobalt top electrode MIS devices that exhibited hysteretic behaviour were examined. The analysis was conducted via sequences of logical memory processes, i.e. writing, reading and erasing, through the application of voltage pulses as detailed at section 2.3. These voltage pulses were applied with the biased and grounded tips on top and bottom electrode respectively. The logical operations through which the device is switched to LRS and HRS are the writing and erasing respectively, while the reading operations are applied to sense the resistance state of the device (HRS or LRS). Figure 4.5 shows the logical processes carried out by electrical voltage pulses 20 ms width.
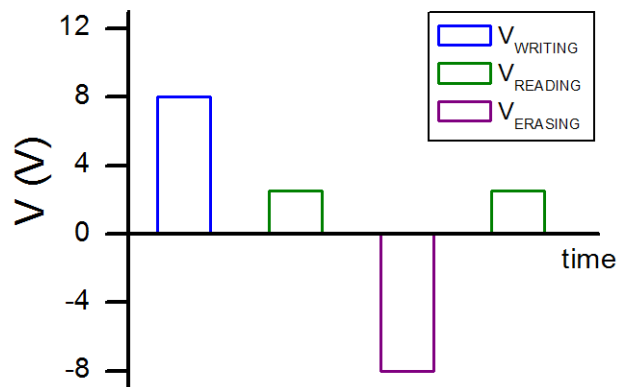

Figure 4.5: Voltage values applied to induce the logical operations. The writing step triggers the device to the LRS, verified by the current measured at the following reading step while the second reading current ratifies the back to HRS produced by the erasing step.

The writing pulse must be larger than the V_{SET} to induce the switching to the LRS meanwhile the reading pulse must be below such V_{SET} for preventing any change on the resistance state during sensing. The writing, erasing and reading voltages

applied were +8, -8 and +2.5V respectively. The results obtained after multiple measurements revealed that the devices did not show good memory properties mainly due to failed set and reset processes (see figure 4.6). Despite the application of different voltage values for the set, reset and reading steps, it did not yield any improvement on the performance.
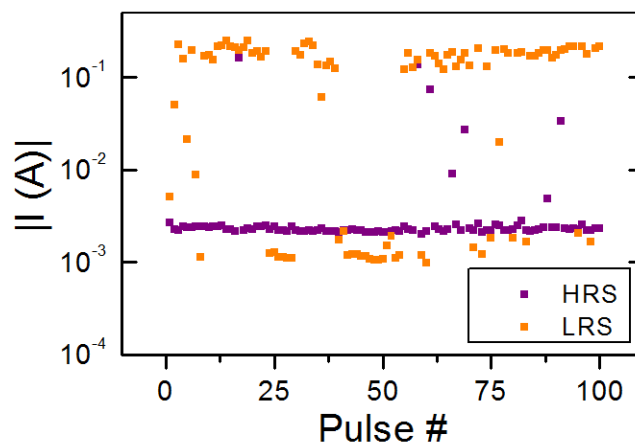

Figure 4.6: Currents sensed corresponded to the reading pulses after the writing (LRS) and erasing (HRS) voltage pulses obtained for a Co/HfO$_2$/Si device with HfO$_2$ grown at 200°C.

Thus, most of MIS devices analyzed did not show hysteretic I-V characteristics, and those that did it, exhibited poor performance derived from the lack of reliability and reproducibility of the hysteretic I-V curves. They were significant handicaps that hinder their potential application as non volatile memory device. From now on, we will focus on the study and analysis of the metal/Insulator/metal (MIM) devices and its potential application as non volatile memory.

CHAPTER 5

Metal/Insulator/Metal devices

In this chapter we present the results obtained from the electrical characterization of metal/insulating/metal (MIM) HfO_2 based devices that combined different bottom/top metal electrodes. The electrical characterization via current-voltage (I-V) curves showed that a particular MIM device (Ti/HfO_2/Co) displayed stable and reproducible bipolar resistive switching as well as an unusual non-crossing I-V curve. The interpretation of such I-V curve was accomplished by different electrical measuring protocols as minor loops and hysteresis switching loops. The results revealed bipolar resistive switching (RS) that occurs complementarily at both metal/oxide interfaces. The device memory properties were confirmed in turn by stability and retention measurements as well as voltage pulses, by which logical computational processes were conducted. Finally, we treat the annealing treatment effect on the electric properties and the device memory properties.

5.1 Current-voltage curves

Different metal/insulating/metal (MIM) samples with different bottom-top electrodes were characterized by conducting I-V curves. Recalling section 2.2 the metals selected to form the bottom electrodes were Titanium and Palladium, while five metals were tested as top electrodes: Gold, Cobalt, Chromium, Titanium and Palladium (table 5.1). The HfO_2 thin film was grown at 300ºC and applying 5 seconds of purge time for all the samples. The measurements were performed at a probe station using a source meter Keithley 2635A at room temperature. The voltage

sweeping was in the range of 15 to -15V, with a 0.3V step size and with the top and the bottom electrodes biased and grounded respectively. The different samples were characterized by applying successive I-V curves in order to determine the display/absence of hysteretic behaviour, and in the case of displaying it to study its reproducibility.

Bottom electrode	Top electrode
Pd	Pd
	Ti
	Au
	Co
	Cr
Ti	Pd
	Ti
	Au
	Co
	Cr

Table 5.1: set of metal/insulating/metal devices characterized electrically.

5.1.1   Palladium bottom electrode based devices

The resulting I-V curves obtained from the characterization of palladium bottom electrode samples showed that if no current limit compliance was applied all the devices underwent an irreversible electrical. As can be observed at figure 5.1 obtained from the Pd/HfO$_2$/Ti device, with the increase of the applied bias from 0 to 15 V, the device shows an initial high resistance state (HRS) and at ~ 6V experiences a set process reflected by an abrupt current increasing (blue curve) that leads to the

low resistance state (LRS). After this set process the device did not return back to the HRS (orange curve) despite the application of tens of successive I-V curves. This behaviour was found in the rest of Pd bottom electrode devices independently of the top metal electrode as showed at figure 5.2.
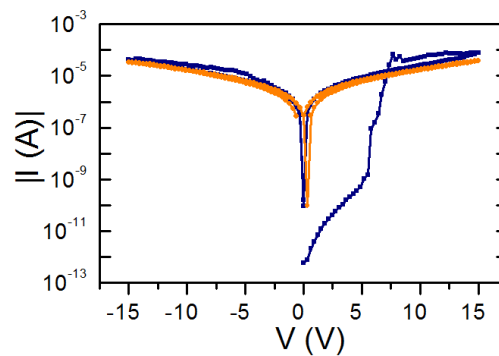

Figure 5.1: I-V curve obtained for Pd/HfO$_2$/Ti without current limit compliance (cc).
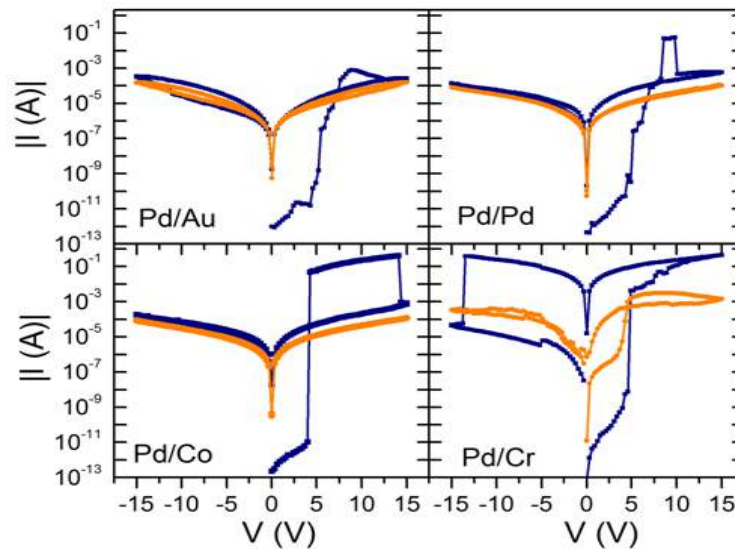

Figure 5.2: characteristic I-V curves obtained for every Pd bottom electrode device characterized without current limit compliance. The blue curve represents the first I-V curve while the orange curve exhibits the I-V curve obtained after the device breakdown.

It seems that irreversible breakdown of the device occurs due to a too high current passing through the device. In a similar way than the aluminium top contacts at the MIS devices, the high currents degraded Pd and Cr top electrodes as illustrated at figure 5.3. This top electrode degradation has been earlier reported[1-3] and ascribed to the O_2 bubbles formation under the anode metal.
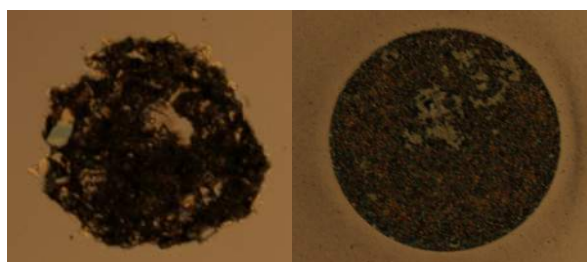

Figure 5.3: degraded Chromium (left) and Palladium (right) top contacts during the electrical characterization.

In order to avoid these undesirable effects, current limit compliance was applied. It led to current limited hysteretic I-V curves as showed at figure 5.4 (blue curve) where the arrows indicate the curve direction. As positive bias from 0 to 15V was applied the device exhibited an initial HRS and a set process at ~ 6V led to the LRS reaching the limit current compliance value (path 1). The device maintained the LRS without breakdown and gave rise to a hysteretic curve as reflected by path 2. As polarity is reversed a significant feature emerges. Notice that despite the device was in a LRS at the end of the voltage sweep at positive values, as soon as the voltage value turned negative, the device exhibited a new HRS. The change of resistance state as the polarity is reversed yielded to an unusual non-crossing I-V curve that will be analyzed ahead in this chapter. At negative voltage values analogous behaviour was found and HRS was displayed until a set process induced the LRS (path 3). The device operated in LRS during the bias return to zero (path 4) displaying a hysteretic curve also at the negative branch. Nevertheless the hysteretic curve was found to be not stable more than 10 successive I-V curves and it suffered a breakdown (orange curve).

Different current compliance values were applied but in all the cases with the same unsatisfactory result of not accomplishing a stable hysteretic curve and hence two stable and alternating resistance states. This behaviour was representative for all the devices with Pd bottom electrode independently of the metal top electrode as showed at figure 5.5.
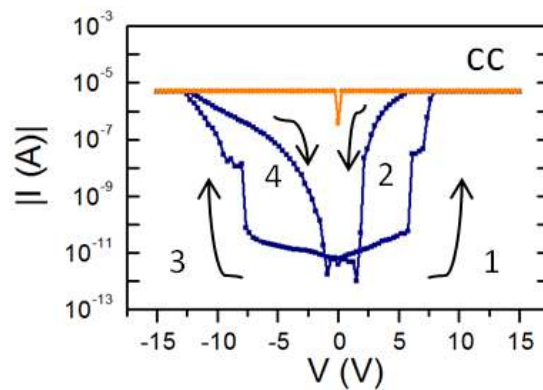

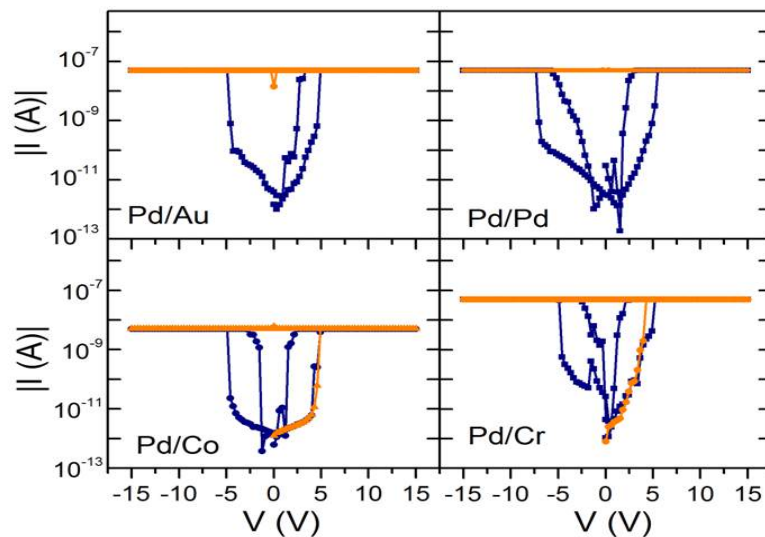Figure 5.4: I-V curve obtained for Pd/HfO$_2$/Ti with current limit compliance (cc).

Figure 5.5: characteristic I-V curves obtained for every Pd bottom electrode device characterized with current limit compliance. The blue curve represents the first I-V curve while the orange curve exhibits the device breakdown after no more than 10 cycles.

Thus the results obtained from the palladium bottom electrode devices showed that these devices underwent a dielectric breakdown the application of current compliance and regardless the metal top electrode. Despite the application of current compliance yielded to hysteretic curves it was not stable and the devices finally underwent electric breakdown after a short number of cycles (in general no more than 10). In conclusion Pd bottom electrode devices did not exhibit a stable hysteretic curve and hence the required manifestation of two stable and switchable resistance states for a potential application as resistive memory. This poor performance may be related with the nature of the bottom electrode as it will be described ahead in this chapter.

5.1.2 Titanium bottom electrode based devices

The Titanium bottom electrode devices were characterized by performing I-V curves in the same way that carried out with the palladium bottom electrode devices. In this way, succeeding dc voltage sweeps 0V→15V→0V→-15V→0V were conducted resulting in the corresponding I-V curves showed at figure 5.6. The main difference found respecting to the palladium bottom electrode devices was the self-limiting current at LRS displayed by the titanium bottom electrode devices. In this sense no limit current compliance application was necessary as no breakdown effect was observed in any case. All the devices exhibited hysteretic I-V as reflected by figure 5.6 (blue curve) where the arrows indicate the curve direction. As can be noted at figure 5.6 the hysteretic curves displayed an analogous behaviour than the palladium devices. Thus, the devices showed an initial HRS to switch to the LRS via the set process. The LRS was preserved during the sweep back to zero volts deriving in a hysteretic curve at the positive branch. Similar behaviour was observed at the negative branch, i.e., an initial HRS that changed to LRS via a set step that was sustained, and originated a hysteretic curve. However the hysteresis was not stable and after a number of cycles (<25) it showed a lack of reproducibility reflected in a

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considerable degradation or it vanished (orange curve) for all the devices except in the case of the Ti/HfO$_2$/Co device [figure 5.7(a)].
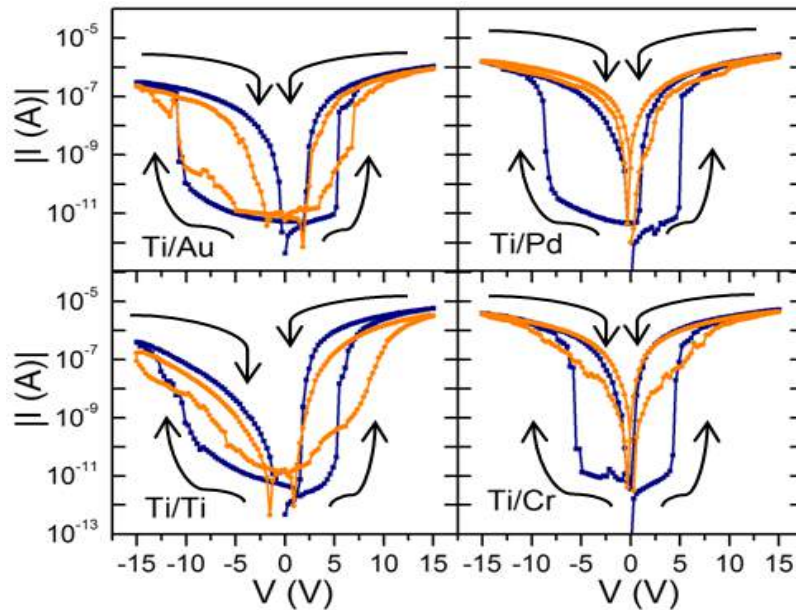

Figure 5.6: characteristic I-V curves obtained for every Ti bottom electrode device. The blue curve represent the first I-V curve (blue line) while the orange curve exhibits the I-V curve obtained after 25 cycles (orange line).

The Ti/HfO$_2$/Co device by contrast exhibited I-V curves with remarkable stability, reflected on a significant reproducibility after 100 cycles [figure 5.7(b)]. The display of stable and alternating switching between two different resistance states could make it suitable for a non-volatile memory application. Hereafter As it was previously observed in the Pd bottom electrode devices, a significant feature of the I-V curves obtained is its unusual non-crossing nature, i.e., the resistance state sensed changed from LRS to HRS at bias polarity is reversed. A deeper study of this non-crossing feature, by means of different measuring protocols, together with its physical interpretation is exposed ahead. The results obtained from both type of MIM devices lead to consider that the metal electrode choice is not trivial and it might have a considerable effect on the device performance. In fact, the effect of the metal

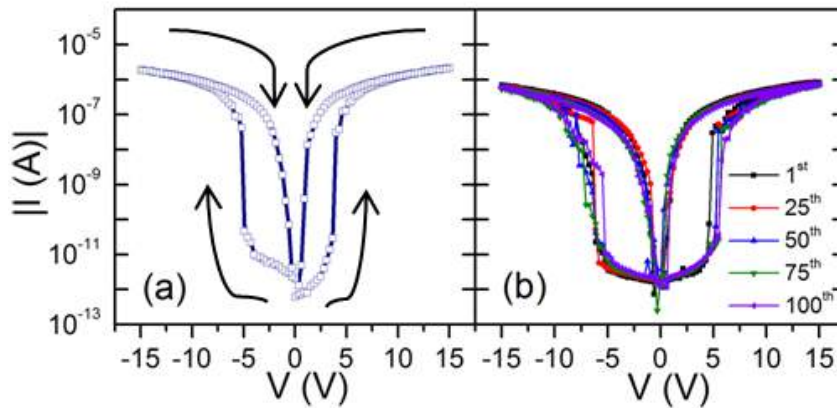electrodes on the conduction mechanism at MIM structures has been earlier reported[4-7].

Figure 5.7: (a) characteristic I-V curve obtained for the Ti/HfO$_2$/Co device. (b) I-V curves displaying the 1st, 25th, 50th, 75th and 100th cycle and confirming the robustness of the device.

In particular, Sawa and coworkers[4] reported the role of high oxygen affinity metals on the origin of rectifying Ti/Pr$_{0.7}$Ca$_{0.3}$MnO$_3$ (PCMO) interface. They reported that Ti layer possibly extracts a large amount of oxygen from the PCMO surface generating oxygen vacancies at interfacial regions, which would induce a high density of interface states. They proposed a switching model whereby the high density of states produces a large degree of the band bending of the Ti/PCMO interface. Lee and co-workers[6] reported very similar conclusions at SrRuO$_3$/Cr-doped SrZrO$_3$/metal junctions. Concerning MIM-HfO$_2$ based devices, the influence of oxygen vacancies at the metal/oxide interface on the Schottky barrier width was reported by Vallée and co-workers[6]. The impact of the oxygen affinity of the electrode metals on the conduction mechanism of MIM HfO$_2$-based devices was also reported[7]. Authors claimed that metal with high oxygen affinity induce oxygen vacancies accumulation at the interface that modify its depletion layer width and consequently the conduction mechanism. In the case of the palladium such oxygen affinity is not given due to its inert nature as noble metal. This could be a significant

point to account for the poor performance exhibited by the palladium bottom devices. The mentioned literature must have to be considered ahead for the interpretation of further characterization results due to the high oxygen affinity of the metal electrodes of our device (Ti and Co).

5.2 Analysis of Ti/HfO$_2$/Co devices

5.2.1 Analysis of the non-crossing I-V curve

As showed at the previous section, a significant feature displayed by the I-V curves was the change of the resistive state sensed (from LRS to HRS) as the voltage polarity was reversed leading to a non-crossing curve as figure 5.8 shows.
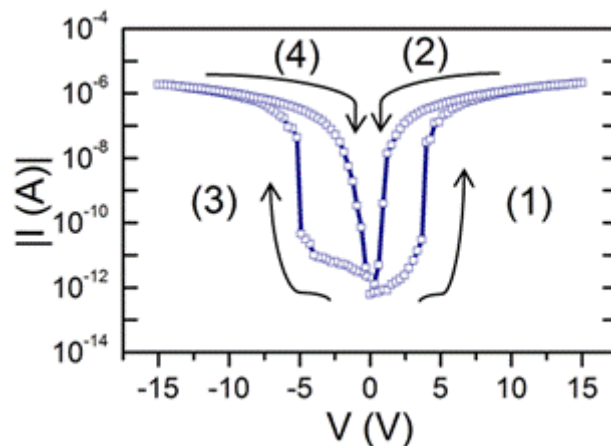

Figure 5.8: typical I-V curve obtained for the Ti/HfO$_2$/Co device.

As a positive voltage bias is applied and the voltage reaches a value around +4.5V, the resistance is drastically reduced and the device is switched to the LRS by a SET process as reflected by the path 1 at figure 5.8. The device operates at LRS until the bias is swept back towards zero (path 2) and the I-V curve exhibits a hysteretic curve. However, when the voltage is reversed the resistance state sensed to HRS. An

analogous picture is found at the negative branch of the curve with a SET step at $\sim$ -5V (path 3) and a subsequent LRS (path 4).

Figure 5.9 sketch the conceptual difference between the typical I-V curve of a bipolar RS device and the I-V characteristic of our device.
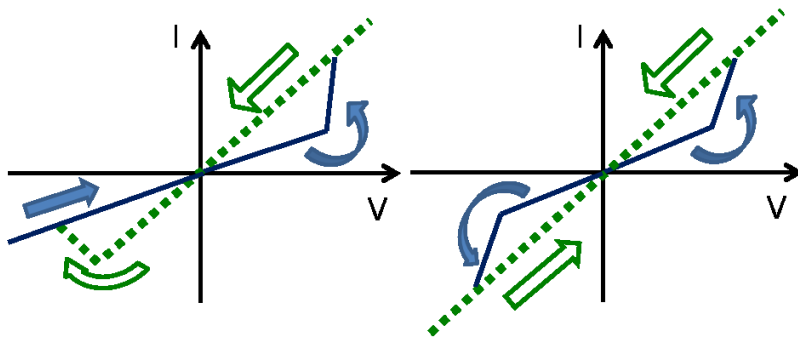

Figure 5.9: characteristic I-V loop displayed for a bipolar RS behaviour (left) and for our MIM structure (right). Dotted line represents the low resistance state, straight line the high resistance state, and the arrows the direction of the curve.

The behaviour of our devices is manifested in an unusual non-crossing I-V curve at the origin instead the characteristic self-crossing I-V curve at zero bias, which is an usual feature of materials exhibiting bipolar RS[8] (see figure 5.9). Furthermore, the resistance change from LRS to HRS when the polarity is reversed. Similar non-crossing I-V curves were previously reported in ZnO[9] and TiO$_2$[10]. Therein the authors appealed to a formation/annihilation of oxygen vacancies at the interfaces along with the contribution of both interfaces to resistance change, to explain the behaviour observed. This type of non-crossing curve has been also reported in systems with complementary RS interfaces[11]. These scenarios must be accounted for further results interpretation.

On the other hand it is noticeable that only SET processes are observable at both bias polarities of the I-V curve whereas no RESET processes could be discerned. Also, the device operates at the HRS regardless of the voltage bias applied at the beginning of the measurement (paths 1 and 3 in figure 5.8).

At this point it is demanded to clarify for the whole understanding of the I-V characteristics the next facts: the origin of the two SET processes, and why we do not discern the RESET processes that should be associated to the observed SET steps. Different measuring protocols as minor loops and hysteresis switching loops were conducted with that purpose as described in the next sections.

5.2.2   Minor loops

If we assume a bipolar nature of the RS in our devices the RESET and SET processes would occur at opposite voltage polarity. In order to confirm that we conducted minor loops measurements which consisted of the application of voltage sweeps as follows: $0V \to 15V \to A \to 15V \to 0V$, where A is a variable voltage value, with a step size of 0.3V. Here the A voltage values applied were: 0, -1, -2 and -3V. The measurements began with the device in an initial HRS, which was switched to the LRS as showed by path 1 in Figure 5.10(a).
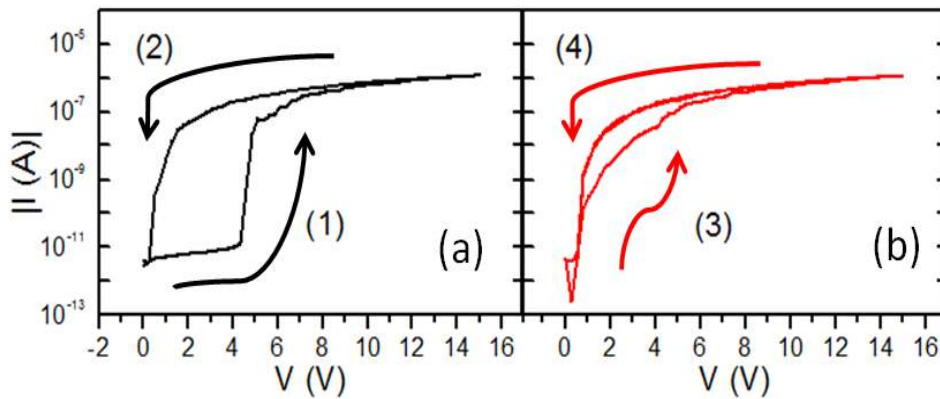

Figure 5.10: (a) Experimental minor loop where the system was set to the LRS from the HRS (path 1) and after the device was swept to 0V (path 2). (b) An increasing of the resistance state was found reflected by the path 3. The final LRS was confirmed by path 4.

When the voltage was then swept back to zero volts (path 2), it resulted in an increase of the resistance state of the device as shown by subsequently path 3 at figure 5.10(b). The resistance state of the device was found to exhibit a gradual enhance with increasing applied voltage A (Figure 5.11b-c). As the voltage was swept to more negative values the resistance state during the initial stages of path 3 became more robust until, when the voltage was swept to -3V (Figure 5.11d), the initial HRS was recovered. This means that a voltage value of opposite polarity with respect to the SET process is required to produce the RESET process, as reflected in Figure 5.11b-d, indicating clearly bipolar behaviour. Comparable results were obtained when these measurements were conducted using the opposite polarity, as illustrated at Figure 5.12.
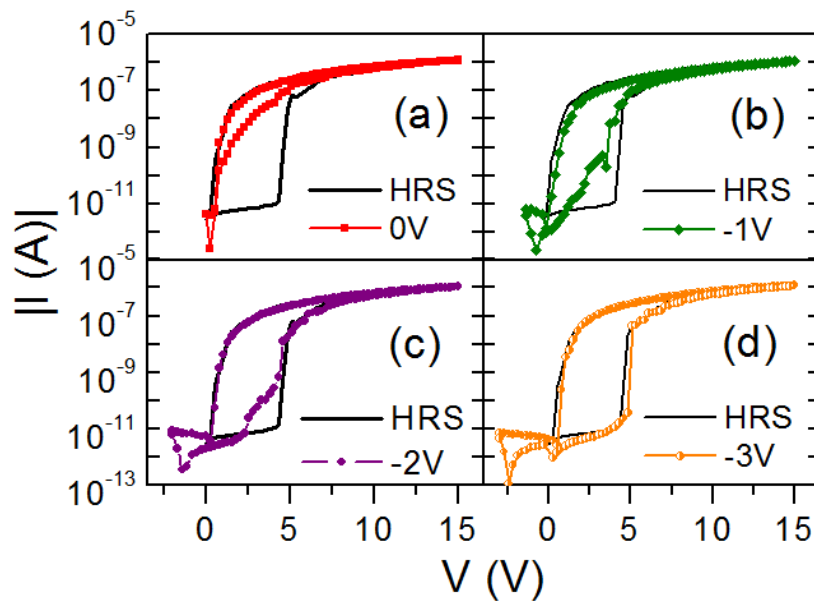

Figure 5.11: Minor loops obtained for the positive branch of the I-V curve for the Ti/HfO$_2$/Co device (HfO$_2$ deposited at 300ºC and 5 seconds of purge time).
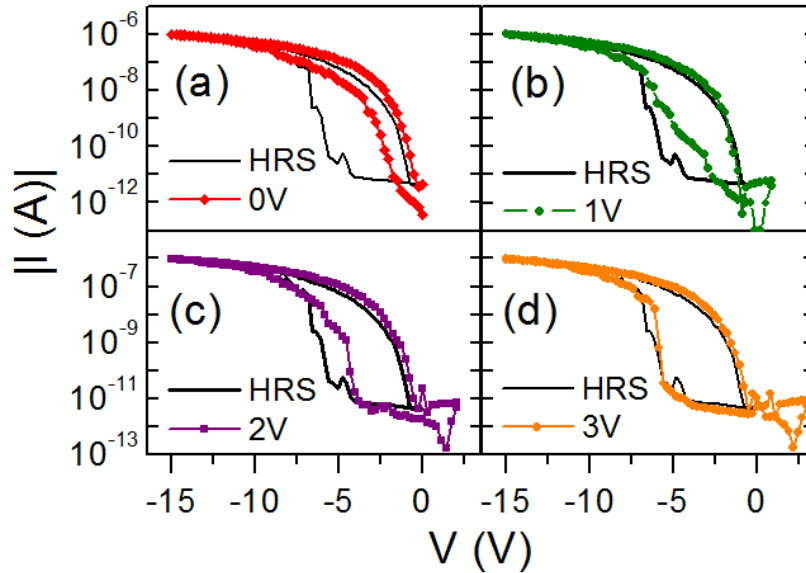
Figure 5.12: Minor loops obtained for the negative branch of the I-V curve for the Ti/HfO$_2$/Co device (HfO$_2$ deposited at 300°C and 5 seconds of purge time).

These results suggested the existence of two SET-RESET processes taking place at opposite voltage polarity that could point at the idea of two independent RS processes at the device. Additionally, this could be related with the existence of two active metal/oxide interfaces as previously observed at TiO$_2$[10] and manganites devices[12], i.e., both interfaces can be switched between a HRS and a LRS by the application of electric pulses. If this assumption were correct, it would indicate a configuration in series of two switching interfaces which would account for the unusual non-crossing I-V curve. Furthermore, the LRS of one junction would be concurrent with the HRS of the opposite junction at a given bias polarity, explaining the transition from LRS to HRS when the voltage polarity is reversed.

In order to gain a deeper insight of the interfaces properties individually and corroborate the presence of two active interfaces, we carried out hysteresis switching loops described in the next section.

5.2.3   Hysteresis switching loops

In order to disentangle the contribution of each interface, hysteresis switching loops (HSL) at opposite bias voltages were conducted. As described at section 2.3 HSL is a parametric plot that displays the evolution of the remnant resistance of a RS device during the application of a train of electrical pulses[13]. Throughout this thesis, HSL plots are defined as the sequence of points $[V_{PULSE}(i), R_{REM}(i,V_{READ})]$, being i the pulse index, V_{PULSE} the voltage of the i-th pulse and R_{REM} is the remnant resistance after the i-th pulse, which is sensed with the reading voltage V_{READ}. The top and bottom electrodes were biased and grounded respectively.

The HSL of Fig. 5.13(a) was obtained with positive V_{READ} = 4V applying 20ms-width pulses with a sequence 0V→15V→-5V→0V in steps of 100 mV.
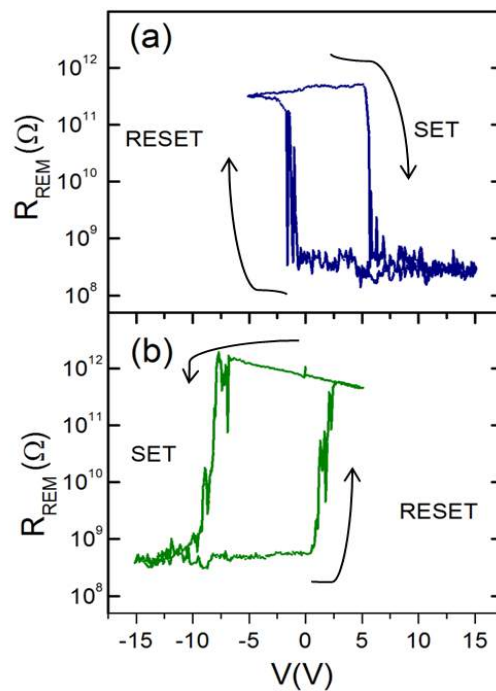

Figure 5.13: Hysteresis switching loops obtained for the positive (a) and negative branch (b) for a reading potential pulse of 4V and -4V respectively.

The data clearly corroborates the bipolar character of the resistive switching. It also shows that for the Ti/HfO_{2-x} interface the minimum SET voltage is ~5V. Even if the RESET procedure starts at low voltages, pulses should overcome ~-3V to ensure proper RESET. For negative V_{READ} = -4V, Fig. 5.13(b) evidences that the SET and RESET voltages of the Co/HfO_{2-x} interface are ~ -10V and ~3V respectively. From these HSLs is also evident that the interfaces are complementary, e.g., a positive voltage SETs the Ti/HfO_{2-x} interface but RESETs the Co/HfO_{2-x} interface. Here, the polarity of this V_{READ} is crucial due to the rectifying character of the interfaces. At positive V_{READ}, the current flowing through the device is mainly limited by the Ti/HfO_{2-x} interface and the HfO_{2-x} layer; the other interface is in direct bias so that it presents a negligible resistance. Assuming that the HfO_{2-x} bulk does not modify its resistance, any effect observed in the HSL that is acquired with positive reading voltage, is attributed to resistive switching in the Ti/HfO_{2-x} interface. Complementary, the HSL obtained with negative V_{READ} reveals RS in the Co/HfO_{2-x} interface.

As it was proposed earlier, this scenario could be represented by a physical scheme composed of two diodes in a back-to-back configuration with a resistor in between. The back-to-back diodes represent the rectifying properties of the two MS interfaces while the resistor depicts the bulk oxide. During an HSL at a given V_{READ} polarity one MS junction behaves as a "reverse-biased" while the opposite interface behaves as a "forward-biased". In this way, the former MS junction, where the main voltage drop is located, displays rectifying properties. However, the latter presents slight limitation to the current independently of its resistance state. When the V_{READ} polarity is reversed the opposite situation is given and we sense the properties of the other MS junction. That leads us to realize that during an I-V curve, for a given bias polarity we sense only the metal/oxide interface that is "reversed-biased". Once the bias is reversed the I-V curve reflects the resistance state of the other metal/oxide interface, previously "forward-biased" and then "reversed-biased".

The results given by conducting minor loops and hysteresis switching loops indicated the existence of two active metal/oxide interfaces that display bipolar behaviour: Ti/HfO_2 and Co/HfO_2. We used hysteresis switching loop with opposite

sensing bias in order to disentangle the contribution of each interface. In addition, "complementary" character of the switching effect at the interfaces was confirmed.

5.3 Resistive switching measurements

The non-volatile memory properties of the Ti/HfO$_2$/Co MIM devices were explored through diverse electrical protocols whose results are described in this section.

5.3.1 Voltage pulses analysis

In order to corroborate the required properties for potential application as non-volatile memory device, sequences of logical memory processes (writing, reading and erasing) were performed through the application of voltage pulses. The voltage pulses were applied as detailed at section 2.3 with the biased and grounded tips on top and bottom electrode respectively. Figure 5.14 shows the logical processes carried out by electrical voltage pulses (20 ms width) and the concomitant currents for the positive I-V branch. At Figure 5.14(a) the device is switched from the HRS to the LRS by a writing pulse (+13V) and during the subsequent reading operation (pulse of +4V) a meaningful current denoting the LRS of the device is sensed. The next erasing pulse (-4V) triggers the switching back to HRS, confirmed by the current sensed at second reading operation. This sequence of pulses was carried out successfully more than 1.5 x 10^3 times without degeneration [1st and 1500th pulses exhibited at Figure 5.14(b)], confirming the device capability as non-volatile memory cell. Voltage pulses results agreed the bipolar nature of the RS. Regarding the non-volatile memory properties of the device they were confirmed after 1.5 x10^3 train pulses. The device showed the capacity to switch between two stable resistance states by the application of voltage pulses and it was reflected by the reading currents values corresponding to the HRS and LRS at figure 5.14.
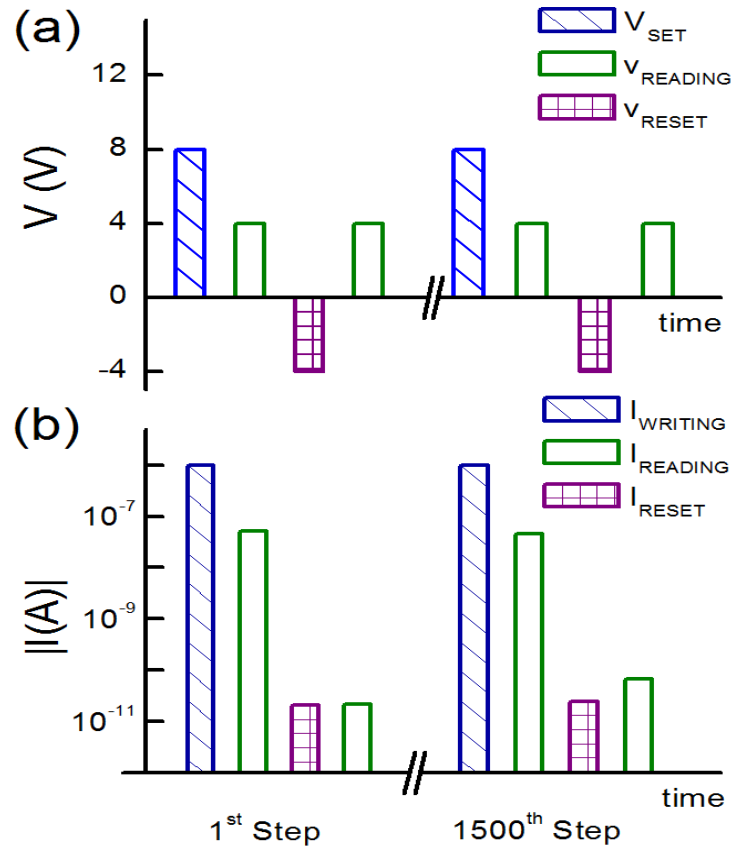
Figure 5.14: Voltage applied (a) and the corresponding currents (b) at 1st and 1500th pulse train for the Ti/HfO$_2$/Co device (HfO$_2$ grown at 300°C and 5 seconds of purge time). The writing step triggers the device to the LRS, confirmed by the current measured at the following reading step and the second reading current ratifies the back to HRS produced by the erasing step.

The histogram of the currents measured for both resistance states is shown at Figure 5.15(a). Their average current values for the HRS and the LRS were 1.97x10^{-8} ± 1.88x10^{-8} A, and 8.67x10^{-11} ± 5.11x10^{-12} A, respectively. A memory window gap of one order of magnitude can be discerned in between HRS and LRS. At figure 5.15(b) the evolution of the reading currents values versus the number of reading pulses is showed.
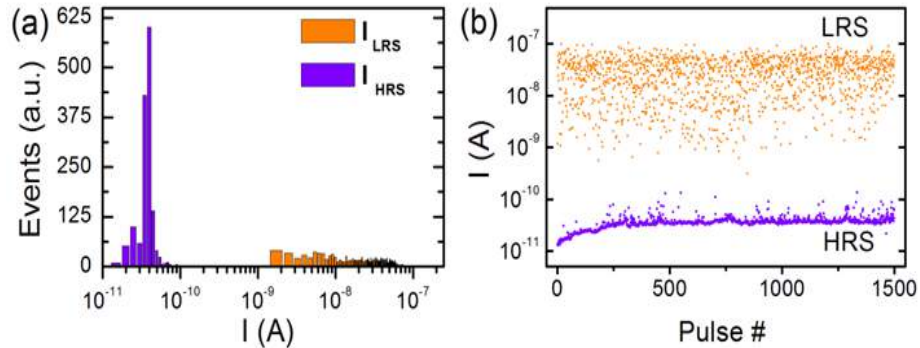
Figure 5.15: (a) Statistics of the currents obtained from the reading voltage pulses after the writing (I_{LRS}) and erasing (I_{HRS}) voltage pulses. (b) Currents sensed corresponded to the reading pulses after the writing (I_{LRS}) and erasing (I_{HRS}) voltage pulses.

The main features found were the slight dispersion found at the LRS reading currents and the stability of the HRS reading current. The dispersion exhibited by the LRS reading currents could be related with the slight resistance increasing that the system experiments when the voltage is swept to zero volts as exposed previously at figure 5.10. If such slight resistance increasing varies from one reading pulse to the next, it would affect the resistance state sensed through the reading voltage step and would originate the LRS reading current dispersion.

5.3.2   Reproducibility and stability measurements

The memory properties analysis was widened with the performance of stability and retention experiments. The measurements were carried out with the biased and grounded tips on top and bottom electrode respectively. Stability measurement consisted of setting the resistance state at either LRS or HRS by the application of an appropriate voltage pulse (+4V to set the device to the LRS, and -5V to reset it to the HRS), and applying 400 successive reading steps (+4.2V) in order to test the steadiness degree of such resistance states. It was carried out for both HRS and LRS for the positive branch. The histogram of the currents measured for both

resistance states is shown at Figure 5.16a. Their average current values for the HRS and the LRS were $1.97 \times 10^{-8} \pm 1.88 \times 10^{-8}$ A, and $8.67 \times 10^{-11} \pm 5.11 \times 10^{-12}$ A, respectively.
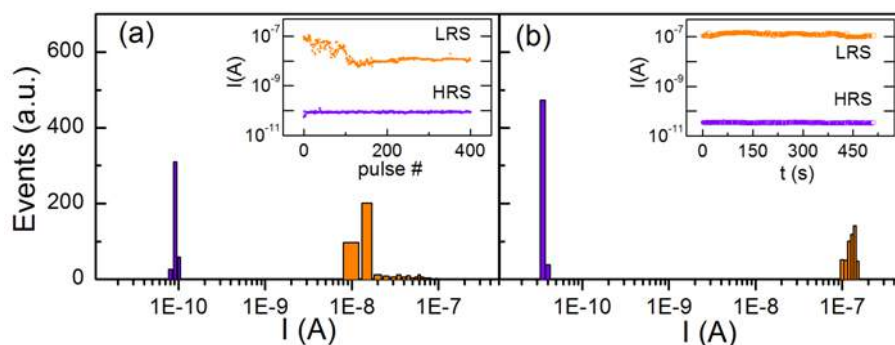

Figure 5.16: Histogram of the reading current values obtained for the HRS and the LRS for (a) stability and (b) retention measurements of Ti/HfO$_2$/Co device with HfO$_2$ deposition conditions of 300°C and 5 seconds of purge time. Inset (a): reading current values as a function of the number of pulses applied. Inset (b): reading current values as a function of time.

On the other hand, retention analysis were driven by setting the device at either LRS or HRS by the application of an appropriate voltage pulse as described above, and measure uninterruptedly the current value under the application of a constant voltage value (+3.75V) for a time (500 s). Figure 5.16b exhibits the histogram obtained from the reading currents at both resistance states. Their average current values and the corresponding standard deviations for HRS and LRS are $3.39 \times 10^{-11} \pm 6.46 \times 10^{-13}$ A and $1.23 \times 10^{-7} \pm 1.40 \times 10^{-8}$ A, respectively. The I_{LRS}/I_{HRS} ratios for stability and retention measurements were 2 and 3 orders of magnitude, respectively. The results from both stability and retention measurements exhibit no degradation of the resistance states, preserving a wide memory window.

Thus, good memory properties of the Ti/HfO$_2$/Co device (grown at 300°C and 5 seconds purged) have been proved via the application of different measuring protocols making it suitable for a potential non volatile memory device.

5.4 Annealed samples

Along this section we study the effect of thermal annealing processes on the resistive switching displayed by the device Ti/HfO$_2$/Co (growth at 300°C and 5 seconds purged). Regarding the effects of the annealing treatments on the crystalline structure they were exposed at section 3.3, although it is convenient to remind that they resulted in an increasing of the crystalline degree and average diameter of crystalline grains from 9 nm to 12 nm (for both annealing treatments) respecting to the as deposited device at 300°C.

Two different annealing treatments were conducted for 10 seconds; one at 500°C and another at 600°C, both carried out at an oven with Nitrogen flux into the chamber. After the annealing process the samples were firstly characterized by performing current-voltage (I-V) measurements. Figure 5.16 displays the corresponding I-V curves obtained for the annealed devices together with that of the as deposited device for comparison.
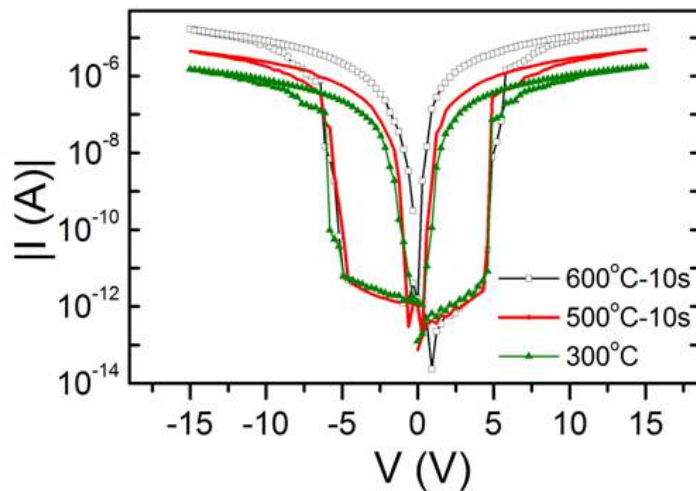

Figure 5.16: characteristic I-V curves obtained from Ti/HfO$_2$/Co devices as deposited at 300°C and 5 seconds purge time, and after 10 seconds thermal annealing at 500°C and 600°C.

It was noticed that the annealing process seemed not to have any effect on either the set voltage value or the currents associated to the HRS. However growing current associated with the LRS was found together with the annealing temperature applied to the device leading to an enlargement of the I_{LRS}/I_{HRS} ratio.

These results agree with some literature[14,15] where it was reported that annealing treatments enhanced the capacity of some metals to get oxygen from the HfO_2 and hence to increase the number of oxygen vacancies. A larger amount of oxygen vacancies at the metal/oxide interface would yield a higher doping level, i.e., higher number of energy states at the band gap respecting to as-deposited samples, leading to larger currents associated to the LRS.

On the other hand, in order to determine the thermal treatment effect on the memory properties, voltage logical memory sequences (writing, reading and erasing), were performed in the same way than described before at section 5.17. The results from both annealed samples revealed two main effects (see Figures 5.17 and 5.18). On the one hand an increase of the reading currents associated to the LRS that agrees with the measured I-V curves. On the other hand, a continuous degradation of the HRS not observed before at as-deposited samples. This degradation affected negatively to the memory capabilities of the devices by a significant and progressive narrowing of the memory window gap.
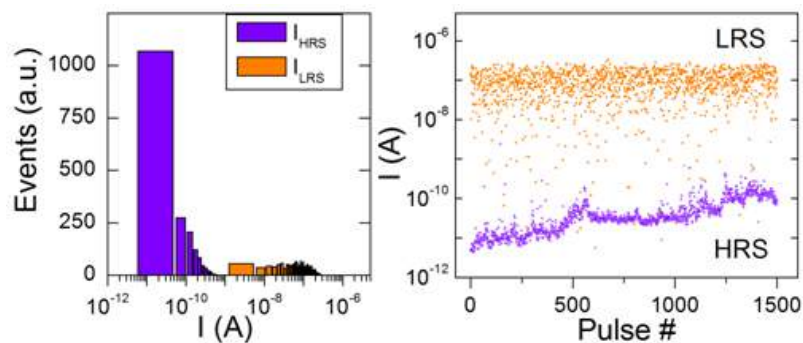

Figure 5.17: (a) Statistics of the LRS and HRS reading currents after 1.5×10^3 pulses sequences from device annealed at 500°C for 10 seconds. (b) Reading currents for LRS and HRS versus the reading pulse number.
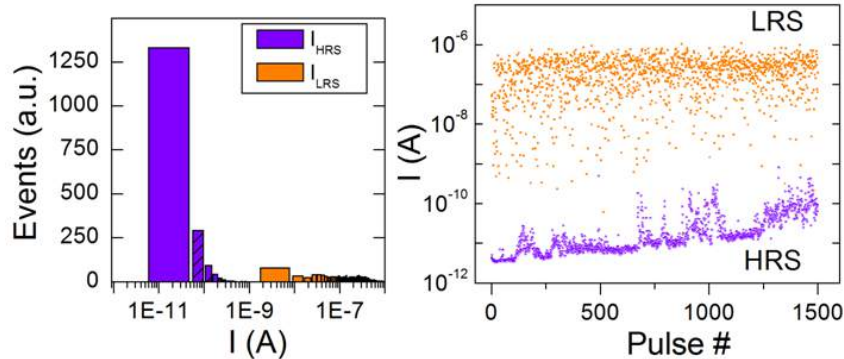
Figure 5.18: (a) Statistics of the LRS and HRS reading currents after 1.5×10^3 pulses sequences from device annealed at 600ºC for 10 seconds. (b) Reading currents for LRS and HRS versus the reading pulse number.

A similar degradation of the memory performance was reported by Marlasca et al[16] in manganites-based memory cells. Therein the redistribution of oxygen vacancies at interfacial regions was crucial for the RS behaviour. They attributed the degradation to a continuous and irreversible accumulation of oxygen vacancies at the interface region that reduces progressively the interface resistance at HRS has been reported in manganites. According to the authors, upon the application of an electric field, local electric fields proportional to the local resistivity are developed and the oxygen vacancies drift towards the interface region varying its local profile and hence the interface resistance. After the change of the local oxygen vacancies, an electric field of opposite polarity might not reproduce the original electric field that induced the initial diffusion of the oxygen vacancies. Then, the vacancies would not return to the original positions and the interface resistance would not return to its original value.

If we assume this scenario at our devices, we could state that the increase of the bulk crystallinity degree and the corresponding vacancies diffusion enhancement affect negatively in our devices to the reproducibility of the vacancies distribution profile. Therefore annealing processes caused an increment of the crystallinity degree of the HfO_2 and the average size crystalline grain. Concerning the memory properties, the results showed a decay of such properties caused by the degradation

of the high resistance state. Eventually, these results seem to confirm a key role of the oxygen vacancies into the switching mechanism.

At this point the electrical characterization has confirmed the bipolar nature of the RS response in our devices. Nowadays it is widely accepted[17-20] that the distribution of oxygen vacancies driven by the electric fields built up at interfacial regions, is the main driving force of the resistive changes occurred at bipolar behaviour systems, also in HfO_2-based devices[21-23]. This switching mechanism was exposed and described at the introduction of this thesis (section 1.3.2). In order to study the effect of the ALD conditions on the RS response we fabricated samples at different deposition conditions which exhibited different RS response as detailed at the next chapter.

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CHAPTER 6

Effect of temperature processing on resistive switching

In this chapter we study the effect of the atomic layer deposition conditions on the electric properties of the samples. It was carried out by the characterization of 26 samples fabricated at different conditions. The results clearly indicated that the fabrication conditions conditioned the resistive switching (RS) response as reflected in a parameter diagram. The effects on RS response of the deposition temperature and the purge time are described and discussed. In the final section of the chapter we present the results obtained from the chemical characterization conducted by means of X-ray photoelectron spectroscopy (XPS). This chemical analysis of the HfO_2 thin films both at the bulk and at the Ti/HfO_2 interfacial regions provided us with a physical correlation between the HfO_2 growing conditions and the electrical response found at different devices.

6.1 ALD conditions effect on resistive switching

The effect of the HfO_2 growth conditions on RS as a function of the deposition temperature and the purge time applied was analyzed by the fabrication of $Ti/HfO_2/Co$ devices. In total 26 $Ti/HfO_2/Co$ samples each containing 80 devices (16 rows x 5 columns), were fabricated at different HfO_2 growth conditions. An extensive statistics was carried out at each of the 26 different samples. In this way, at each sample at least 10 different devices were characterized by applying 10 successive I-V curves following the next voltage sweep: $0V \rightarrow 15V \rightarrow 0V \rightarrow -15V \rightarrow 0V$, with 0.3 V step size and top (bottom) electrode biased (grounded) in all cases.
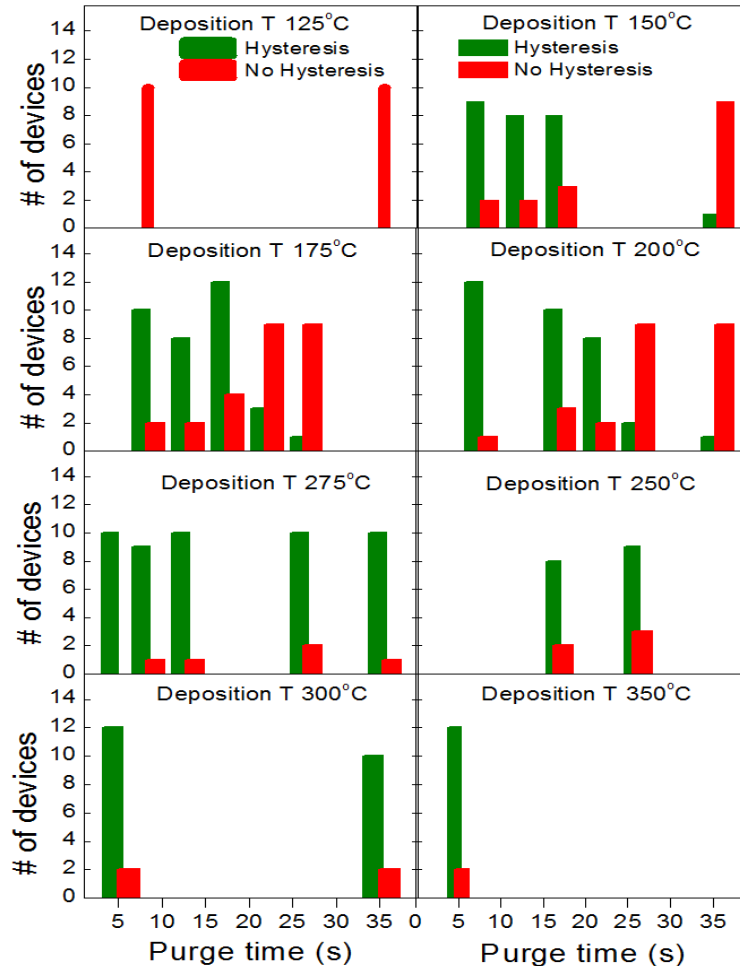
Figure 6.1: Histograms showing the results of the electrical characterization obtained from samples fabricated at different conditions.

The characterization of the samples was conducted by testing at least two devices per column to make it representative of the whole sample. Along the characterization two types of samples were found; those that exhibited hysteretic curve and those that did not. The results obtained for each device showed reproducibility of at least 80% in the behaviour displayed. Depending of the fabrication conditions the electrical response varied as can be observed at figure 6.1 which shows the characterization results for each deposition temperature as a function of the purge time.
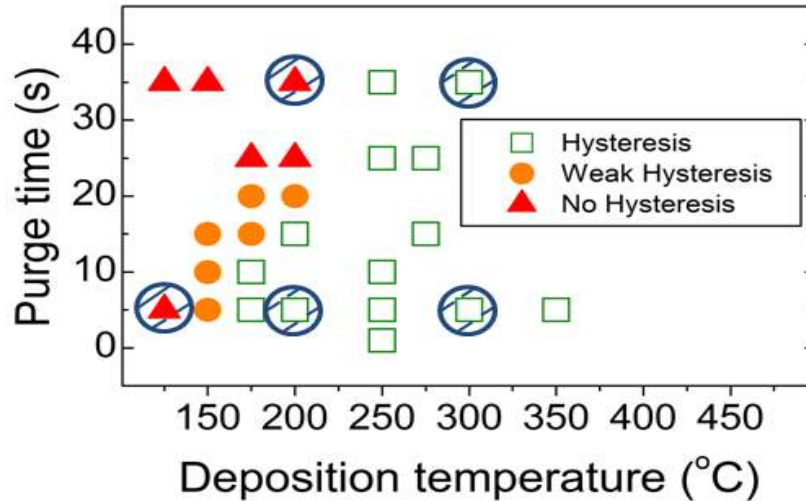
Figure 6.2: Summary of resistive switching behaviour (see text for definitions) obtained for samples fabricated at different deposition temperatures and purge times. The electrical characterization was carried out at 10 devices per sample in order to get a reliable statistics to form the parameter diagram. The samples inside the patterned circles were analysed by XPS.

In the case of the samples displaying hysteresis, a criterion of reliability was established in order to determine the robustness of the hysteretic curve. Such criterion was based on 150 successful switching I-V cycles and used to discern between hysteretic and weak hysteretic behaviour (being weak hysteretic devices those whose hysteresis faded away before 150 cycles). The resulting statistic was gathered into the parameter diagram displayed in Figure 6.2, where the results obtained from the characterization are showed as a function of the robustness criterion before mentioned. In this way, the parameter diagram suggested a trend whereby the manifestation of the RS seemed to be unfavoured as low temperatures and long purge times are applied during the HfO_2 growing process. On the contrary, devices grown at high temperatures and short purge times were more prone to exhibit stable RS effect. In between, as a result of the reliability criterion applied, we found an intermediate performance (weak hysteresis) where the initial hysteretic curve did not endure up to 150 I-V cycles. Consequently, the RS effect manifestation

seems to be supported under certain HfO_2 grown conditions as high deposition temperatures and short purge times. The parameter diagram also revealed that samples with both amorphous and polycrystalline HfO_2 showed RS. This is a very remarkable point as it indicated us that there was not direct correlation between HfO_2 crystallinity degree and RS manifestation. Thus, it seemed that the source of the resistive switching effect was still to be elucidated.

The parameters diagram confirmed the influence of ALD growing conditions on the RS response. Following we described separately the effect of the deposition temperature and the purge time reflected on experimental I-V curves from devices grown at different conditions.

6.1.1   Deposition temperature effect on resistive switching

As it was mentioned at the previous section, the ALD growing conditions affect the RS performance. In this section we analyze a set of devices grown at different deposition temperatures and a common purge time of 5 seconds to study the effect of the deposition temperature on the RS effect. This purge time (5 seconds) was selected as the tree electrical behaviours before described (hysteresis, weak hysteresis and no hysteresis) are observed in the range of deposition temperatures at this purge time value. The results obtained from the electrical characterization are showed at Figure 6.3 which displays a substantial relation between the deposition temperature and the resistance hysteresis absence/manifestation. It was found that the sample deposited at the lowest deposition temperature (125ºC) did not display RS. However RS effect could be observed for higher deposition temperatures and the increasing of the deposition temperature came together with an enlargement of the resistance ratio between the LRS and the HRS denoted as the ratio between the LRS and HRS currents (I_{LRS}/I_{HRS}).

This increase of the I_{LRS}/I_{HRS} ratio was essentially due to an increase in the current associated with the LRS.
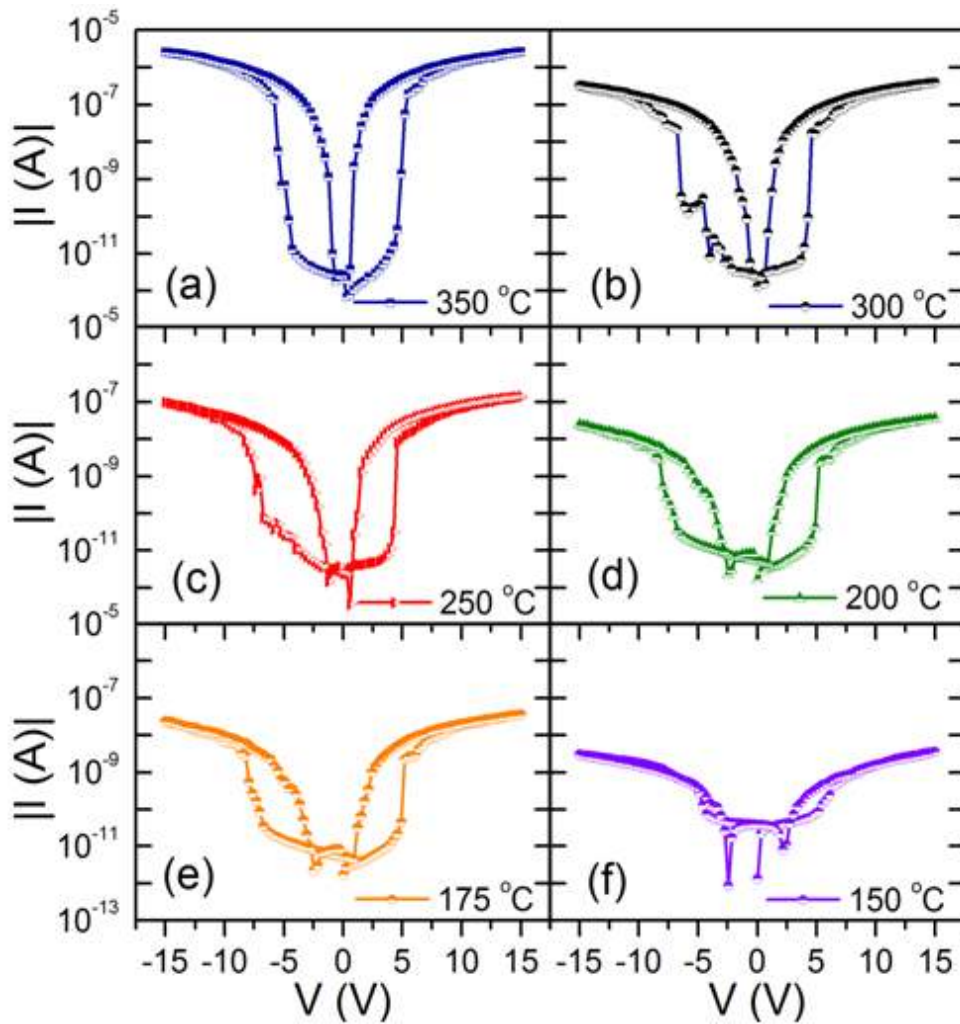

Figure 6.3: I-V curves corresponding to samples with HfO_2 grown with 5 seconds purge time but at different deposition temperature

But, do these results agree with the switching mechanism described at the previous section? If we assume such switching mechanism we could interpret these results as follows. The capacity of the Ti layer to form oxygen compounds is

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temperature dependent and the absence or low amount of oxygen vacancies may be reflected on both non-switching and weak hysteresis devices for deposition temperatures of 125°C and 150 °C respectively. However switching devices are obtained from a deposition temperature of 175 °C confirming the enhanced Ti capacity to react with the oxygen with the temperature. Therefore, higher oxygen vacancies density would be originated at higher deposition temperature at the interface what would lead to a more noticeable resistance modulation of the interface, and consequently larger LRS currents (larger I_{LRS}/I_{HRS}).

6.1.2   Purge time effect on resistive switching

Similarly to the analysis carried out at the former section, here we analyzed the results obtained from the characterization of a set of samples growth with different purge time and common deposition temperature (200°C). Again, we study these devices under this deposition temperature (200°C) as at the range of purge time values explored the tree electrical responses were found. The experimental I-V curves are content at Figure 6.4 and show an increased I_{LRS}/I_{HRS} ratio observed when the purge time is reduced. Accordingly RS effect was promoted by short purge times at a given deposition temperature, while long purge times seemed to inhibit the RS manifestation. Following with the assumption exposed earlier it would lead to consider that according to the results the purge time value has a notable effect on the number of oxygen vacancies originated at the metal/oxide interfacial region. Concretely, short (long) purge times seemed to contribute (inhibit) the creation of oxygen vacancies. In order to clarify the purge time effect on the RS effect and to establish also a physical correlation between the fabrication conditions and the electrical response, X-ray photoelectron spectroscopy (XPS) analysis was carried out. Hysteretic and no hysteretic samples were used to carry out that analysis. The analyzed samples are labelled at figure 6.2. The results obtained are described in detail in the next section.
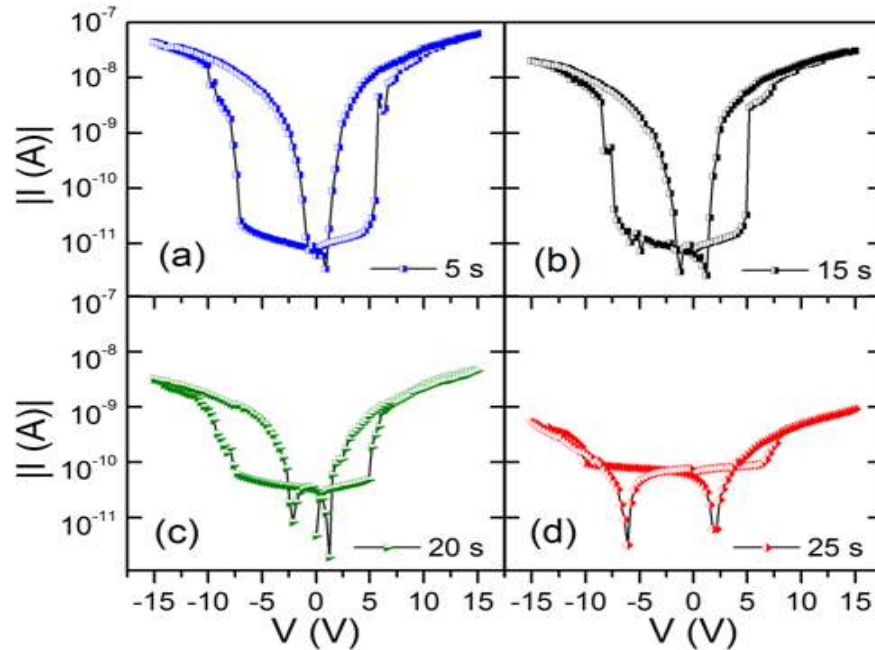
Figure 6.4: I-V curves corresponding to samples with HfO_2 grown at 200ºC and at different purge times.

6.2 X-ray Photoelectron Spectroscopy analysis

In this section we present the results obtained from the chemical characterization conducted by means of X-ray photoelectron spectroscopy (XPS). This technique provided the chemical analysis of the HfO_2 thin films both at bulk and at Ti/HfO_2 interfacial regions. The analysis was carried out on as deposited samples in order to find a physical correlation between the HfO_2 growing conditions and the electrical behaviour, i.e. the lack or display of resistive switching (RS) effect. As such, analysis was used to investigate how the HfO_2 atomic layer deposition conditions affected the chemical properties of the deposited films, and to deduce if there was any systematic relation to the observed RS behavior. The effect of the annealing treatments on the chemical properties was also studied by the analysis of annealed samples.

6.2.1   As deposited samples

We performed XPS experiments on samples fabricated at different deposition temperatures and purge times including switching samples, which display RS effect, and non-switching samples (do not display RS effect).
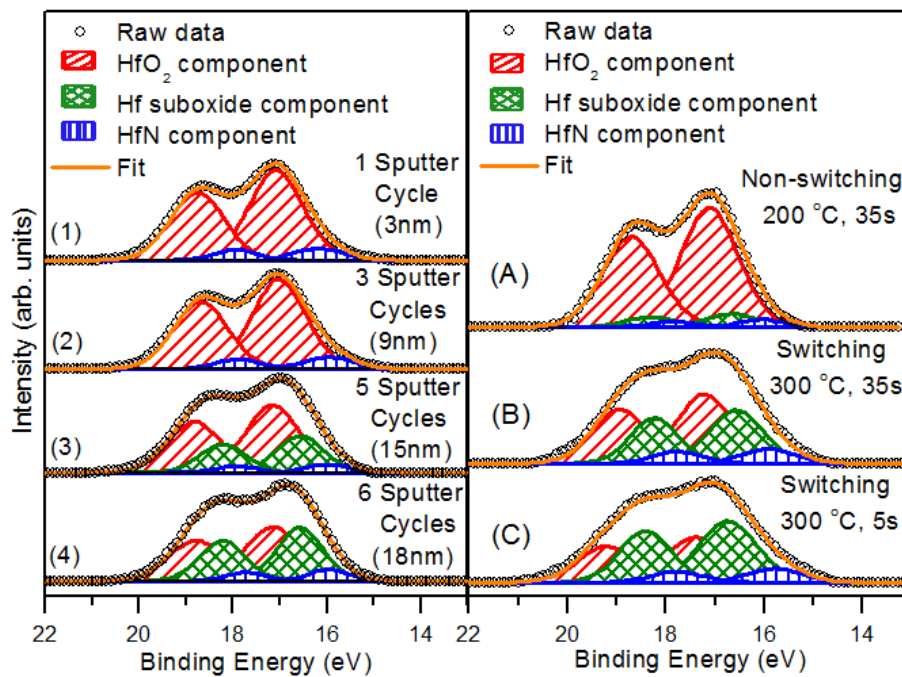

Fig 6.5: (a) Shows the evolution of the Hf 4f region, for a switching device, upon sputtering from the surface to the underlying Ti layer. The approximate depth of each profile is also detailed in parentheses. A significant presence of Hf sub-oxides content was found at the Ti interface (after 5 and 6 sputter cycles). (b) Shows the difference in Hf 4f XPS spectra at the Ti/HfO_{2-x} interfacial region for different ALD conditions (A) 200 C, 35s purge (non-switching device), (B) 300 C, 35s purge (switching device), (C) 300 C, 5s purge (switching device).

Figure 6.5 (a) shows Hf $4f$ XPS spectra film for a switching device grown at 200 C and 5s purged from four different depths in the HfO_2; near the surface (1 sputter cycle), in the bulk (3 sputter cycles), at the first detection of Ti (5 sputter

cycles) and after a subsequent sputter (6 sputter cycles). The overall shape of the spectra exhibit two contributions associated with the two non-equivalent $4f_{7/2}$ and $4f_{5/2}$ core levels. Deconvolution of the spectra was carried out in order to ascertain which Hf species were present in the film.

In all cases quantitative agreement was achieved between the Hf 4f assignment and that for the corresponding O 1s and N 1s spectra. The spectra show that near the surface and in the bulk, the film is predominantly composed of stoichiometric HfO_2 (red contributions in Figure 6.5), which exhibits an Hf 4f 7/2 peak at 17.1eV, consistent with previous studies[1-3]. A second, much smaller contribution, from a lower binding energy component (Hf 4f 7/2 at 15.9eV), is assigned to a Hf-N species (blue components), possibly from HfN_x or HfO_xN_y[2,4]. These species could arise from the presence of unreacted ALD precursor (Tetrakis (dimethylamino)hafnium) or alternatively nitrogen could be incorporated into the film from the purge gas. XPS analysis was used to detail the relative N content found in HfO_2 films prepared under different deposition conditions (see Table 6.1).

Deposition Temperature (°C)	Purge Time (s)	% Nitrogen in the HfO_2 film	
		Bulk	At Ti interface
125	5	23	25
200	5	8	6
	35	6	2.5
300	5	10	10
	35	11	10

Table 6.1: Relative nitrogen content in HfO_2 films in the bulk and at the underlying Ti interface from samples prepared under different deposition condition.

The composition of the film remained almost constant until detection of the underlying Ti. The uniformity of the Hf 4f signal during depth profiling of the bulk (up to 4 sputter cycles) indicated that no significant preferential sputtering takes place.

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Upon sputtering down to the underlying Ti layer a noticeable change in the shape of the Hf 4f spectrum is observed, with less distinction between the two spin-orbit contributions. This is due to the presence of a new component with an Hf 4f 7/2 peak at 16.5eV, which is associated with the presence of Hf suboxides[5] (green components).

To determine whether the presence of these interfacial sub-oxides is important in order to achieve RS, Hf 4f XPS spectra at the Ti/HfO$_2$ interface were acquired for switching and non-switching samples prepared under different conditions [spectrum (4) in Figure 6.5 (a) and all spectra in Figure 6.5 (b)]. Spectrum (A) was from a 200 C, 35s purged sample, which yielded a non-switching device. The spectrum was primarily composed of HfO$_2$ with very small contributions from Hf sub-oxide and HfN components. This was in contrast to spectra (B) and (C) in Figure 6.5 (b) and spectrum (4) in Figure 6.5(a), all of which exhibited substantial Hf sub-oxide components. These samples were prepared following procedures that yielded switching devices; either by decreasing the purge time [5s purge (4)], or by increasing the deposition temperature [300 C (B)] or by changing both parameters [300 C, 5s purge (C)]. After analysis of further samples, it became clear that a significant presence of Hf sub-oxides (oxygen vacancies) was required at the interfacial layer with the Ti in order to obtain reproducible hysteretic devices, which is in agreement with previous findings[6].

Table 6.2 shows the relative proportions of the different Hf species for the samples analyzed by XPS. They were calculated by the ratio of the area under the curves of the different components. Table 6.2 indicates also that larger Hf sub-oxides relative proportions are obtained when the samples are deposited coupling short purge times and high deposition temperatures. These results would agree with the trend observed on the RS response at the parameter diagram from the previous section 7.1.

Sample	%HfO$_2$	%HfO$_{2-x}$	%HfN
125°C-5s purge	38	37	25
200°C-5s purge	63.5	30.5	6
200°C-35s purge	87.5	8.5	4
300°C-5s purge	38.5	51	10.5
300°C-35s purge	52	38	10

Table 6.2: relative proportions of the different Hf species for the samples analyzed by XPS.
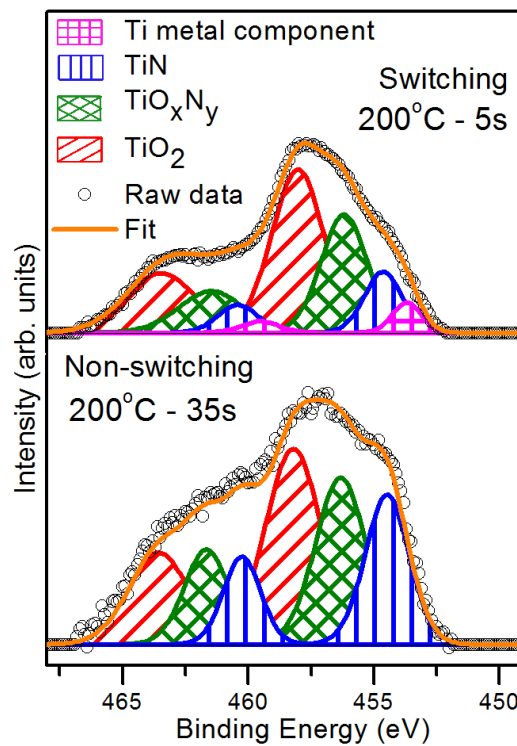

Fig. 6.6: XPS Ti 2p spectra of (a) a 5s purge, 200°C sample (switching device) (b) a 35s purge, 200°C sample (non-switching device). The spectra show the relative increase in nitrogen containing Ti components for the 35s purged sample.

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On the other hand, XPS analysis of the underlying Ti layer revealed its role as an oxygen and nitrogen gettering agent. Titanium is known for its strong affinity for forming oxygen and nitrogen compounds and has been found to act as a getter in similar device structures[7-9]. Figure 6.6 shows the Ti $2p$ XPS spectra from two different samples, one switching (200 C, 5s purge), the other non-switching (200 C, 35s purge). The overall shape of the spectra again exhibits two components due to the Ti $2p_{3/2}$ Ti $2p_{1/2}$ spin orbit doublet. The spectra were deconvoluted to assign the different Ti species present at the interface, with care to maintain a quantitative fit with the corresponding O 1s and N 1s data. For both samples the interfacial region was found to be composed of titanium oxides, oxynitrides and nitrides with little or no Ti(0) metal detected at the Ti/HfO$_2$ interface. The Ti $2p_{3/2}$ peak at 453.7eV in spectrum 6.6(a) is characteristic of Ti(0) metal[10,11], the peak at 454.6eV corresponds to TiN[10,12,13] the component at 456.4 was assigned to TiO$_x$N$_y$[10,12,14] and the Ti $2p_{3/2}$ peak at 458.2eV is typical of amorphous TiO$_2$[10,12,14]. The presence of Ti(IV) oxide was expected due to formation of a native oxide layer[15,16] on transferring the sample from the Ti sputter chamber to the ALD chamber during sample preparation. Whereas the detection of titanium nitride and oxynitride species indicated that the Ti layer scavenges oxygen (and nitrogen) from the neighboring HfO$_2$, generating oxygen vacancies in the interfacial region of the film, which are important for producing RS devices.

Further analysis of figure 6.6 shows that the nature of the Ti interfacial layer was also found to depend on the HfO$_2$ deposition conditions. The spectra show that the sample deposited using a 35s nitrogen purge time (b) had significantly increased nitrogen containing Ti components, whilst the 5s purged sample (a) exhibited less nitrogen containing components and still showed a small metallic component. These results indicated that the HfO$_2$ deposition conditions have a significant effect on the gettering potential of the underlying Ti, which in turn determines the amount of interfacial Hf sub-oxides present and hence the resistive switching behavior of the device. Long nitrogen purge times cause the Ti layer to saturate, reducing its ability

to remove oxygen from the HfO_2 layer. These results would account for the results obtained at section 6.1.2 where RS effect was supported at short purge times and inhibited at long ones. Low deposition temperatures were also found to be detrimental to the oxygen gettering ability of the Ti. Devices fabricated using the lower deposition temperature tested of 125 C (5s purge) did not exhibit hysteresis performance.
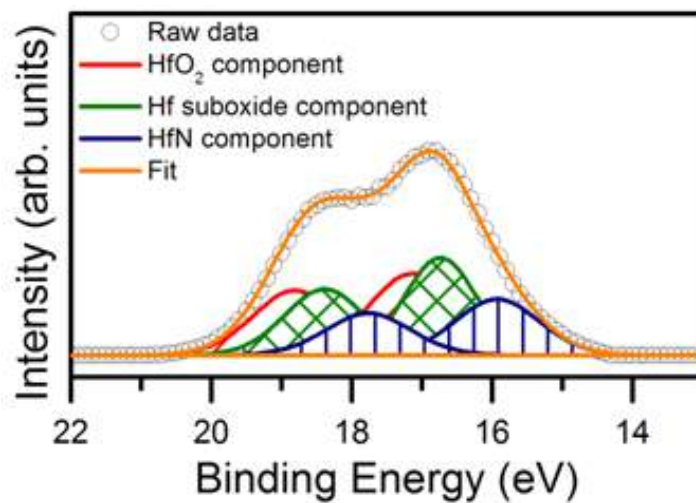

Fig. 6.7: XPS Hf 4f spectra of a sample deposited at 125 C with a 5s purge time.

However, XPS analysis of the Hf 4*f* region did not show the predominantly HfO_2 interfacial layer observed for other non-switching devices, as highlighted in figure 6.7. In fact we observed Hf sub-oxides, but more noticeably a significantly higher quantity of nitrogen containing Hf species than in devices deposited at higher temperatures. This was true not only at the interface with the Ti but throughout the HfO_{2-x} film. We propose that at this low reaction temperature (125°C) either the ALD reaction does not go to completion or the reaction by-products are not removed efficiently resulting in a contaminated film, causing poor device performance.

6.2.2   Annealed samples

Finally, XPS analysis was conducted to determine the effect of annealing processes on the chemical composition of the deposited films, and find if there is a systematic correlation to the corresponding RS performance observed described at chapter 5.4.
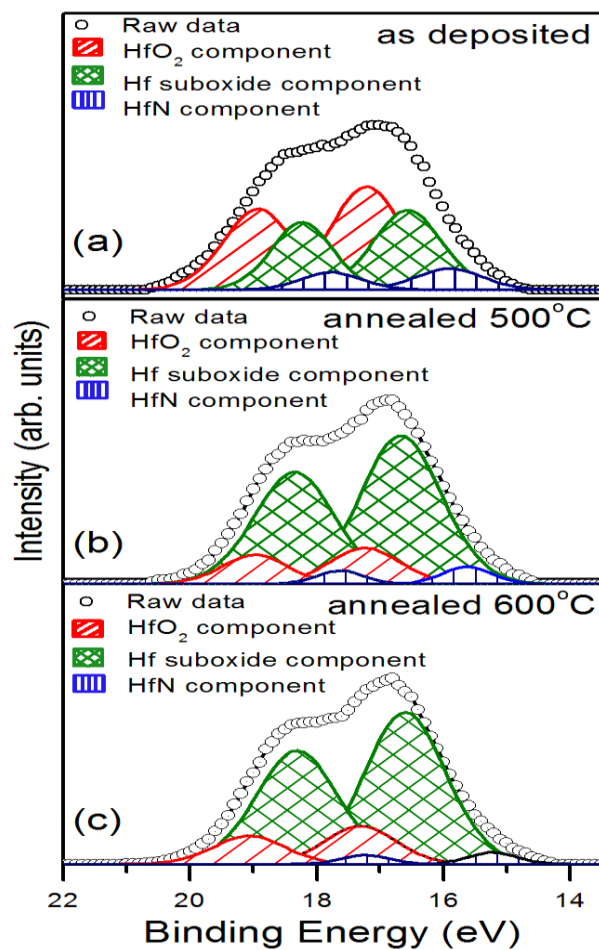

Figure 6.8: Shows Hf 4f XPS spectra at the Ti/HfO$_{2-x}$ interfacial region for (a) as deposited sample (300 C, 35s purge), after annealing treatment at 500°C (b) and at 600°C (c) for 10 s.

Figure 6.8 shows Hf 4f XPS spectra at the first detection of Ti (5 sputter cycles) from (a) a switching sample as-deposited sample (300°C and 35 s purge), (b) after an annealing process at 500°C for 10 seconds, and (c) after an annealing process at 600°C for 10 seconds. Decomposition of the spectra show HfO_2 component (red contributions in figure 6.8), HfN component (blue components), and a component at lower binding energy than the HfO_2, which was assigned to Hf sub-oxides (green components) as described above at previous analysis. The annealing treatment effect on the chemical composition was revealed mainly by a significant increase of Hf sub-oxides (oxygen vacancies) at the interfacial layer with the Ti for both annealed samples respecting the as-deposited.

Sample	%HfO_2	%HfO_{2-x}	%HfN
As-deposited	52	38	10
500°C-10s	16.5	78	5.5
600°C-10s	17.5	79	3.5

Table 6.3: relative proportions of the different Hf species for the as-deposited and annealed samples for 10 seconds for 10 seconds at 500 °C and 600 °C.

These results provided strong evidences that the annealing treatment enhances the oxygen gettering capacity and originates a larger density of oxygen vacancies at the interface with the Ti. This would yield an increment of the energy levels at the band gap and a subsequent increment of the LRS current as described at chapter 5.4. The increment of the hafnium sub-oxides, i.e., oxygen vacancies, at interfacial region revealed by XPS spectra after post-annealing treatments is quantitative reflected at table 6.3 through the relative proportion of the different hafnium species in the as-deposited sample and the two annealed.

The results obtained from X-Ray photoelectron spectroscopy (XPS) analysis provided us a direct physical correlation between the ALD growing conditions and

the RS response showed by the devices. XPS results confirmed the presence of HfO_2 sub-oxides (HfO_{2-x}) at the Ti/HfO_2 interface of the samples displaying resistive switching. In contrast, the non-RS samples showed a lack of HfO_2 sub-oxides at such interface, with the exception of the sample grown at 125°C and 5 seconds purged. In such sample, despite the detection of HfO_2 sub-oxides, a poor performance was found (non-switching) what was related to a significant quantity of nitrogen containing Hf species that contaminated throughout the HfO_{2-x} thin film. The presence of this high amount of nitrogen could be due to uncompleted ALD reactions or ineffective removal of reaction by-products at this deposition.

Thus, it seems that the oxygen vacancies source lies in the capability of the Ti layer to react with the oxygen from the HfO_2 bulk to form oxygen compounds. According to the XPS analysis the gettering capability of the Ti layer would be hinder under certain ALD deposition conditions as low temperatures and long purge times. Consequently, the growth conditions would be crucial for the switching response of the devices.

On the other hand, the XPS results are compatible with the assumption considered at previous chapters, i.e., a switching mechanism wherein the oxygen vacancies play an active role into the origin of the RS effect. In this manner, the oxygen vacancies role is related with the modulation of the interfacial Schottky energy barrier. The spatial distribution of oxygen vacancies would be driven by the action of an electric field, which would drift oxygen vacancies forth and back interfacial domains depending on the bias polarity between the near oxide and interfacial region[17-19]. In this way, under a negative bias the oxygen vacancies are attracted and pile up at the interface producing a modulation of the interface resistivity. The accumulation of oxygen vacancies can be conceived as local doping of the electronic state of the HfO_2 at the interfaces. This oxygen doping gives rise to multiple defect energy levels within the band gap region[20-24] that leads to a quasi-ohmic contact, and set up the device in the LRS. When the bias is reversed the oxygen vacancies are repelled from the interface and the Schottky energy barrier is restored in a reset process whereby the device returns to the HRS. On the contrary,

the lack of enough oxygen vacancies density at the interfacial region drives to a non-switching behaviour.

In the next chapter we will describe the measurements carried out within a temperature range to determine the electric conduction mechanism of our devices. We also designed and fabricated samples with different top/bottom electrode area ratio to discern if the resistivity modulation at the interface is a local effect or involves the whole interface area though.

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CHAPTER 7

Analysis of the electric conduction at low resistance state

This chapter covers the determination of the electric conduction mechanism at LRS based on the measurements carried out at different temperature. We also treat the characterization of a set of samples with different top/bottom electrode area ratio whose results confirm that the change of resistance involve the whole electrode area indicating an interface switching type.

7.1 Temperature effect on resistive switching

In order to achieve deeper insight in the nature of the RS mechanism we study the measuring temperature effect on the RS. It was explored by carrying out characteristics I-V curves in vacuum (base pressure 2×10^{-5} mbar) within a temperature range from 125 to 340K with a device grown at 300°C and 5 seconds purge time. The measurements were carried out using Keithley source meter 2636A at a probe station provided with a cooling system based on a helium compressor enabled to drop the sample holder temperature to 4.9K. A waiting time of 15 minutes was taken after the equipment reached each of the measuring temperatures to ensure the stabilization of the sample temperature. The measurements were carried out with the biased and grounded tips on top and bottom electrodes respectively. Figure 7.1 shows the I-V curves obtained at different measuring temperatures and clearly display the temperature influence on the RS at both bias polarities. The results revealed two main features.
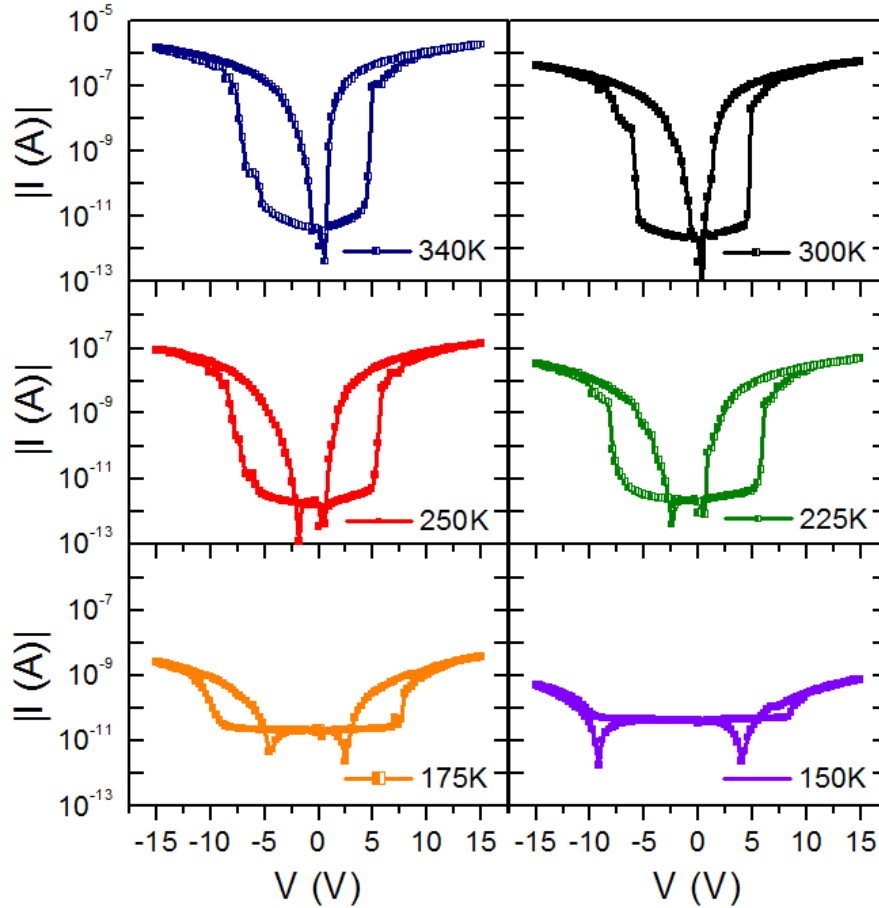
Figure 7.1: characteristics I-V curves obtained at 150K, 175K, 225K, 250K, 300K and 340K for the Ti/HfO$_2$/Co grown at 300°C and 5 seconds purge time.

On the one hand, a clear shift of the set process voltage (V$_{SET}$) value as a function of the temperature as reflected at figure 7.2. The V$_{SET}$ value decreased with the rising of the temperature until it became stable from 300K. On the other hand, a decreasing of the I$_{LRS}$/I$_{HRS}$ ratio with the dropping of the measuring temperature until the hysteretic curve faded away at 125K. These two characteristics would agree with the switching mechanism proposed above based on a diffusion process of oxygen vacancies towards and away the metal/oxide interface induced by the application of an electric field. In this way the presence of positive charged oxygen vacancies at the anode originates the doping of electronic state of the HfO$_2$ with the corresponding

energy levels at the band gap[1-5]. These energy levels lead to the modulation of the interface energy barrier triggering the set process and the corresponding change of the interface resistance. As the voltage polarity is reversed the cathode repels the oxygen vacancies and the original resistance state is recovered (reset process).
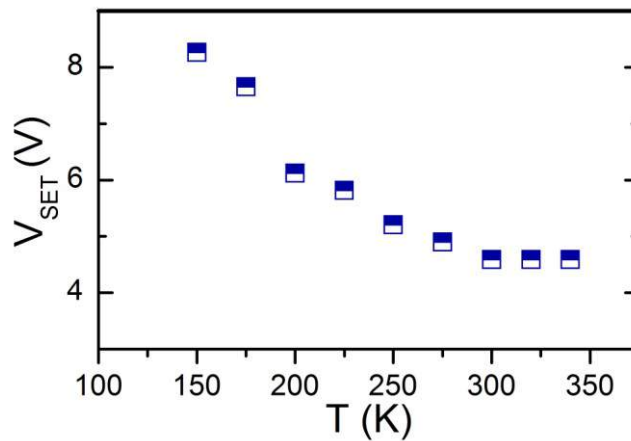

Figure 7.2: evolution of the set voltage along with the measuring temperature.

The diffusion process is also a thermal activated process and as such it would be slowed down at low temperatures. Then, it could be expected that the lower is the temperature, the higher is the voltage required to drift the necessary amount of oxygen vacancies at the interface to compensate the drop of temperature. However, there is a temperature value at which the diffusion of the oxygen vacancies seems sufficiently inhibited for hampering vacancies to reach the interface, and hence impeding the RS effect. In the case of the sample grown at 300ºC and 5 seconds purge time, the switching effect was not discerned below 150K. As regards the decreasing of the I_{LRS}/I_{HRS} ratio at low temperatures, it could be asserted to the smaller quantity of oxygen vacancies reaching the interface. It would induce an inferior energy modulation of the energy barrier and hence lower LRS currents.

Following the measurements obtained with the sample grown at 300ºC, we proceed to conduct the same I-V curve measurements with samples grown at 175ºC,

200ºC, 250ºC and 350ºC, and 5 seconds purged. A representative number of such I-V curves for each sample are shown at figure 7.3.
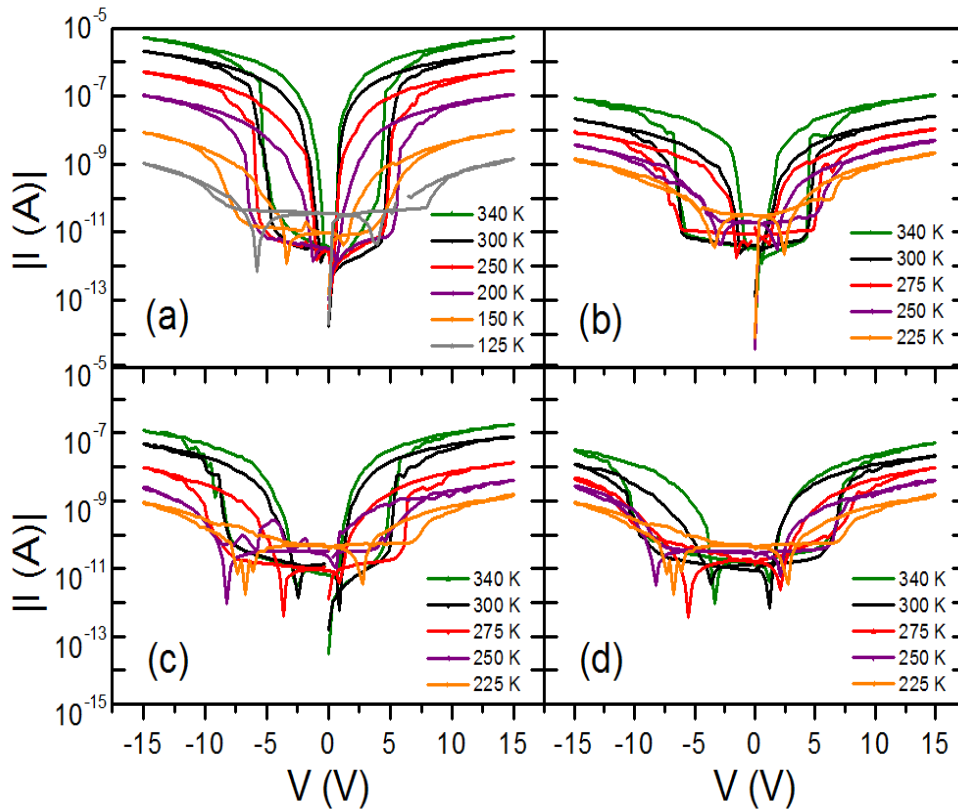

Figure 7.3: characteristics I-V curves obtained for the Ti/HfO$_2$/Co grown at (a) 350ºC, (b) 250ºC, (c) 200ºC, and (d) 175ºC, and 5 seconds purge time.

Firstly, it was observed that the hysteretic curve endures for a wider temperature range at samples fabricated at higher temperatures. For instance, at devices grown at 175ºC and 200ºC the hysteretic curve fades away at 200K, while it can be still discerned at 125K in devices grown at 350ºC. It could be accounted for a larger amount of oxygen vacancies nearby the interface which would yield RS manifestation even at 125K. In contrast, the drift of the required amount of vacancies in the direction of the interface is hindered at low temperatures for samples with

smaller density of oxygen vacancies. This leads to a RS effect display limited within a narrower temperature rank.

Secondly, the shift of V_{SET} to higher voltage values as measuring temperature decreased was found a common feature for all the devices. Figure 7.4 displays the drift of the V_{SET} as a function of the deposition temperature for devices grown at different temperatures. As the temperature diminishes the thermal diffusion becomes inhibited what makes necessary compensate it by applying higher voltage values to pile up the required number of vacancies and induce the RS.
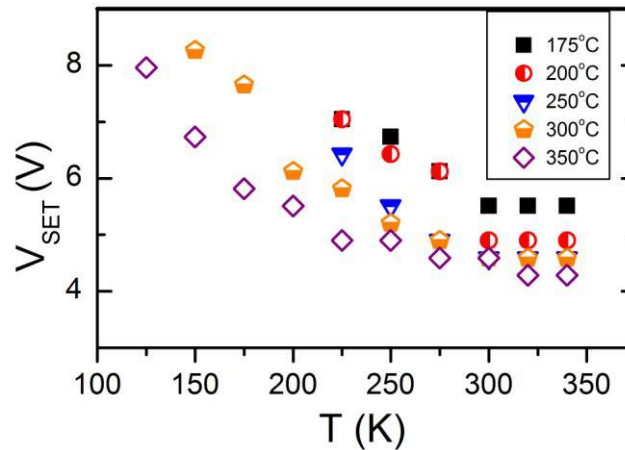

Figure 7.4: evolution of the V_{SET} along the measuring temperature for the devices grown at 175°C, 200 °C, 250 °C, 300 °C and 350 °C, and 5 seconds purge time.

Finally, the higher was the deposition temperature of the sample the larger was the I_{LRS}/I_{HRS} ratio for a given measuring temperature. It is consistent with the fact that larger oxygen vacancies densities are prompted at high temperatures as exposed previously at this section.

All these results together with the XPS analysis confirmed that the growth conditions (deposition temperature and purge time) play a decisive role respecting the amount of oxygen vacancies generated at the interface and as a consequence determine the performance of the different devices. In addition, the switching

mechanism previously suggested becomes reinforced yet again. However a question is still uncertain: is the energy barrier modulation a local effect or does it involve the whole interface? In the first case it would be related to a filamentary nature of the switching where the partial formation/annihilation of conducting filaments at interfacial regions would be the RS origin. In the latter case, the change of resistance would be extended to the whole interface region. It would entail a scaling of the device resistance with the electrode area as discussed in the introduction at section 1.3.4. In order to determine whether the RS is a local effect or can be attributed to the entire interface, a set of samples with a range of different bottom/top electrode area ratio were fabricated and characterized. The results of this study together with the determination of the conduction mechanism at LRS are detailed in the next section.

7.2 Electric conduction mechanism at LRS

In order to determine the conduction mechanism that governs the low resistive state (LRS), the normalized currents monitored at 15 V (the device at such voltage is in LRS) during the measurements of the previous section were plotted as a function of the measurement temperature [Figure 7.5(a)]. The normalized currents obtained for each of the devices exhibited very similar behaviour as can be observed at Figure 7.5(a) what would indicate that the same conduction mechanism governs at LRS for all the devices. The data obtained from the device grown at 300°C were fitted with a general equation that describes the current as a function of the temperature in insulating and semiconducting materials[6] [Figure 7.5(b)]:

$$I(T) = Io \; exp(^{To}/_T)^x \qquad (1)$$

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where Io is the residual current, To is the characteristic hopping temperature and x is the hopping exponent, which determines the transport mechanism.
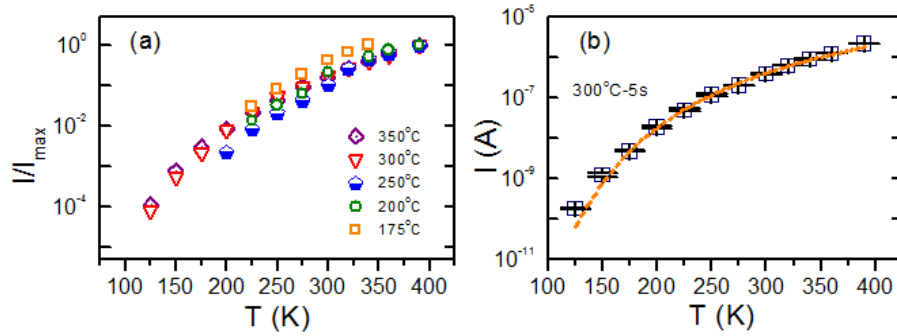

Figure 7.5: (a) temperature dependence of the current measured at 15V for devices fabricated at different deposition temperatures indicated at the legend. (b) Fitting of the currents obtained for the device at 300°C where the orange line represents the fitting obtained after applying the equation describing the conduction in insulating and semiconducting materials.

As a first approximation the data were fitted applying an exponent value of -1 showed at figure 7.5(b). It would be in agreement with either single activated transport or hopping conduction. To discriminate and determine the conduction mechanism governing at LRS, we need to carry out the fitting using different values of the exponent x. In this way, the next values were applied to the hopping exponent x: -1, -1/2 and -1/4, which correspond to nearest neighbour hopping or single activated transport, Efros-Shklovskii hooping and Mott variable range hopping respectively[7].

The fitting curves showed at figure 7.6 revealed negligible differences between each other, which did not make possible the determination of the conduction mechanism. The elucidation of the hopping exponent and thereby the conduction mechanism, was carried out via ab-initio method plotting the hopping energy activation as a function of the temperature [w (T)], versus the measurement temperature. The hopping energy activation was calculated by the equation[6]:

$$w\,(T) \cong -\,\bar{T}\,\frac{\Delta Ln\,\rho}{\Delta T} \qquad (2)$$

where $\bar{T}$ is the mean temperature, $\Delta Ln\,\rho$ is the resistance variation registered, and ΔT is the temperature variation in between two consecutive measurement temperatures.
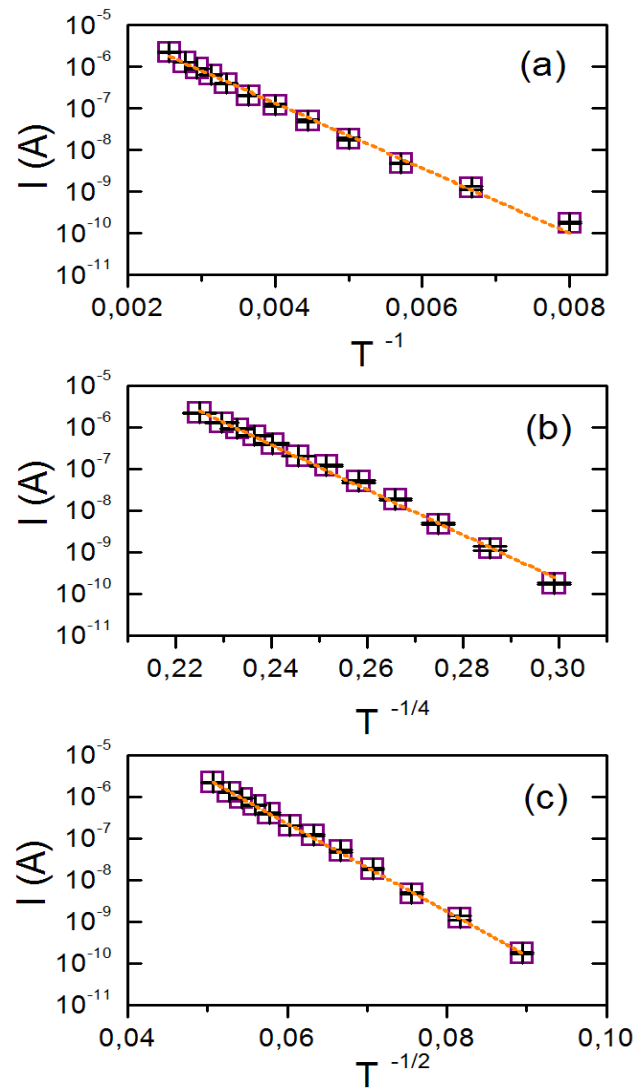

Figure 7.6: Plot of I at 15V vs. T^{-x} applying different values for the hopping exponent: -1 (a), -1/4 (b) and -1/2 (c) and the corresponding fitting curve.

The figure 7.7 displays the plot of w (T) versus the mean temperature. The slope of the fitting curve yields the hopping exponent value, and thus determines the conduction mechanism. The hopping exponent value obtained for x ≈ -1/2 means that Efros- Shklovskii variable range hopping (ES-VRH) is the conduction mechanism that governs at LRS in our devices.
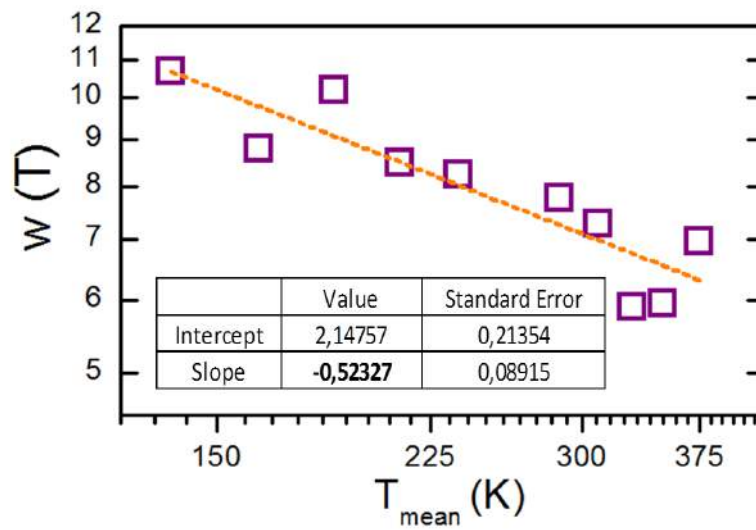

Figure 7.7: Plot of w (T) vs. T mean and the fitting curve obtained via ab-initio method. The curve slope yields the hopping exponent value (≈ - 0.52).

ES-VRH is characterized by charge hopping in between energy states of similar energy and implies the presence of energy states in the band gap of the material with several singularities; the energy states are within a narrow range of energy, and a small gap at the own energy states band originated by defects. This scenario is consistent with the presence of defects (oxygen vacancies) in the interface, complementing and supporting the results given by the XPS analysis exposed at the previous chapter 6.

7.3 Study of electrode area on resistive switching

The results along this thesis seem to indicate a switching mechanism based on the interface energy barrier modulation induced by changes in the oxygen vacancies concentration at the interface regions driven by the electric fields. In order to rule out a switching mechanism of filamentary nature, we fabricated a set of samples with patterned bottom electrodes as described at section 2.2. The rationale was to create different bottom/top electrode area ratio to study the RS effect and the currents obtained at LRS.
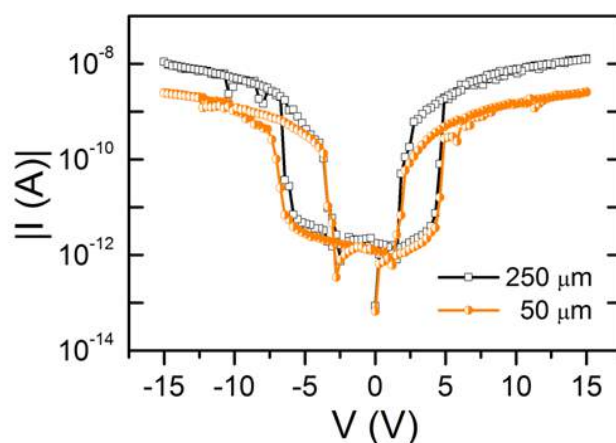

Figure 7.8: I-V curves obtained for devices with 100 m top size, and 50 m and 250 m width bottom electrodes.

The difference between the filament and interface type of RS could be identify with the area dependence of the device resistance[8] as reported on perovskites[9] and TiO_x[10]. The patterned bottom electrodes were strips of different widths in a range from 25 to 250 μm, while the patterned top electrodes size was confined between 100 μm to 650 μm. The different devices were characterized by the performance of I-V curves (see figure 7.8) following the measuring protocol described at the section 2.3.

ANALYSIS OF THE ELECTRIC CONDUCTION AT LOW RESISTANCE STATE

If the assumption of a RS mechanism originated by the energy modulation of the whole metal/oxide junction would be correct, then the currents registered at LRS should be proportional to the electrode area involved. Figure 7.9 displays the currents monitored at 15V when the device was set into the LRS versus the bottom electrode width for devices with different top size electrodes. The legend indicates the top electrode size and the x-axis indicates the width of the bottom electrode. The analysis of the data is carried out assuming a linear behaviour at LRS that entails both a current increase proportional to the electrode area ratio and currents linear fitting including the axis origin. Under these considerations we can state that the resistance at LRS can be expressed as follows:

$$R = \frac{V}{I} = \frac{\rho\, t}{L\, w} \quad (3)$$

where   is the resistivity of the HfO_2, t is the HfO_2 thin film thickness, L is the top electrode size and w the bottom electrode width.

Considering the equations introduced above the slope of each graph (m) can be expressed as:

$$m = \frac{V\, L}{\rho\, t} \qquad (4)$$

The graphs from figure 7.9 exhibits a linear relation between the current measured at LRS and the electrode area involved, confirming that the current is proportional to the electrode area.

If we plot the slopes obtained from the four graphs corresponding to different top electrode sizes versus such top electrode sizes, we should find a linear relation in the case a linear behaviour governs the electrical conduction at LRS. Thus, if we obtain a linear fitting the curve equation can be defined as follows:

$$\frac{V\, L}{\rho\, t} =\ m\, L + b \qquad (5)$$

where m is the slope of the curve, w is the bottom electrode width and b is zero as the curve pass through the axis origin.
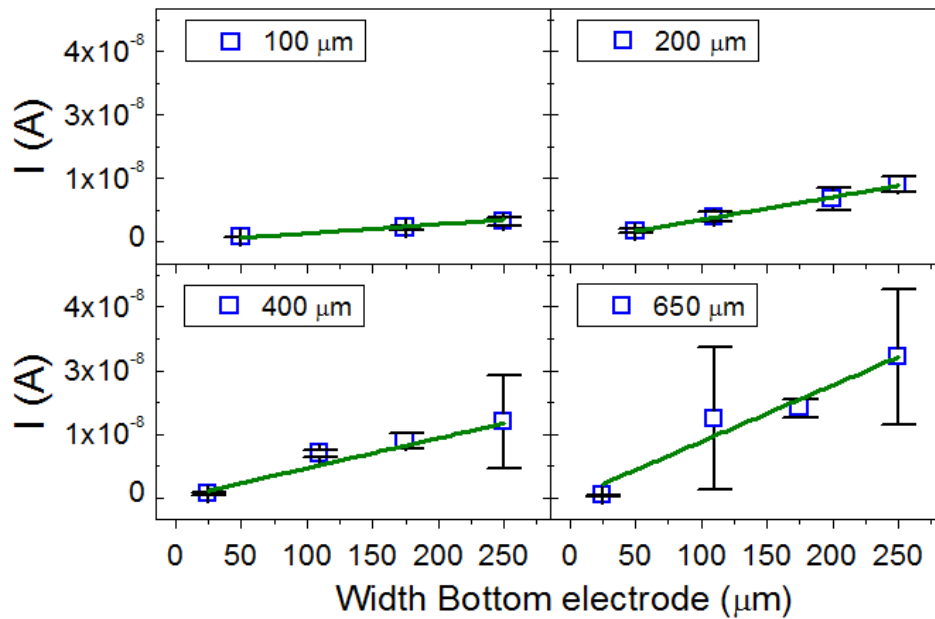

Figure 7.9: Current sensed at 15V versus the bottom electrode width for the four different top electrode sizes. A linear behaviour was found in all the cases as showed by the linear fitting.

The figure 7.10 confirms the linear relation between electrode area and LRS currents. This is consistent with the RS mechanism proposed along this work based on the interface resistance modulation by changes in the local density of oxygen vacancies at the interfacial regions induced by an electric field. This allows us to determine the RS basis among the diverse switching mechanism discussed at the Introduction, confirming that the resistive switching in our HfO_2-based devices takes place over the whole area of the device and it is not an effect restricted at local interfacial regions.
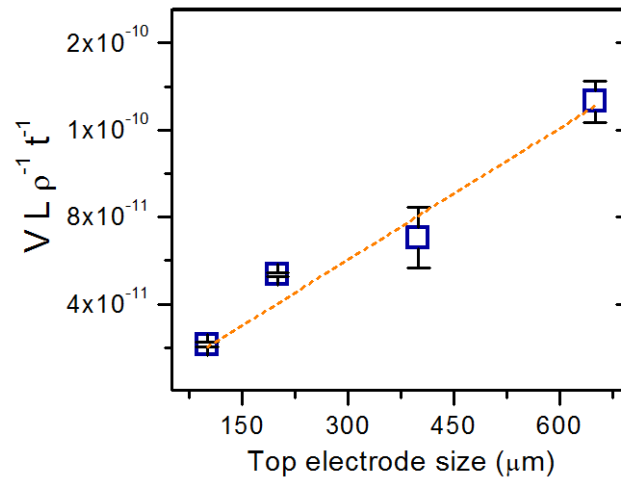
Figure 7.10: slopes given by the previous linear fitting versus top electrode size.

In the next chapter, we will develop a mathematical framework in order to validate the switching mechanism above proposed to describe the behaviour observed at our devices. In addition we rationalize the whole behaviour of the device and reproduce the experimental current-voltage curves of devices with different metallic contacts via a mathematical framework based on simple assumptions

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CHAPTER 8

Proposed resistive switching model

As it was exposed in previous sections, the analysis of the results obtained along this thesis led to point at a scenario of two complementary interfaces displaying bipolar resistive switching. The RS takes place at the metal/oxide interfaces and it would be promoted through the modulation of the energy barrier height of the junction by the drift of oxygen vacancies forward and back the interfacial region. Such energy barrier modulation would be caused by the arising of energy states at the band gap introduced by the oxygen vacancies at the interface. We shall articulate that physical scenario into the following mathematical framework.

8.1 Description of the model

8.1.1   Basic components of the model

The electrical current is modulated by three components, the Ti/HfO_2 interface, the bulk HfO_2 and the HfO_2/Co interface. Both interfaces are modelled as metal/semiconductor junctions with barrier height ϕ_1 in the case of the HfO_2/Co interface and ϕ_2 for the Ti/HfO_2 interface. The bulk HfO_2 is modelled as a linear resistor with constant resistivity ρ_B and thickness L. The applied bias is the sum of the voltage drop in each of the three components,

$$V = V_1 (J, _1) + J_B L + V_2 (J, _2) (1)$$

where same current density J flows through all the components. The functions V_1 (J, ϕ_1) and V_2 (J, ϕ_2) express the current-voltage (I-V) characteristics of each Schottky barrier.

The presence of oxygen vacancies modifies the height of the Shottky barriers, ϕ_1 (n_1) and ϕ_2 (n_2), being n_1 and n_2 the density of oxygen vacancies at the interfaces. Solving J from equation 1, together with the functions V_1 (J,ϕ_1), V_2 (J, ϕ_2), ϕ_1 (n_1) and ϕ_2 (n_2) lead to the general equation:

$$J = f (V, n_1, n_2), \quad (2)$$

which does not have an algebraic in the present work since equation 6 is numerically solved. The RS is induced by to the modulation of the barriers by means of n_1 and n_2. In fact, the application of voltage pulses to the device generates electric fields V_1 and V_2 strong enough to overcome the anchoring energy of the oxygen vacancies to the HfO_2 matrix. It generates an ionic current that introduce or remove vacancies from the interfaces depending on the polarity. Notice that there are two kinds of barriers in the system, as well as two currents: an electric current of electric carriers and an ion current of oxygen vacancies. The former, J, flows through the HfO_2 layer; the carriers has to overcome the injection barrier ϕ_1 or ϕ_2 depending on the current polarity. The latter is activated when the oxygen vacancies overcome the anchoring energy to the matrix, V_0.

8.1.2 Modulation of the vacancy content at the interfaces

We consider the bulk as an infinite source/sink that exchanges vacancies with the interfaces. The thermally activated exchange is described by the following differential equations:

$$\frac{dn1}{dt} = sgn\,(V1)\cdot a\cdot exp\left[-\beta\cdot(V0-|V1|)\right] \qquad (3)$$

and

$$-\frac{dn2}{dt} = sgn\,(V2)\cdot a\cdot exp[-\beta\cdot(V0-|V2|)], \qquad (4)$$

where q V_0 is the anchoring energy of the vacancies to the bulk and a an (unknown) attempt rate. $=q\,k_B^{-1}\,T^{-1}$ being k_B the Boltzmann constant, q the carrier charge and T the temperature. These equations indicate that flux of vacancies entering the interfaces (or coming out from it), is controlled by the barrier V_0. The voltage drop at the interfaces, V_1 and V_2, effectively reduce this barrier and exponentially increases the flux of vacancies.

8.1.3 Current-voltage characteristics of the metal-semiconductor interfaces

We assume the functional forms for the current density through the HfO$_2$/Co interface (subscript R):

$$J = J_R\,(n_R)\,[exp(\ V_R)-1] \qquad (5)$$

The Ti/HfO$_2$ interface (subscript L) is equivalent but in the opposite direction:

$$J = J_L\,(n_L)\,\{exp[\ (-V_L)]-1\} \qquad (6)$$

The saturation currents J_L and J_R depend on the barriers as follows:

$$J_{L,R} = A^{**}\,T^2\,exp[-\ _{L,R}\,(n_{L,R})] \qquad (7)$$

where A^{**} is the reduced effective Richardson constant.

8.2 Comparison between experimental and modeled I-V curves

The conceptual picture of two complementary interfaces presenting bipolar resistive switching, confirmed by the hysteresis switching loops (HSLs) measurements at section 5.2.2. is schematized in Fig. 8.1. In the literature, this configuration was reported as a "switchable rectifier"[1], and in a more general context, it belongs to the family of devices that presents complementary resistive switching[2-5]. The device can be divided into [from left to right in Fig. 8.1(a)] a left contact (C_L), an interface region (I_L) modeled as a Schottky barrier, a bulk layer and finally the interface region (I_R) corresponding to the right contact (C_R). The energy band diagram of the system in thermal equilibrium, assuming an n-type semiconductor[6], is presented in Fig. 8.1(b). The RS mechanism found in our devices is attributed to local changes in the oxygen vacancy density at the interfaces by means of electric field. These changes result in a modification of the injection barriers, which in turn produces a modulation of their effective resistance. This mechanism has been widely reported for several systems[7-9] as well as for HfO_{2-x}[10-13] In fact, oxygen vacancies originate a sub-band at the HfO_{2-x} bandgap[14, 15], turning the Schottky barrier into an ohmic junction[16]. The SET process occurs when local electric fields increase the concentration of oxygen vacancies at the interfaces. The RESET process (at opposite polarity) removes the oxygen vacancies from the interfaces, restoring the original injection barrier. Typically our device can display three different configurations, with only one of the interfaces in LRS [as in Fig. 8.1(c) and (d)] or with both interfaces in LRS [Fig. 8.1(e)]. As we shall later see, a state with both interfaces in HRS is not recovered in normal operation. The electrical characteristics of configurations formed by two switching interfaces in series, has been rationalized by mathematically modelling the system[17,18].
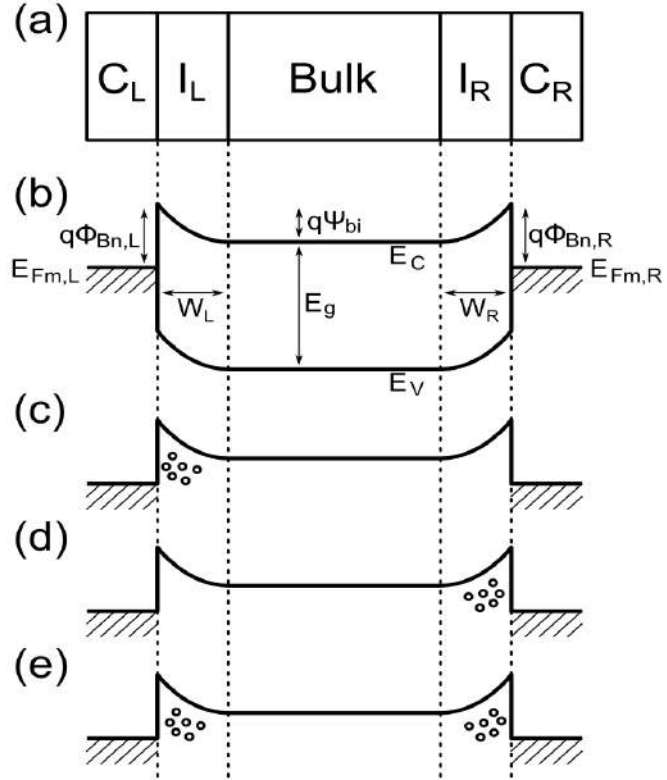
Figure 8.1: (a) schematic illustration of the structure of our devices. (b) Energy band diagram at thermal equilibrium of the system, where $E_{Fm,L}$ and $E_{Fm,R}$ are the Fermi energies of the metal contacts (C_L, C_R), W_L and W_R are the widths of the depletion layers, E_g is the energy band gap of the semiconductor, $q\psi_{bi}$ is the built-in potential, E_V and E_C are the valence and conduction band respectively and $q_{Bn,L}$ and $q_{Bn,R}$ are the energy heights of the Schottky barriers. (c-e) different possible configuration of the system; with high concentration of oxygen vacancies (spheres) at the left interface (c), right (d) and in both interfaces (e). For the sake of simplicity, in this plot we represented the injection barriers alike and not changing after the introduction of the oxygen vacancies. Actually, in our model we assume that the injection barriers are strongly modified by the oxygen vacancies, turning the metal-semiconductor interfaces into ohmic contacts. We also account for unlike junctions.

We articulate the physical scenario described above into the following mathematical framework. The current flowing through the device, I, is modulated by

the two interfaces (I_L and I_R, modeled as Schottky barriers) and the semiconducting bulk. The bulk is modeled as a linear resistor with constant resistivity, i.e., we consider non-linear effects only at the interfaces.

The applied bias V is the sum of the voltage drop at each of the three components:

$$V = -V_L(-I, n_L) + I \, R_B + V_R(I, n_R) \qquad (8)$$

where $V_{L,R}$ are the potential drop at each interface, $n_{L,R}$ are the concentration of oxygen vacancies at the interfaces, and R_B is the resistance of the bulk region. The functions $V_{R,L}$ ($I, n_{R,L}$) express the rectifying characteristics of the metal-semiconductor interfaces. Here we assume that the transport through the interfaces, can be captured by the thermionic-emission-diffusion model for conduction in metal-semiconductor interfaces[6]:

$$V_{R,L} = \frac{k_B T}{q} \ln\left[1 + \left(I / i_0\left(n_{R,L}\right)\right)\right] \qquad (9)$$

where k_B is the Boltzmann constant, q the carrier charge, T the temperature and i_0 the saturation current. This assumption is based on the hypothesis that it is not possible to develop a stable large reverse voltage across the interfaces. In fact, as soon as the electric field increases, it activates the introduction of oxygen vacancies towards the interface, increasing the saturation current ($i_0 \propto n_{R,L}$)[6]. Thus RS is modeled as a modulation of the energy barriers by means of n_R and n_L :

$$\frac{d}{dt} n_{R,L} = \text{sgn}(V_{R,L}) \exp\left(-E_0 + \left|V_{R,L} / W_{R,L}\right|\right) \qquad (10)$$

where E_0 is the anchoring energy of the ions to the matrix (i.e. oxygen vacancies to the HfO$_{2\text{-x}}$) and W is the depletion layer width of the interface. The application of voltage pulses generates electric fields V_L/W_L and V_R/W_R strong enough to overcome the anchoring energy of the ions[17], triggering a redistribution of vacancies between the bulk and the interfaces. Whether the electric field introduces or removes ions from the interfaces depends on the polarity. We obtain the temporal evolution of vacancy distributions at the interfaces, n_L and n_R , by numerical integration of Eq. (10). The integration must be performed in self-consistency with Eq. (8) and Eq. (9), obtaining also the evolution of the device current I and the voltage drop at each interface for any applied voltage waveform V(t). In short, we can simulate the I-V characteristics and study the distribution V along the interfaces and the bulk. Concerning the modeled curves presented, all them were performed as follows. The initial status of the device was supposed to be $n_{R,L}$ = -ln(10^{-15}) (units are arbitrary throughout this section). Then we modeled the application of voltage pulses sweeping V = 0 $\rightarrow$ +15 $\rightarrow$ -15 $\rightarrow$ 0, in steps of 0.01V. At each step the saturation currents were set to i_0 = exp(-$n_{R,L}$) and then the total current was calculated by solving Eq. (8) by the Newton-Raphson[19] method with accuracy=10^{-20}. We assumed k_BT/q=0.025 and R_B=10^8. Once I is obtained, the voltage drop at each component was calculated (Equations 8 and 9), and then by means of Euler approximation of Eq. (10), we updated the parameter n at each interface[19]. We set E_0=4.9 and $W_{R,L}$=3 in the case of the Ti/HfO$_{2\text{-X}}$/Co structure. During all the calculation, $n_{R,L}$ were kept between -ln(10^{-15}) < $n_{R,L}$ < -ln(10^{-6}).

Figure 8.2(a) shows the excellent agreement between experimental and simulated I-V curves for Ti/HfO$_{2\text{-x}}$/Co. The evolution of these simulated parameters is crucial for the interpretation of the I-V curve, which is described in figure 8.3 (a-c). The current in the first quadrant of the I-V loop (positive bias) is governed by the Ti/HfO$_{2\text{-x}}$ interface (I$_L$) and the bulk, whereas, it is dictated by the HfO$_{2\text{-x}}$/Co interface (I$_R$) and the bulk in the third quadrant (negative bias). We can only infer the behaviour of the "hidden" interfaces with the aid of the numerical simulations. The

sequence of the different states of the system is described in figure 8.3 together with the voltage at the interfaces. This sequence is numbered (1) to (6), in accordance with figure 8.2.
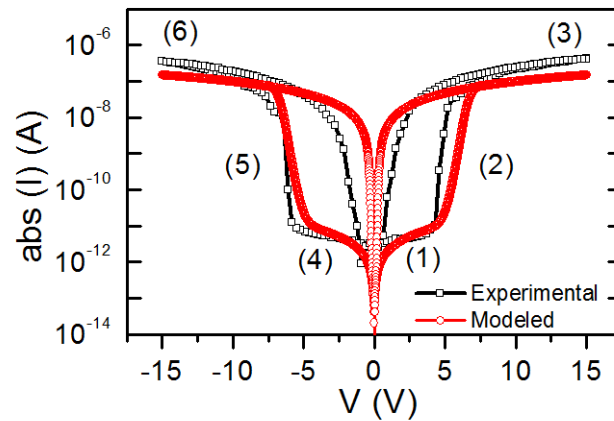

Figure 8.2: experimental and simulated I-V curves for the Ti/$_{HfO2-x}$/Co devices.

We start our analysis with the Ti/HfO$_{2-x}$ interface in HRS (1) (almost free of oxygen vacancies) and the HfO$_{2-x}$/Co interface in LRS (with a high concentration of vacancies). Initially, almost all the potential drops in the Ti/HfO$_{2-x}$ interface, which is the main limitation for the current. When this voltage reaches the V$_{SET}$ of the Ti/HfO$_{2-x}$ interface (2), it switches to the LRS (3). The applied voltage turns to drop mainly at the bulk, which is now the limiting factor for the current. Concurrently the voltage drops slightly at I$_R$ as the vacancies are repelled, and I$_R$ switches to HRS. Nevertheless, the RESET of this interface has not effect in the current as long as the device is biased with positive voltage. When the bias polarity is reversed to negative values (4), the I$_L$ is still in LRS and I$_R$ in HRS where the main potential drop occurs. In this quadrant, the SET of the HfO$_{2-x}$/Co interface is clearly reflected (5), but not the subsequent RESET step of the Ti/HfO$_{2-x}$ interface. Essentially, for negative bias, the HfO$_{2-x}$/Co interface limits the current until it SETs, then the current is dominated by the bulk. In this way, as the V$_{SET}$ of the HfO$_{2-x}$/Co interface is reached (5) it switches

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to LRS (6) and the potential drops predominantly again in the bulk. Simultaneously I_L returns to the HRS as the oxygen vacancies move back towards the bulk.
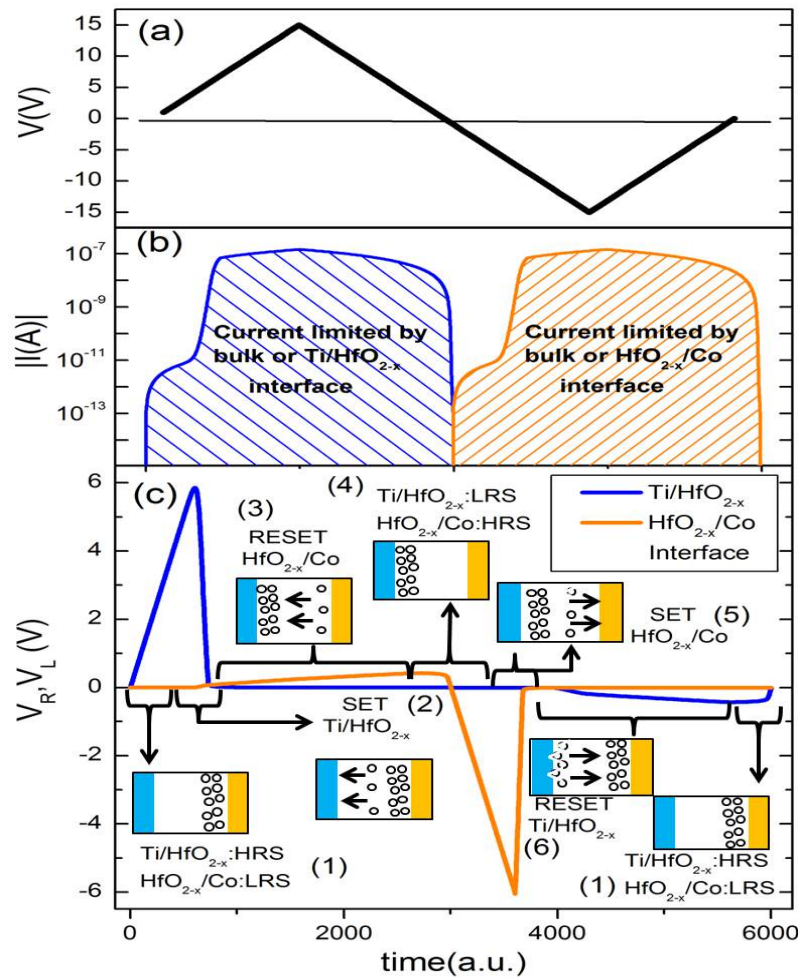

Figure 8.3: (a-c) Evolution of the simulated parameters in time-steps, corresponding to the numerical integration presented in figure 8.2. For positive bias (voltage is presented in panel (a), the HfO_{2-x}/Co interface do not limit the injection of carriers to the devices; the current is governed by the Ti/HfO_{2-x} interface and the bulk, while for negative bias it is limited by HfO_{2-x}/Co interface and the bulk [see panel (a)]. The sequence of the different states of the system is described in panel (c) together with the voltage at the interfaces. This sequence is numbered (1) to (6), in accordance with figure 8.2.

We finally consider a non-trivial confirmation of the whole model, testing it in devices with configuration Ti/HfO$_{2-x}$/Au, i.e. we substituted the Co electrode by Au. In the case of the Ti/HfO$_{2-X}$/Au device the asymmetry in the modelled behaviour was obtained by increasing 3 times the W$_R$ ($W_R = 3W_L$). The rationale behind this substitution lies in the marked different in the enthalpy of these two metals to react with an HfO$_2$ matrix[20].
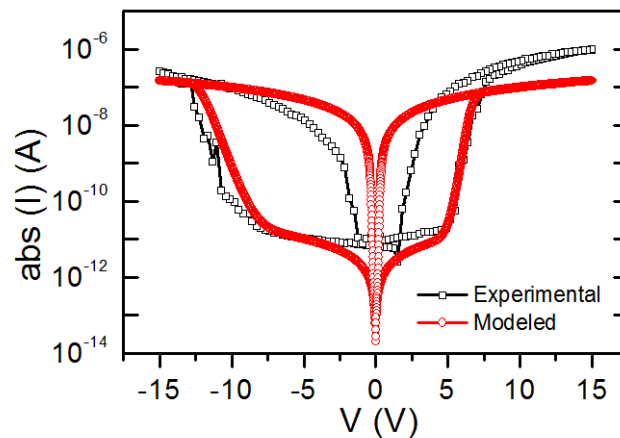

Figure 8.4: experimental and simulated I-V curves for the Au/HfO$_{2-x}$/Ti devices.

The modification of the I$_R$ should mainly impact on the third quadrant (negative bias) and indeed it creates a marked asymmetry in the I–V characteristics (Figure 8.4). As predicted, positive bias senses the state of the Ti/HfO$_{2-x}$ interface (I$_L$) while negative bias senses the HfO$_{2-x}$/Au interface (I$_R$). Moreover, figure 8.4 presents the perfect agreement when we introduce an asymmetry in the widths of the depletion layers W$_R$ = 3 W$_L$ in equation (10). This is consistent with a picture in which a "textbook" Schottky barrier is formed at I$_R$ when the Au electrode is in contact with the semiconductive layer. In contrast, the higher reactivity of the Ti effectively reduces the extension of the barrier [7].

In conclusion the mathematical framework has allowed us to verify the switching mechanism governing our devices. It also helped us to elucidate clearly the interplay between the two switching interfaces and the particular behaviour of the I-

V curves exhibited together with the fact that each interface is univocally associated to a specific quadrant of the I-V hysteresis loop.

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CONCLUSIONS

The fabrication and characterization, both physical and electrical, of HfO_2-based metal/oxide/semiconductor (MIS) and metal/oxide/metal (MIM) devices were carried out in order to analyze its potential application as non-volatile memory device. The HfO_2 thin films were grown by means of atomic layer deposition (ALD). The memory properties are based on the resistive switching (RS) effect displayed by the devices.

Initially the samples were characterized by conducting current-voltage (I-V) curves. The electrical characterization results from MIS samples revealed that they did not satisfy the properties required to a potential non volatile memory and were discarded. On the other hand, among the MIM samples characterized there was a sample in particular ($Ti/HfO_2/Co$) that showed remarkable good properties and it was more deeply characterized as described ahead. The electrical characterization of MIM samples revealed an unusual non-crossing current-voltage hysteresis loop. The interpretation of the I-V curve was accomplished via different electrical measuring protocols. Thus, minor loops and hysteresis switching loops enabled to disentangle the switching properties of each individual interface which exhibited bipolar RS. The most significant feature was the complementary character of the RS displayed by opposite interfaces, i.e., the effect of the electrical field on the interface resistance is opposed and concurrent. This non-trivial interplay of both switching interfaces yielded to the characteristic non-crossing I-V hysteresis loop of our devices. Additionally the memory properties were tested and confirmed after performing 1.5 $x10^3$ train pulses without degeneration in the non-volatile memory capacities. Also retention and stability capacities were proved via different measuring protocols. An extensive study of the ALD growth conditions effect on the RS response was carried out by fabricating 26 different MIM samples within a range of different deposition temperatures (from 125 to 350ºC) and purge time (from 1 to 35 seconds). The electrical characterization results assembled into a parameters diagram where the

CONCLUSIONS

deposition conditions and absence/ manifestation of RS seemed to be interrelated. The strong influence of the deposition conditions on the RS behavior could provide us a hint on the switching source, if the role played by the growing conditions can be elucidated. In order to establish a correlation between growing conditions and electrical performance, XPS analysis was conducted in several samples grown at different conditions and showing opposite RS response. On the one hand the corresponding results constituted the physical correlation between growing conditions and electrical behaviour by relating the absence (display) of the RS with the lack (existence) of HfO_2 sub-oxides at the interface. On the other hand, these results enlightened the physical origin of the switching mechanism observed.

In this way, the results obtained along this thesis suggested a hypothesis whereby the resistive switching origin is related with the local density variation of oxygen vacancies at the interface region. The diffusion towards/away the interface of such defects is electrical field induced, and the presence of the oxygen vacancies at the interface produces the arising of energy states within the interface energy band gap, which enable the modulation of the interface resistance. The metal/oxide interfaces commute between a HRS, due to the injection barrier of the metal-semiconductor interface, and a LRS caused by an accumulation of oxygen vacancies that turns the interface into an ohmic contact.

Lastly, the development of a mathematical framework based on the assumptions earlier described, allowed us to mathematically study and rationalizes the whole behaviour of the devices as well as reproduces the experimental I-V curves verifying the proposed switching mechanism.

Due to the limited time for the realization of the present thesis, there is some characterization work that has not been carried out. Such work could be appealing for a deeper understanding of the memory device and the conclusions would gain strength. The further characterization work could be such as:

_ Analysis and determination of the electric conduction mechanism at the high resistance state (HRS)

_Chemical characterization by means of X-ray photoelectron spectroscopy (XPS) of the Co/HfO_2 and Au/HfO_2 interfaces

LIST OF PUBLICATIONS

"HfO$_2$ based memory devices with rectifying capabilities", C. Quinteros, R.Zazpe, F.G.Marlasca, F.Golmar, F.Casanova, P.Stoliar, L.Hueso, and P.Levy, **J. Appl. Phys**. 115, 024501 **(2014)**.

"Resistive Switching Dependence on Atomic Layer Deposition Parameters in HfO2-based Memory Devices", R. Zazpe, M. Ungureanu, F. Golmar, P. Stoliar, R. Llopis, F. Casanova, D. F. Pickup, C. Rogero, and L. E. Hueso. **J. Mater. Chem. C, (2014)**.

"Resistive switching in rectifying interfaces of metal-semiconductor-metal structures", R. Zazpe, P. Stoliar, F. Golmar, R. Llopis, F. Casanova1 and L. E. Hueso, **Applied Physics Letters** 103, 073114 **(2013)**.

"A Light-Controlled Resistive Switching Memory", M. Ungureanu, R. Zazpe, F. Golmar, P. Stoliar, R. Llopis, F. Casanova and L.E. Hueso, **Advanced Materials** 24, 2496 **(2012)**.

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